FLUKE

2280 SERIES

DATA LOGGER

Service Manual

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*For European customers, Air Freight prepaid.

John Fluke Mfg. Co., Inc., P.O. Box C9090, Everett, Washington 98206

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SECTION 1

HOW TO USE THIS MANUAL

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INTRODUCTION

WARNING

THESE SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID ELECTRIC SHOCK, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN THE USER MANUAL UNLESS YOU ARE QUALIFIED TO DO SO.

The 2280 Series Service Manual is a service and maintenance guide to the Data Logger. It complements two other volumes in the 2280 Series Manual Set, the 2280 Series System Guide and the 2280 Series User Guide. The Service Manual covers standard mainframe and option assemblies, and presents general maintenance, cleaning, performance testing, calibration, and board-level troubleshooting procedures. Theory of operation, parts lists and schematics are also included in the Service Manual.

This Service Manual is intended for use by technicians and maintenance personnel who need an in-depth coverage of the inner workings of the 2280 Series Data Logger. Information needed to maintain the Data Logger as well as isolate problems to specific circuit board assemblies is given in this manual. Once the defective assembly has been identified, repair can be accomplished through our Module Exchange Program (MEP) in most cases. MEP cannot be transacted in some countries. It is recommended that you contact you local Fluke authorized Service Facility (listed in Appendix B) to obtain instructions for replacement or repair. Theory of operation sections and schematics are provided in this manual to aid a qualified person in troubleshooting beyond the circuit board level.

ORGANIZATION

Section 1 How to Use This Manual

Describes the organization and use of the Service Manual.

Section 2 General Information

Describes the Data Logger and its available accessories and options. Required test equipment, shipping, and factory service information are included here.

Section 3 Theory of Operation

Covers the theory of operation for the Data Logger mainframe. Option assembly theory is contained in the individual option subsections of Sections 8, 9, and 10.

Section 4 Maintenance

Describes maintenance of the instrument. Cleaning instructions, internal access procedures, and mainframe performance testing are included here.

Section 5 Troubleshooting

Consists of diagnostic self-tests and performance tests designed to isolate a malfunction to the circuit board level. Component level troubleshooting may be performed using the Theory of Operation (Section 3) and Schematic Diagrams (Section 7).

Section 6 List of Replaceable Parts

Contains parts lists for the Data Logger mainframe and gives parts ordering information. Option assembly parts lists are in the individual subsections of Sections 8, 9, and 10.

Section 7 Schematic Diagrams

Presents Data Logger mainframe schematics on foldout pages. Schematics for option assemblies are located in the individual option subsections.

Section 8 Options -160 Through -169

Covers Options -160 through -169 in subsections ordered numerically by option number. Includes theory of operation, maintenance procedures, performance validation procedures, calibration instructions, schematics, and a replacement parts list.

Section 9 Options -170 Through -179

Covers Options -170 through -179 in subsections ordered numerically by option number. Includes theory of operation, maintenance procedures, performance validation procedures, calibration instructions, schematics, and a replacement parts list.

Section 10 Options -200 and Above

Covers Options -200 and above in subsections ordered numerically by option number. Includes theory of operation, maintenance procedures, performance validation procedures, calibration instructions, schematics, and a replacement parts list.

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A Specifications
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HOW TO USE THE MANUAL SET

2280 Series User Guide

This book describes the Data Logger from top to bottom. A beginner could use it as a complete course in programming the Data Logger in a data acquisition system; whereas, a more experienced user would probably only need parts of it for orientation and quick reference. An untrained operator will find all the basics here as well.

2280 Series System Guide

This manual describes all aspects of 2280B/2285B installation in a data logging system. The System Guide serves as a complete course in defining the user's data logging functions, identifying system requirements, making the necessary hardware connections, and verifying correct operation. An inexperienced user may need all this information to get the Data Logger up and running. A user who is already familiar with data logging may only need to refer to this information occasionally. In either case, each element of the installation process is easily accessible and fully referenced.

2280 Series Service Manual

The Service manual, which is primarily a maintenance guide to the 2280 Series Data Loggers, covers general maintenance, cleaning, performance testing, calibration, and board-level troubleshooting procedures. The Service Manual also includes theory of operation, parts lists and schematic diagrams for mainframe and option assemblies.

NOTATION CONVENTIONS

- Reference to the Instrument

  Generally, the instrument is referred to as the "2280 Series Data Logger." The terms "2280" or "Data Logger" are also frequently used for brevity. These terms are all-encompassing, referring to the 2280B, 2285B, and 2280A. Differences among these three models are defined in the Appendices to this manual.

- Printed Circuit Board Assemblies

  The notation "PCA" (printed circuit assembly) is used when referring to printed circuit board assemblies.

- Logic Polarity of Signals

  Throughout the theory of operation sections of the Service Manual, logic signals whose names are followed by "(L)" are asserted or active low. The same signal also appears as SIGNAL(L) on the schematic. When a signal followed by "(H)" has no parenthetical postscript, it is active or asserted high.

- Address Notations

  Memory addresses in hexadecimal and address ranges, where specified, are inclusive. That is, address range 0000 to 2000 includes addresses 0000 and 2000.

- Keystroke Notations

  The Data Logger uses literal notation for keyboard entries. Therefore, programming examples found in this manual are presented exactly as they should be entered from the keyboard.

  Some other notation conventions used to identify and differentiate keyboard entries are:

  (xxx) Requests a required input of your choice. For example, "NOT (operand)" inverts the logical value of the operand in parentheses and requires you to specify the operand.

  XXX Here, the name of the input should be typed exactly as shown. For example, "TIME" requires that you enter the literal word "TIME" into the keyboard.

SECTION 2

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DESCRIPTION

The data logger functions as a programmable electronic notebook, that takes and records measurements in a wide variety of ways. The data logger is operated and programmed through the front panel keys or through an optional interface from a remote host device. Programming is prompted in English and menu-driven, so that a special programming language is not required. The front panel of the data logger contains operating and programming keys, a 40-character alphanumeric display, and a 40-column thermal printer. A cartridge tape drive unit, Option 2280A-214, is available.

One data logger mainframe can service up to 100 analog channels or 120 digital data channels. System channel capacity can be increased to 1500 by adding Model 2281A Extender Chassis to house additional I/O options.

In addition to the data acquisition ability, the data logger has extensive computational power that allows it to perform complex data reductions. Combinations of addition, subtraction, multiplication, and division functions may be used to convert raw data to relevant values. Option 2280A-211 Advanced Math Processor provides square root, exponentiation, trigonometric functions, standard deviation, logarithms, and Boolean and other logical operator functions. The Advanced Math Processor also enhances data throughput by assisting with operations that the data logger Controller normally handles alone.

Front Panel Controls

Figure 2-1 shows the operating and programming keys located on the data logger front panel. The programming keys are covered by a snap-on cover with a thumb latch on the right edge. These keys are called programming keys because they are only used for programming functions. The operating keys are located to the right of the programming keys and can be used when the keyboard cover is in place. For programming and operating instructions, see the 2280 Series System Guide and the 2280 Series User Guide.

Rear Panel Components and Connectors

The components and connectors located on the rear panel of the Data Logger are shown in Figure 2-2. Six horizontal slots are available for installing scanners, A/D Converters, and other measurement and control options. To the left of the horizontal option slots are two vertical slots, Port A (closest to the horizontal slots) and Port B (shown in Figure 2-2 with the IEEE-488 Interface Option installed). Ports A and B accept interface options that allow the data logger to communicate with peripheral devices. Port A can be used to output data or to program and operate the data logger from a terminal or computer host device, but Port B can only be used to output data.

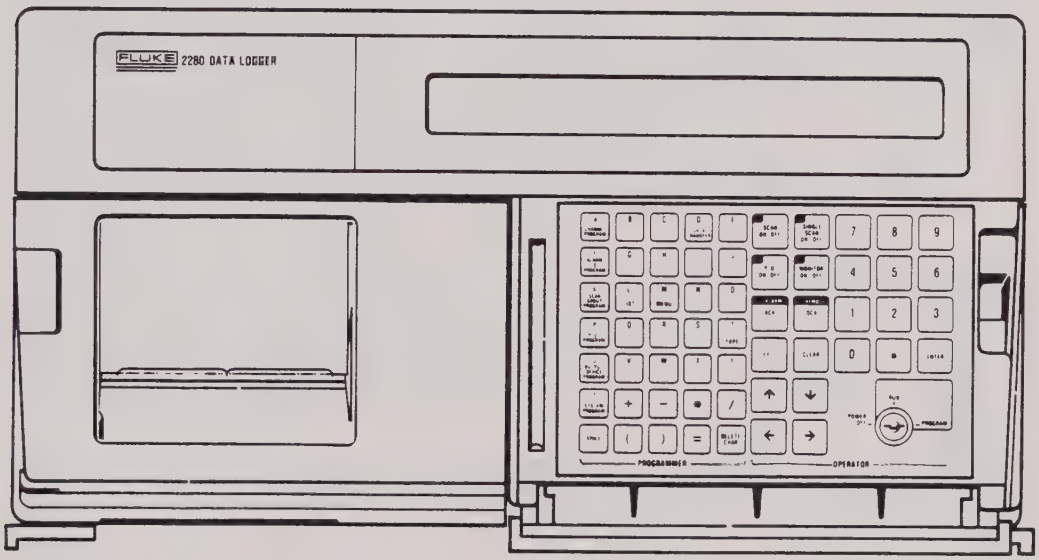

Figure 2-1. 2280B Front Panel

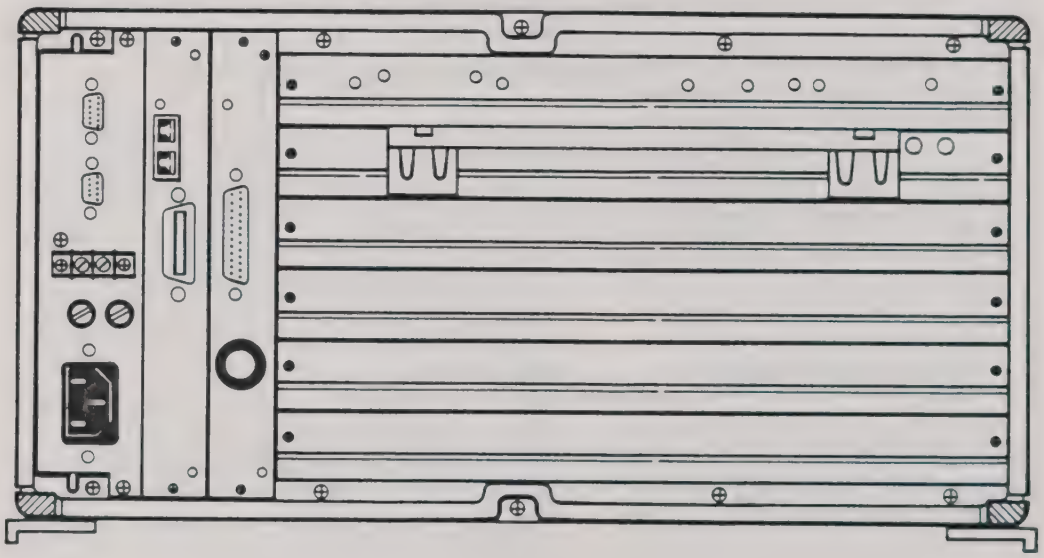

Figure 2-2. 2280B Rear Panel

Fuses, power inputs, and two connectors are mounted in the main panel on the extreme left side of the data logger as viewed from the rear. The uppermost connector, J23, is the Extender Chassis Connector. Just below J23 is the Hardware Trigger and Master Alarm Output Connector, J25. Two screw-terminal connections and a ground terminal are provided in the center of the rear panel for dc power input and earth ground connection. Two input fuses are located just below the dc input terminals, and the ac line input connector is located at the bottom of the rear panel.

Power Requirements

The data logger operates on any of four ac line voltage ranges: 100V ac, 120V ac, 200V ac, or 240V ac. Line voltage variance of 10% is acceptable on all input voltage ranges except the 240V range. In the 240V ac range, maximum input voltage is limited to 250V ac. Line frequency for all ac voltage inputs may be either 50 Hz or 60 Hz. The data logger also operates on 12V dc power input. The data logger automatically switches to dc voltage operation if the ac line input is interrupted while a dc source is connected to the rear panel terminals. Both the ac and dc power inputs are fuse protected. Fuse F1 protects the ac input circuit and fuse F2 protects the dc input circuit. Refer to the rear panel decal or Table 4-1 for correct fuse ratings for each voltage range. See Section 4 for fuse replacement procedure.

Two switches, located on the edge of the transformer assembly closest to the front panel, are used to select any one of the four possible ac input voltage ranges. Refer to the line voltage selection procedure in Section 4 when setting the line voltage switches.

REQUIRED TEST EQUIPMENT

Test equipment required for all data logger performance tests and calibration procedures is summarized in Table 2-1. Equipment required for each test is also listed with the procedure in the applicable section or subsection.

Table 2-1. Summary of Required Test Equipment

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
DC Calibrator	+31.3 mV +/- 20 uV +2.048V +/- 50 uV -2.048V +/- 2 uV of +2.048 500 mV +/- 20 uV 6.2V +/- 155 uV 6.8V +/- 0.1V 5.0V +/- 100 uV 7.9V +/- 200 uV 63V +/- 800 uV (used only for one optional test) 1.008V +/- 40 uV	Fluke Model 343
100:1 Divider	+/- 0.005%	Fluke Accessory Y2022
DC Voltmeter	+10V +/- 0.06V 50.0 mV +/- 0.001 mV 500.0 mV +/- 0.005 mV	Fluke Model 8502A
Resistor	1 kilohm +/- 5%, 1/2 W	Fluke Part # 108597
Resistor	10 kilohm +/- 5%, 1/2 W	Fluke Part # 109165
Resistor	8 ohm +/- 0.25%, 1/2 W	Fluke Part # 641449
Room Temperature Oil or Water Bath	.....	.....
Mercury Thermometer	0.02 oC resolution	Princo ASTM-56C
Calibration Extender/Fixture	.....	Fluke Accessory Y2056 (no substitute)
Digital Extender Assembly	.....	2400A-4021 Fluke Part # 486910

OPTIONS, ACCESSORIES, AND OTHER RELATED EQUIPMENT

All options available for the 2280 Series data loggers at the time of this printing are listed in Table 2-2. All Accessories are listed in Table 2-3. Table 2-4 lists other related equipment for use with the data logger. Refer to Sections 8, 9, and 10 of this manual for further information on data logger options.

Table 2-2. Data Logger Options

OPTION NUMBER	NAME	FUNCTION
2280A-160	AC Voltage Input Connector	AC to dc conversion, voltage division, screw-terminal connections (for use with Option 2280A-162).
2280A-161	High Performance A/D Converter	Analog-to-digital converter, dual slope integration.
2280A-162	Thermocouple/DC Volts Scanner	Scans 20 channels, 1 microvolt, 3 poles per channel (for use with Options 2280A-160, 2280A-171, 2280A-175, or 2280A-176).
2280B-163	RTD/Resistance Scanner	Scans 20 channels, 4 poles per channel, 1 pole per decade, precision current source excitation (for use with Option 2280B-177). Cannot be used in the 2280A.
2280A-164	Transducer Excitation	Contains one precision 2V or 4V source and five precision 1 mA current sources (for use with Option 2280A-174 and 2280A-162).
2280B-167	Counter/Totalizer	Measures frequency or counts events on six channels. Cannot be used in the 2280A or 2285B.
2280A-168	Digital I/O Assembly	Provides 20 single-bit channels for Alarm or Status input or output or for bcd or binary input (for use with Options 2280A-169 or 2280A-179).
2280A-169	Status Output Connector	Provides 20 screw-terminal connections for external digital devices (for use with Option 2280A-168).

Table 2-2. Data Logger Options, cont.

OPTION NUMBER	NAME	FUNCTION
2280B-170	Analog Output	Four-channel current (4 to 20 mA) or voltage (0V to 10V or -5V to +5V) outputs, 12 bit. Cannot be used in 2280A or 2285B.
2280A-171	Current Input Connector	Provides 20 current input connections each with a shunt resistor (for use with Option 2280A-162).
2280A-174	Transducer Excitation Connector	Provides screw-terminal connections for voltage and current sources (for use with Option 2280A-164).
2280A-175	Isothermal Input Connector	Provides screw-terminal connections for 20 thermocouple input channels (for use with Option 2280A-162).
2280A-176	Voltage Input Connector	Provides screw-terminal connections for 20 voltage input scanner channels (for use with Option 2280A-162).
2280B-177	RTD/Resistance Input Connector	Provides screw-terminal connections for 20 channels of 3- or 4-wire RTD or resistance measurement (for use with Option 2280B-163). Cannot be used in 2280A.
2280A-179	Digital/Status Input Connector	Provides screw-terminal connections for binary or status digital input signals (for use with Option 2280A-168).
2280A-211	Advanced Math Processor	Provides complex mathematical computation capability for the data logger.
2280A-214	DC-100 Cartridge Tape Drive	Cartridge tape program and data storage and retrieval option.
2280A-341	RS-232-C Interface	Provides full duplex serial data communication with selectable baud rate and parity.

Table 2-2. Data Logger Options, cont.

OPTION NUMBER	NAME	FUNCTION
2280A-342	IEEE-488 Interface	Provides parallel communication with external devices compatible with the IEEE-488 standard.
2280B-MAN	2280 Series Manual Set	Includes all three manuals: 2280 Series User Guide, 2280 Series System Guide, and 2280 Series Service Manual
2280A-UGK	2280A Upgrade Kit	Fluke Service Center provides and installs kit to upgrade a 2280A to a 2280B (see Appendix B in the Service Manual for differences between 2280A and 2280B).

Table 2-3. Accessories for the 2280B

ACCESSORY	DESCRIPTION
Y2042 DC-100A Cartridges	Package of five tape cartridges for use with Option 2280A-214 DC-100 Cartridge Tape Drive.
Y2044 Rack Slide Kit	Slide kit for mounting the Data Logger or the 2281A Extender Chassis in a 19-inch-wide, 24-inch-deep equipment rack.
Y2045 Rack Mount Kit	Mounting flanges for installing the data logger or the 2281A Extender Chassis in a 19-inch-wide. 24-inch-deep equipment rack.
Y2046 Thermal Printer Paper (10-pack)	Paper for the data logger Printer. Each roll contains 4000 lines.
Y2047 Extender Chassis Multi-Connector	Interconnection unit for connecting the multiple 2281A Extender Chassis to the data logger.
Y2050 Data Logger Programming Forms	Tablets of preprinted forms to aid in developing data logger programs.
Fluke Part # 486910 Digital Extender PCA	Allows the vertical digital boards to be extended out from the mainframe for troubleshooting.
Y2056 Calibration Extender/Fixture	Allows the horizontal circuit boards to be extended out from the mainframe for calibration or troubleshooting.

Table 2-4. Other Related Equipment For Use With the 2280B

ITEM	DESCRIPTION
Fluke Model 2281A Extender Chassis	Allows adding extra data logger channels by housing additional option assemblies.
Fluke Option 2281A-402 Extender Chassis Cable	Cable to connect a 2280 Series Data Logger to a 2281A Extender Chassis or to link two 2281A Extender Chassis. Ordered in lengths from 1 to 1000 meters.
Fluke Option 2281A-403 Connectors for Extender Chassis Cable	Connectors for each end of a 2281A-402 Cable. Installed onto the cable at the factory.
Fluke Option 2281A-431 Power Supply for the 2281A Extender Chassis	Optional power supply for the 2281A Extender Chassis. Used for remote operation in some cases.
Fluke Accessories Y8021, Y8022, and Y8023 IEEE-488-Compatible Cables	Used to connect the data logger (with Option 2280A-342 installed) to IEEE-488-compatible devices.
Fluke Accessories Y1707, Y1708, and Y1709 RS-232-C Cables	Used to connect the data logger (with Option 2280A-341 installed) to a device with an RS-232-C port.

SHIPPING INFORMATION

The data logger mainframe is packaged with foam end caps in a cardboard shipping container. This container also contains a smaller box holding the manual set, the line cord, a tablet of programming forms, extra rolls of paper, the keyboard and printer doors, the connector and housing for the trigger input, and the master alarm output connector.

Upon receipt of the instrument, inspect the shipping container for any possible shipping damage. Special instructions for inspection and claims are included on the shipping container.

If it is necessary to reship the instrument, use the original container. If the original container is not available, a new one can be obtained from the John Fluke Manufacturing Co., Inc. upon request.

SERVICE INFORMATION

The data logger is warranted for a period of one year upon delivery to the original purchaser. The warranty is located on the back of the title page in the front of this manual.

Factory authorized calibration and service for each Fluke product is available at various locations worldwide. A complete list of these service centers is given in Appendix A located in Section 11 of this manual. If requested, an estimate will be provided to the customer before any work is begun on an instrument whose warranty period has expired. Maintenance plans are available to maintain the data logger at your site, to supplement the normal warranty period, or to do both. For specific information, contact your nearest Fluke Technical Service Center or Sales Representative.

SECTION 3

THEORY OF OPERATION

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INTRODUCTION

This section of the Service Manual contains the theory of operation for 2280 Series data logger standard mainframe assemblies. Theory of operation explanations are supported by block diagrams, simplified schematics, and tables where necessary to clarify concepts. All data logger standard assembly schematics are on fold-out pages in Section 7, which you can refer to while reading the text by folding them open and out away from the manual.

This section of the manual deals only with the theory of operation. Installation and configuration instructions for the data logger are located in the 2280 Series System Guide. Operating and programming instructions and reference material are located in the 2280 Series User Guide.

Many options are available to provide the data logger with many measurement, control, logging, and interface functions. Theory of operation discussions and schematics for data logger options are included in individual option subsections of Sections 8, 9, and 10.

OVERALL FUNCTIONAL DESCRIPTION

Figure 3-1 is a simplified overall block diagram that shows the interrelation of the major parts of the Data Logger. Referring to it while reading the overall functional description will help clarify how the data logger assemblies work together.

At the heart of the data logger are the controller and memory assemblies. The controller is a Z-80-microprocessor-based CPU that commands all operations and functions of the Data Logger. The controller shares the use of the memory assembly with the optional Advanced Math assembly. The controller, memory, and advanced math assemblies are linked by the shared memory bus, which consists of an address bus and a data bus for the controller, and an address bus and a data bus for the Advanced Math option.

The data logger controller also communicates with other assemblies using the Serial Link and the PIO Bus. The busses are described in the next two paragraphs, and their communication protocols are described in greater detail under the heading, "Details of Interprocessor Communication," following the block diagram analysis.

The serial link connects the 2280 Series mainframe CPU assembly with all measurement and control options, which include the a/d converter, digital I/O options, and analog I/O options in the Data Logger system. To communicate with all option assemblies, the serial link circuitry (on the power supply assembly) translates TTL-level signals from the controller into RS-422 signals. The RS-422 signals are sent and received through two pairs of conductors. Through one pair, the controller transmits while all options listen. Through the other pair, an option selected by the controller can transmit only to the controller.

The PIO bus is an 8-bit parallel bus that carries messages between the controller assembly and the logging and interface assemblies. The logging and interface assemblies are the Display/Keyboard assembly, the Printer assembly, the DC-100 Cartridge Tape option, the IEEE-488 Interface option, and the RS-232-C Interface option.

Operating voltages from the power supply are delivered to the controller and all other blocks on the serial link over the serial link. A separate power supply bus delivers power to all blocks linked to the device bus.

The following summary breaks the Data Logger down into its seven major circuit blocks and briefly describes the function of each. The detailed circuit analysis explains in detail how each of the the seven major blocks operates. The seven major blocks in the Data Logger are discussed in the following paragraphs in the same order they are presented in the detailed circuit analysis.

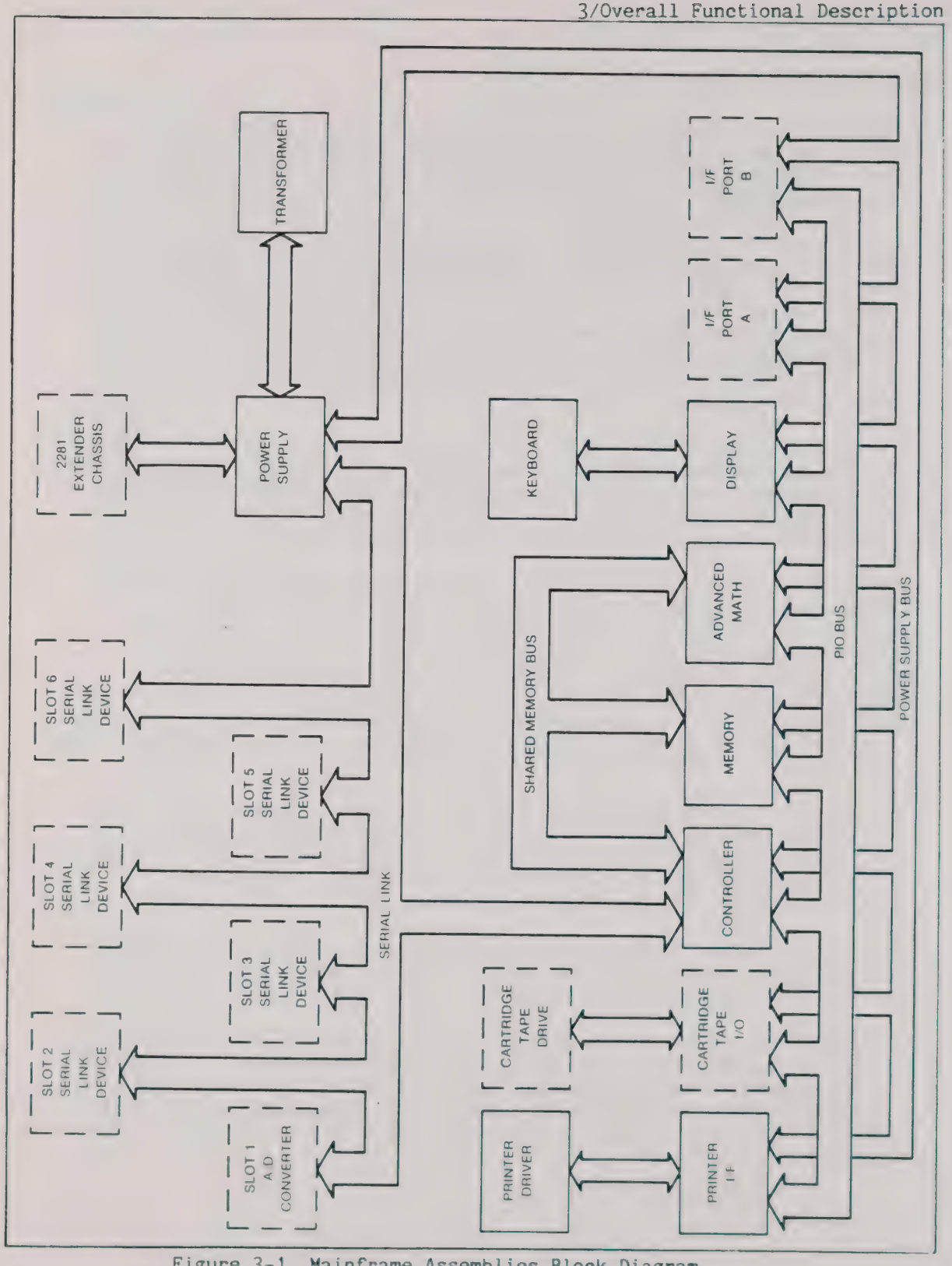


Figure 3-1. Mainframe Assemblies Block Diagram

- Motherboard

  The motherboard provides interconnection between the various data logger assemblies through the PIO bus and the connectors mounted on the motherboard. Power is also distributed to all assemblies through the motherboard.

- Transformer

  Both ac and dc power, after entering the data logger through rear panel terminals, passes through the transformer assembly. Ac power is rectified and filtered to provide an unregulated +dc voltage to the power supply assembly. Dc power, which can be used as primary or backup power for the instrument, is switched to the power supply assembly when needed. Additional circuitry on this assembly trickle charges the 12V battery connected to the rear dc input terminals.

- Power Supply

  The power supply converts a non-regulated dc input voltage, called +dc on the schematic and in the circuit analysis, into several regulated and protected output voltages. The power supply input voltage (+dc) is obtained from the transformer assembly and ranges from 10 to 22 volts.

  Two of the outputs provide current-limited, regulated dc voltages of +5 volts and +24 volts. The power supply also outputs -12 volts and a voltage called +5B that varies between +3 and +5 volts for charging the memory-hold battery. All outputs are supplied to the Data Logger mainframe through the motherboard, while +24 volts is supplied to extender chassis through a serial link connector and cable. The power supply also contains circuitry that generates three TTL-logic reset signals, alarm, and trigger signals. Communication circuitry on the power supply assembly translates TTL-level signals from the controller into RS-422 signals for communication with all devices on the serial link.

- Controller

  Together with the memory assembly, the controller assembly forms the heart of the data logger. The controller is centered around a Z-80 microprocessor that coordinates communication with, and control of, all parts of the Data Logger. The controller connects to the serial link, the PIO bus, and the shared memory bus for communication with every part of the Data Logger. A non-volatile (battery-powered) real time clock on the controller keeps track of date and time while the instrument is turned off.

- Memory

  The memory assembly contains most of the ROM accessed solely by the controller, and all the RAM shared by the Advanced Math option and controller. The ROM and RAM portions of the memory are separate, allowing the controller to access the ROM at the same time the Advanced Math option accesses shared RAM. Simultaneous access of

shared RAM by both the Advanced Math option and the controller assembly is prevented by a bus-arbitration circuit which places one of the two simultaneous requesters in an idle state. RAM components are powered by the +5V battery supply at all times to ensure that the RAM contents are retained while the instrument is off.

The memory assembly is linked to the controller by the controller address bus and the controller data bus. The Advanced Math option communicates with the memory through the math address bus and the math data bus.

- Display

The Display assembly performs four functions. They are, communicating with the controller, controlling the dots of the vacuum Fluorescent display, controlling the buzzer, and scanning the keyboard for keystroke entries. The Display assembly's microprocessor communicates with the controller over the PIO bus.

- Printer

The printer is a 40-column thermal printer that is controlled by circuitry on two circuit boards: the printer interface board and the printer driver board. The printer interface board, which plugs into the motherboard, contains the circuitry necessary to interface with the controller over the PIO bus and to drive the printer motors. The printer driver board, which connects to both the thermal printer and the printer interface board, contains the circuitry that drives the printheads.

DETAILED DESCRIPTION

Motherboard

The Motherboard provides interconnection between the various data logger assemblies. Printed circuit board edge card connectors are mounted on both sides of the motherboard. Each connector on the side of the motherboard facing the front of the instrument accepts only one type of assembly. Each assembly that is installed in the front portion of the instrument has a dedicated position for installation. The horizontally positioned connectors on the rear side of the motherboard accept all serial link and scanner options. Connectors J2[A:F] provide serial link communication signals and 24V dc power. Connectors J1[A:F] allow serial link options (A/D Converters) to interface to other options (Scanners) installed below them.

Transformer

Both ac and dc power, after entering the data logger through rear panel terminals, passes through the Transformer Assembly. Ac power is reduced in voltage by transformer T1, rectified through diodes CR1 and CR2, and filtered using capacitors C1, C2, and C3 to provide an unregulated dc voltage to the Power Supply Assembly. Dc power, which can be used as primary or backup power for the instrument, is switched to the Power Supply Assembly when needed. CR3 provides this switching when the ac input power is disconnected. Circuit components Q1, CR6, CR7, R7, and R8 provide a trickle-charge current to the battery when ac input power is connected and the instrument is turned on.

Power Supply

The Power Supply Assembly has five separate circuit blocks as illustrated in Figure 3-2. The main functional blocks are the +5 and -12 volt supply, the +24 volt supply, the +5B backup circuit, the reset circuitry, and the communication circuitry. Each block is described under a separate heading.

+5 VOLT AND -12 VOLT SUPPLY

The +5 volt and -12 volt power supply is a pulse-width modulated (PWM) regulator and converter (refer to the simplified schematic, Figure 3-3). The supply converts the +dc voltage received from the transformer assembly into +5 volts dc and -12 volts dc. The +5 volt portion is a step-down, or buck regulator, while the -12 volt portion is a flyback pre-regulator that requires additional output regulation. The PWM section runs at a frequency of 50 kHz and is synchronized with the +24 volt supply PWM regulator. The +5 volt output remains within 4 percent of 5.1 volts, and is current-limited to 5 amperes.

When the signal START5 is asserted, or released to the high state, the PWM slow-starts until the +5 volt output is within tolerance. De-asserting START5 immediately shuts off the switching supply.

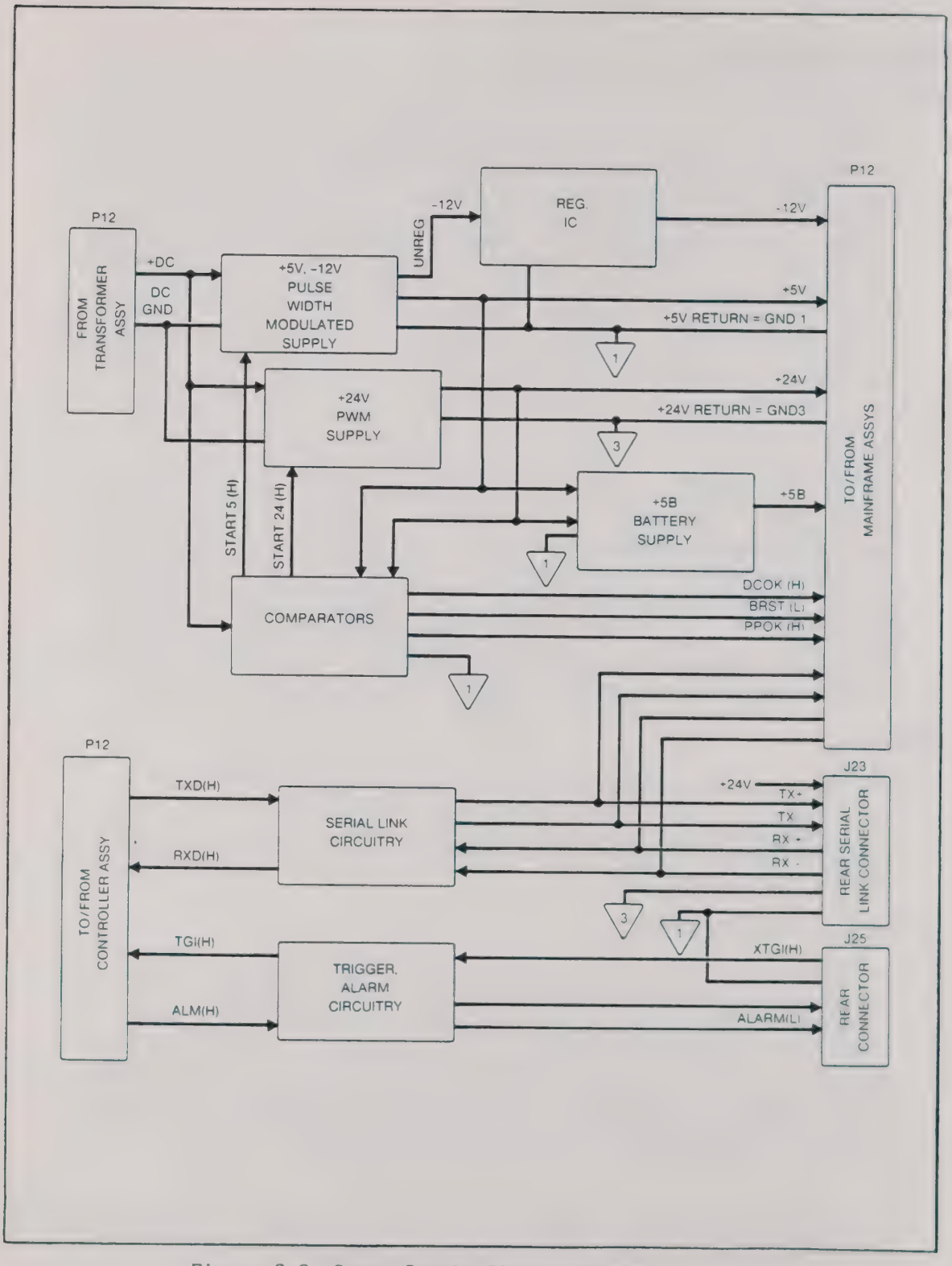


Figure 3-2. Power Supply Block Diagram

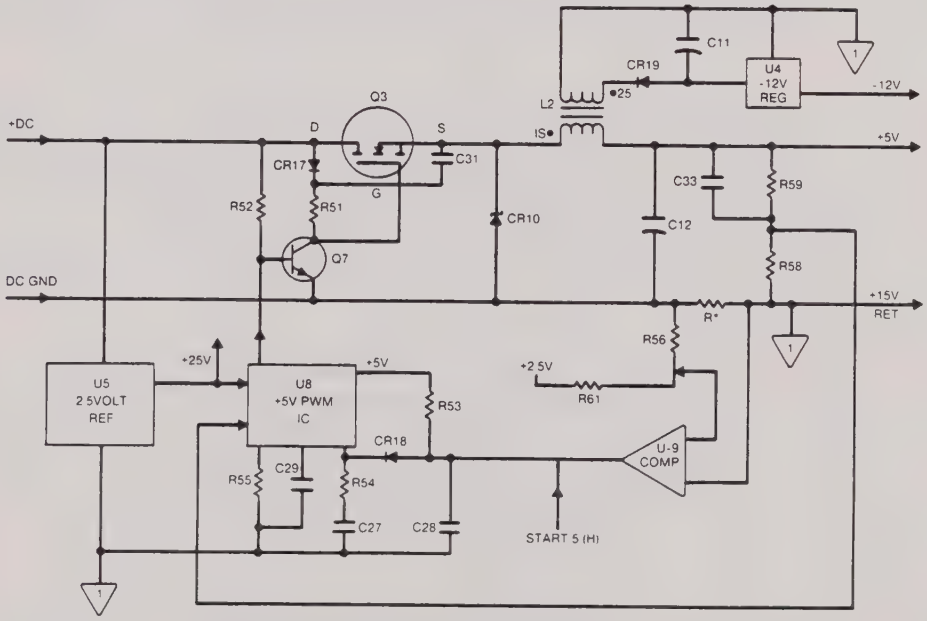


Figure 3-3. +5 and -12 Volt Power Supply Simplified Schematic

Internally, the +5 and -12 volt supply is regulated as follows. The PWM IC (U8) senses the +5 volt output through a resistive divider made up of R58 and R59, and compares the voltage to a 2.5 volt reference voltage generated by U5. The PWM IC adjusts the duty cycle of the total period set by resistor R55 and capacitor C29 by turning transistor Q3 on and off to keep the average output voltage at a nominal 5.1 volts. Capacitor C29 also limits the maximum duty cycle to 95%, while C33, R54, and C27 tailor the closed-loop system frequency response for maximum bandwidth with stability.

When Q3 is on, current ramps up through inductor L2, to increase the voltage across C12, store energy in both components, and supply power to the load. When Q3 is shut off by the PWM IC, current ramps down through Schottky diode CR10 and inductor L2, as energy is drawn from L2 to supply C12 and the load for the remainder of the 50 kHz period. This also forward biases diode CR10, clamping the cathode at approximately -0.4 volts. Some timing relationships and general voltage levels for both the +5 volt and +24 volt supplies are shown in the timing diagram, Figure 3-4.

The gate drive for MOSFET transistor Q3 is a bootstrap circuit comprised of Q7, CR17, R51, R52, and C31. To turn Q3 off, Q7 is turned on by the PWM, pulling the gate of Q3 near ground, and reducing the gate-to-source voltage below its threshold value. At the same time, charge is stored in C31. To turn Q3 on, Q7 is turned off and the charge stored in C31 is dumped into the gate of Q3. This voltage charges up the gate-to-source capacitance, raising the gate-to-source voltage above it's threshold level, thereby turning Q3 on.

A current-limit circuit limits the power available from the +5 volt supply. The voltage developed from the current flowing in the PCA trace labeled R*A in the schematic is compared to a calibrated voltage set up by a resistive divider, R56 and R61, and the 2.5-volt reference. When the sensed voltage exceeds the calibrated value, comparator U9 pulls enough charge out of C28 to limit the PWM duty cycle, thereby reducing the output voltage and limiting the output current.

Slow start circuitry made up of R53, C28, and CR18 brings the PWM duty cycle up slowly from zero on start-up. Current flowing into capacitor C28 develops a rising voltage to which the PWM duty cycle control voltage is clamped.

The -12 volt supply also receives power from L2. When transistor Q3 is off, the 1S end of L2 is clamped at -0.4 volt, and the 5.4-volt drop that appears across winding 1 is reflected through the turns ratio to winding 2. This forward-biases CR19, transferring energy from L2 into C11 and the -12 volt load. When transistor Q3 is on, CR19 is reversed-biased, and an active voltage regulator, U4, runs off of the charge stored in C11 to deliver the -12 volt output.

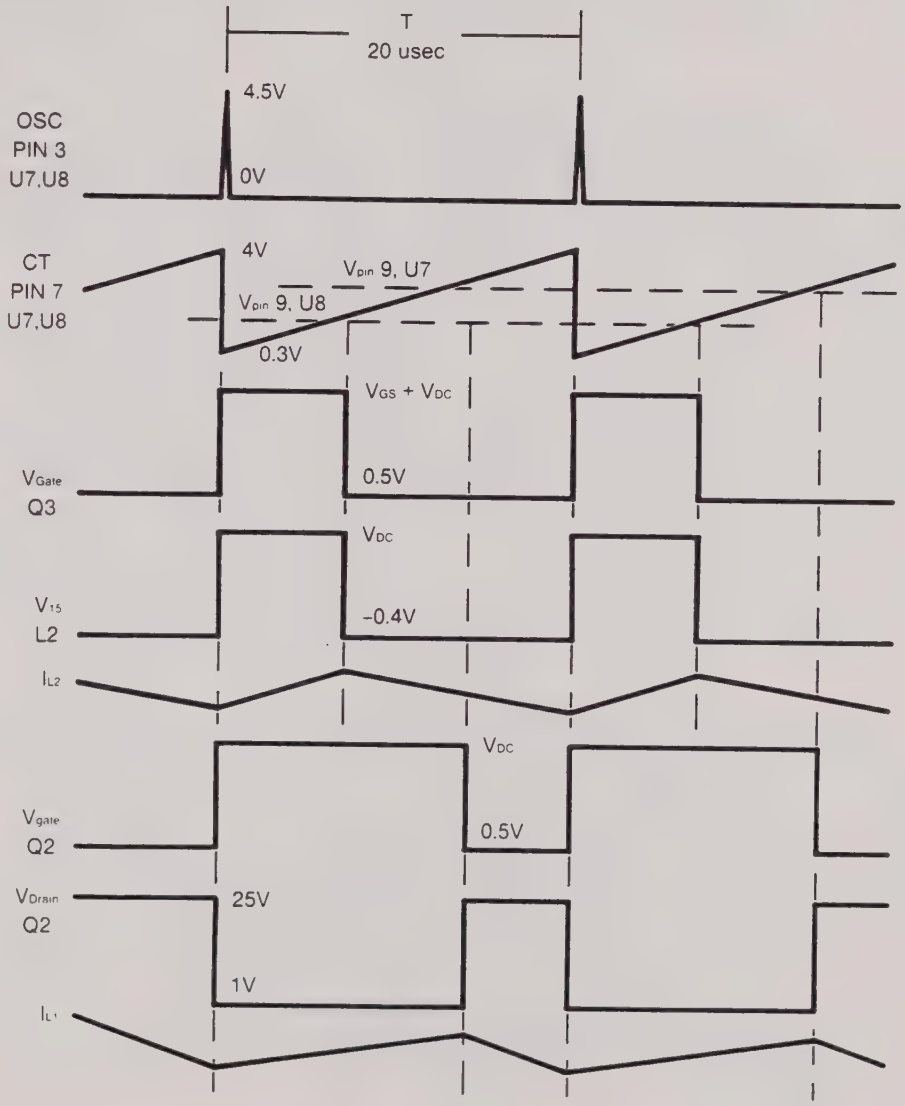


Figure 3-4. Power Supply Timing Diagram

+24 VOLT SUPPLY

The +24 volt supply converts +dc into +24 volts, working as a pulse-width modulated step-up regulator. The supply is synchronized with the 50 kHz frequency of the +5 volt PWM. The +24 volt output remains within 4 percent of 23.7 volts, while the +dc input current is limited to 8 to 9 amperes. Figure 3-5 is a simplified schematic of the +24 volt supply.

The +24 volt PWM IC, U7, is synchronized with the +5 volt PWM, U8, by sharing the oscillator (OSC) and ramp (CT) signals. The duty cycle of MOSFET transistor Q2 is controlled by U7 through the gate drive circuitry centered around Q4, Q5, and Q6. Turning Q2 on causes current to ramp up through L1 and store energy in the inductor. During this time, the load current is supplied by C9. When Q2 is shut off, current flows through CR11 to store energy in C9 and supply the load.

A parallel feedback path determines the PWM duty cycle control voltage so that 60 Hz output ripple can be minimized, while maintaining adequate loop stability. The +24 volt output is sensed through a resistive divider made up of R49 and R50, and is compared to a 2.5-volt reference to determine the dc operating point. Loop stability with high dc gain is established by U10, R34, C32, and R35, the dc feedback amplifier circuit. Any 60 Hz ac ripple that appears at the output of the supply is fed back through the bandpass filter formed by U10, R65, R66, C6, C7, and R23. The outputs of both of these feedback amplifiers are summed in the non-inverting summing amplifier formed by R41, R42, R43, R46, and the amplifier internal to U7. Two additional capacitors (C25 and C20) serve to keep the supply stable under rated conditions.

Over-voltage protection is provided by zener diode VR2, resistors R48, R64, and the shut-down circuit internal to U7. Over-current protection is provided by a comparator circuit that limits the current flowing through Q2, L2, and hence into the +24 volt supply. The protection circuit compares the voltage drop across R*B, a PCA trace, to the voltage set up by R62, R57, and U3 that tracks the +24 volt ground. A comparator (U9) pulls enough charge out of C21 to limit the duty cycle, thereby limiting the input current to the +24 volt supply. During power-up and when coming out of current limit, the slow-start circuit formed by R45, C21, and CR16 controls the pulse width to maintain a slow increase in duty cycle. Since the feedback loop is open at this time, the dc feedback amplifier output is clamped by two diodes in the dc amplifier local feedback path, CR27 and CR28.

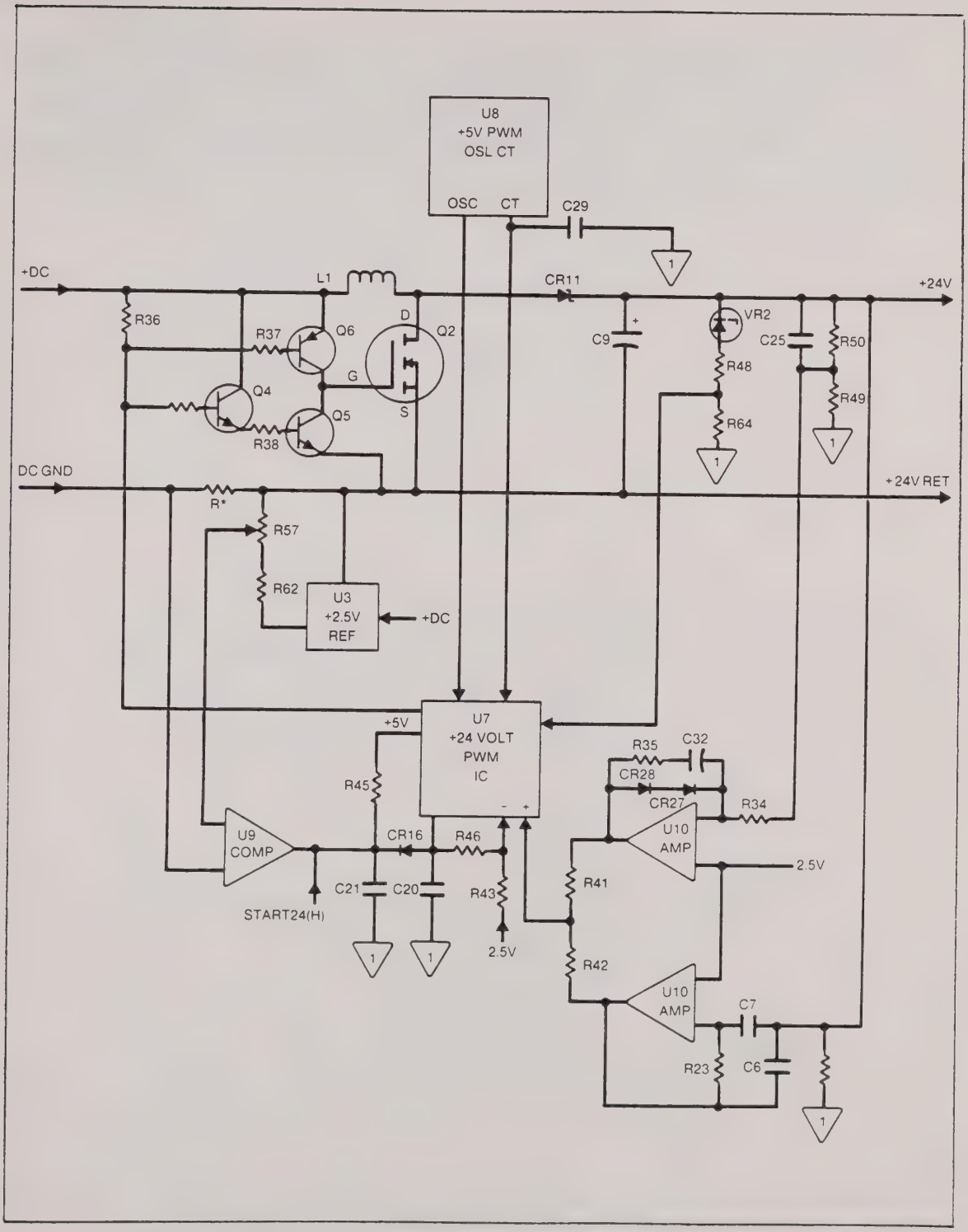


Figure 3-5. +24 Volt Supply Simplified Schematic

+5B BACKUP CIRCUIT

The memory back-up supply circuit is centered around a rechargeable nickel-cadmium battery, BT1 as shown in the simplified schematic, Figure 3-6. When the power supplies are running, the battery is charged from the +24 volt output through R60, while the +5B output is taken from the +5 volt supply through Schottky diode CR22. When the power supplies switch off, the battery smoothly couples power to the +5B output through Schottky diode CR26. The +5B output is protected during an open battery condition by zener diode VR5.

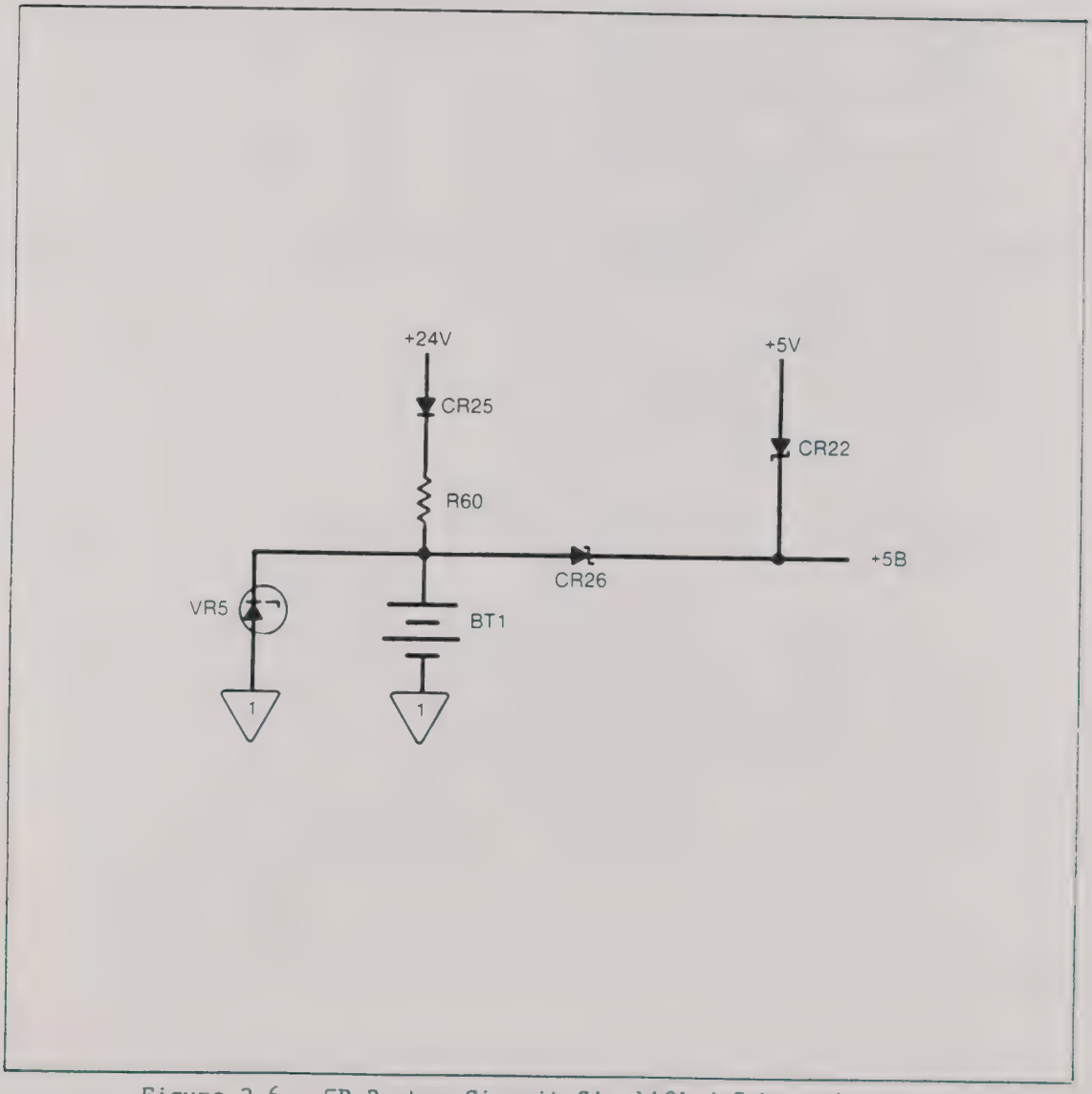


Figure 3-6. +5B Backup Circuit Simplified Schematic

RESET CIRCUITRY

The reset circuitry section of the power supply starts and stops the +5 volt, -12 volt, and +24 volt supplies, and controls three TTL-level logic reset lines. Figure 3-7 is a simplified schematic of the reset circuitry.

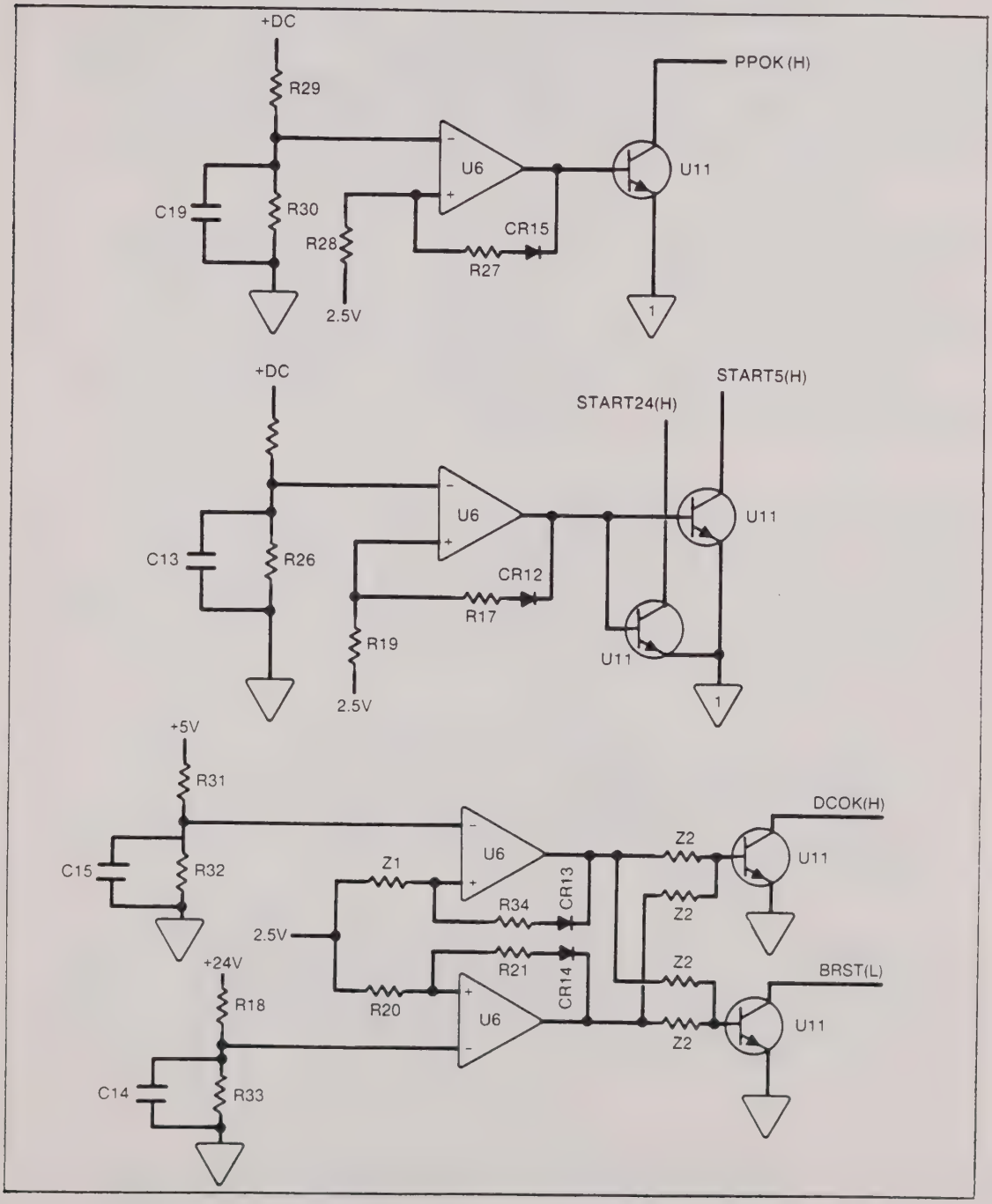


Figure 3-7. Reset Circuitry Simplified Schematic

One set of comparators watches the +dc voltage from the transformer assembly. If +dc is greater than 10 volts, START5 and START24 are both asserted to allow startup. After startup, START5 and START24 are left asserted as long as +dc remains greater than 8.3 volts. The +dc voltage is also examined to determine the state of the mainframe logic signal PPOK (Primary Power Okay). Signal PPOK is asserted when +dc exceeds +10 volts, and it remains asserted as long as +dc remains above 9 volts.

The other two comparators generate the mainframe TTL-logic reset signals DCOK (dc supplies okay) and BRST (L) (Bus Reset). As long as the +5 volt output remains above 4.8 volts and the +24 volt output remains above 17.8 volts, DCOK remains asserted and BRST (L) remains de-asserted. If either the +5 volt output or the +24 volt output fall out of tolerance, DCOK is de-asserted, and BRST (L) is asserted.

The reset circuitry is centered around U6, U11, and several resistors, capacitors, and diodes. Signal PPOK is generated by a comparator circuit that drives an open-collector transistor in U11. Here, R29 and R30 divide +dc to a level that can be compared to the 2.5-volt reference, C19 filters noise with a minimal time delay, and R27, R28, and CR15 provide necessary hysteresis. Signals START5 and START24 are developed by a second comparator that checks +dc through the R25 and R26 divider. Filtering is provided by C13, and hysteresis is developed by R17, R19, and CR12.

Two comparators with their outputs ANDed together generate logic signals DCOK and BRST(L). If either the +5 volt or +24 volt output falls out of regulation, both logic lines are pulled low through open-collector transistors in U11. Resistors R31 and R32 divide the +5 volt output, and R18 and R33 divide the +24 volt output for comparison with the 2.5 volt reference. Capacitor C15 provides filtering with minimal turn-off delay, while C14 and C15 both provide turn-on delay.

COMMUNICATION CIRCUITRY

Communication circuitry on the power supply circuit board translates TTL-level signals from the controller into RS-422 signals for serial link communication. Other parts of the communication circuitry condition alarm outputs and trigger inputs that are accessible through connectors on the Data Logger rear panel. Figure 3-8 is a simplified schematic of the communication circuitry.

Serial link Transmit Data from the mainframe, TXD, is conditioned by and transmitted from the four drivers of U1, which are resistively coupled in parallel by R3 through R10 to allow a non-fatal driver failure. The two resulting bi-phase output lines, TX+ and TX-, are protected by clamp diodes CR1, CR2, CR3, and CR4, zener VR1, and series resistors R1 and R2.

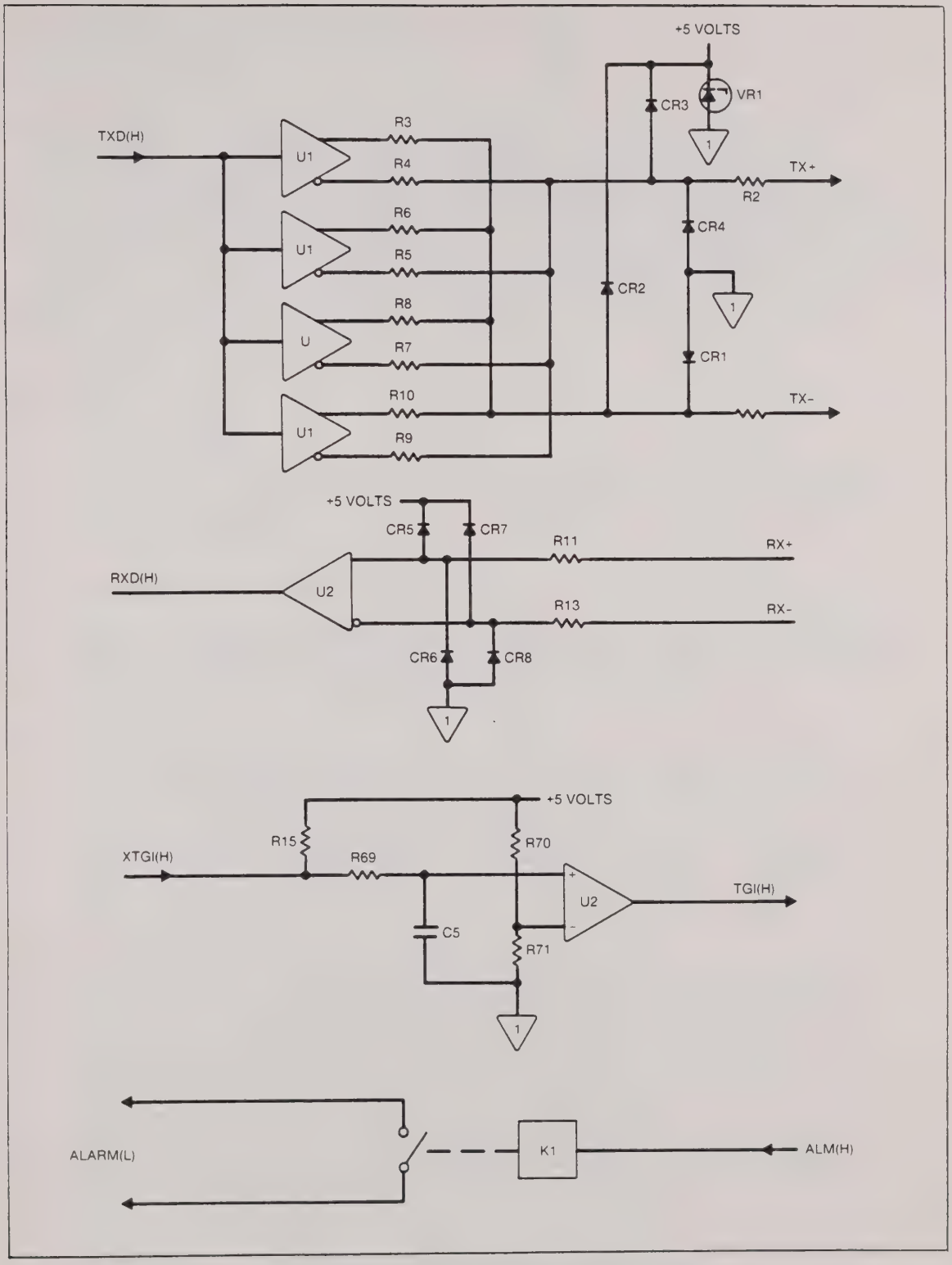


Figure 3-8. Communication Circuitry Simplified Schematic

Serial link receive data is received by U2 after the bi-phase signal lines, RX+, and RX-, are resistively terminated by R11 and R13 and are diode-clamped by CR5, CR6, CR7, and CR8. The receiver IC, U2, then converts the Receive Data into one TTL-level mainframe signal, RXD.

Part of the communication circuitry conditions XTG1, the TTL-level, external, trigger-input signal, into TG1 for the mainframe. Signal XTG1 is first filtered and biased-up by R15, R69, and C5. Operational amplifier U2 then compares XTG1 to the threshold level set by R70 and R71 to determine TG1. Another circuit drives the alarm output relay, K1, from the mainframe logic signal, ALARM.

Controller

FUNCTIONAL DESCRIPTION

The Controller Assembly is the heart of the 2280 Series Data Logger. It contains the instrument's main microprocessor and control logic, a portion of the RAM and ROM memory, a battery power clock, and a watchdog timer circuit. The Controller Assembly also contains the circuitry required to implement the PIO Bus which is used to communicate with logging and interface devices, and an asynchronous serial communication IC used to communicate with measurement and control devices over the Serial Link. All functions of the Controller Assembly are accomplished by the nine major blocks shown in Figure 3-9. A brief description of each block follows.

BLOCK DIAGRAM ANALYSIS

- Microprocessor

  A 4-MHz Z-80 microprocessor is used in the data logger. The program for the processor is contained in ROMs residing on this assembly and the Memory Assembly.

- Oscillator and Control Logic

  A 4-MHz clock is provided for the Z-80. Several logic components are used to decode the addresses coming from the microprocessor and steer enabling signals to memory and input and output devices.

- Memory

  One 8K-byte ROM and two 2K-byte RAM"s on this assembly provide part of the ROM and RAM used by the microprocessor. This part of the RAM is volatile--that is, not powered by the internal battery. Therefore, that part of RAM is only used as temporary storage for variables required by the program the microprocessor is executing.

- PIO Bus Communication

  The PIO Bus is an eight bit parallel communication interface through which the Controller Assembly communicates with all logging and interface devices. The logging and interface devices are the internal printer, display and keyboard, DC100 cartridge tape option, and the Port A and Port B communication options which can be either IEEE-488 or RS-232. This interface is implemented with a Z-80-PIO integrated circuit. The PIO Bus consists of eight signals used for the bidirectional exchange of data, five to address the logging and interface devices, two that identify the type of transaction to be performed, and five to provide handshaking and synchronization.

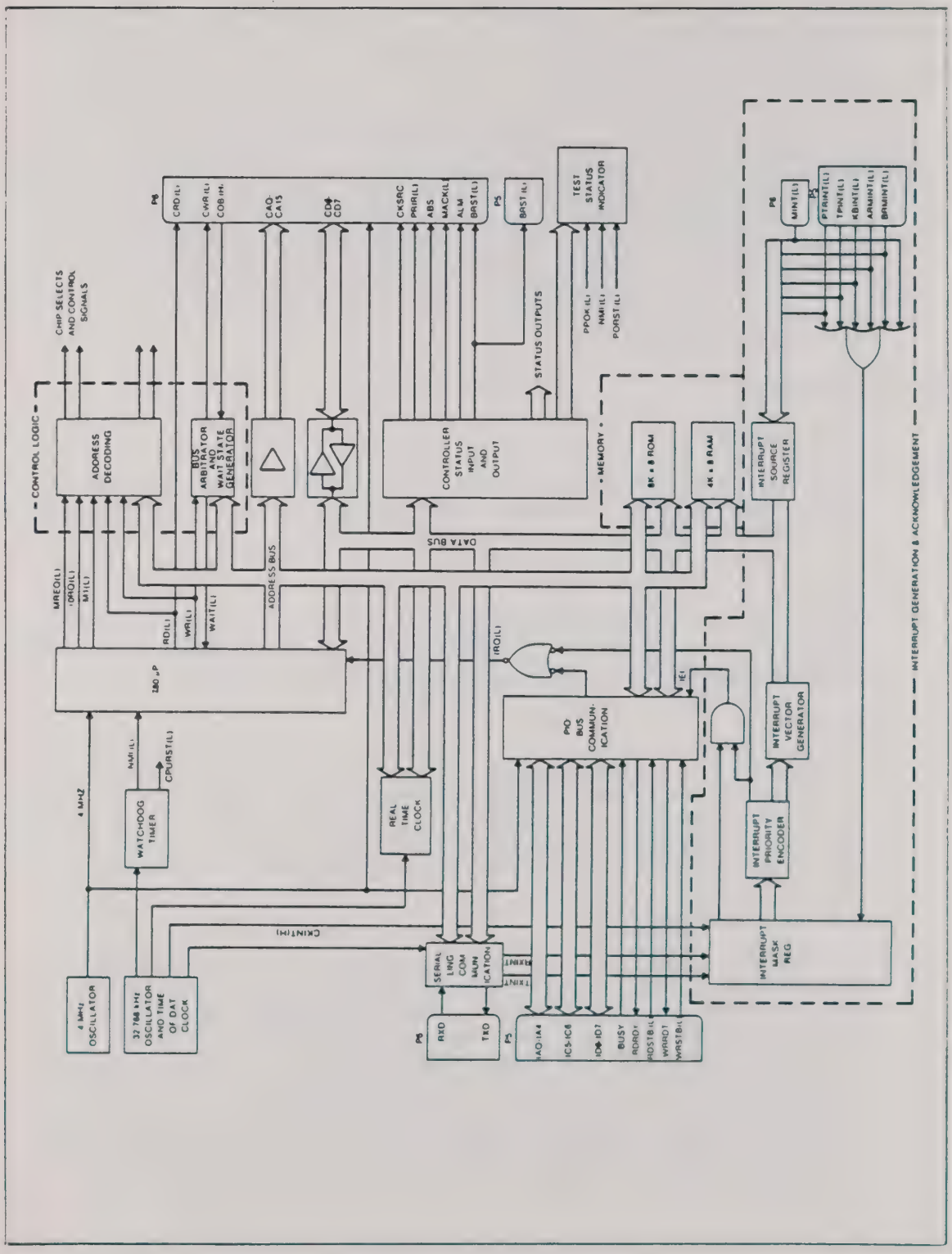


Figure 3-9. Controller Block Diagram

- Serial Link Communication

  Communication between the controller and the measurement and control devices (High Performance A/D Converter, Digital Input/Output, Current/Voltage Analog Output, and Counter/Totalizer Input Options) is done over the serial link. All serial link communication is between the controller and measurement and control devices; measurement and control devices do not communicate directly with each other. Serial Link transmission is asynchronous at 25 kHz.

- Interrupt Generation and Acknowledgement

  Several real time events occur periodically in the data logger that must cause the firmware program to temporarily stop what it is doing, take care of the real time event, and then resume what it was doing. The processor is interrupted during PIO Bus and Serial Link operations, and by the real time clock, watchdog timer, and the Advanced Math Option. Circuitry is provided to synchronize the asynchronous events with the processor and select the interrupt of highest priority for presentation to the processor.

- Controller Status Input and Output

  Operation of the data logger requires the ability to sense and generate several special signals. These signals allow the processor to sense or measure the serial output of the clock chip, the external trigger input used to trigger scans, the status of primary instrument power (to verify that the processor will be allowed to execute for a guaranteed minimum time), and the position of the front panel key switch. The circuitry in this block generates the external master alarm output relay drive, a signal to reset the devices on the PIO Bus, drive signals for the Test Status LED Indicator on this assembly, and several signals used to synchronize memory operations.

- Time of Day Oscillator and Clock

  The time of day clock keeps track of the current year, month, day, hour, minute, and second. It is powered by the battery supply, so the data logger can keep track of current time when the instrument is off. The clock chip derives its timebase from a 32.768 kHz crystal oscillator. This oscillator also functions as a frequency divider, supplying the watchdog timer with a 2 Hz clock and providing the microprocessor with an interrupt 32 times a second.

- Watchdog Timer

  The watchdog timer provides a mechanism to restart the data logger should some catastrophic event occur that stops the processor's operation. This timer interrupts the processor twice each second. If the firmware does not acknowledge this interrupt, the Watchdog Timer circuitry resets the entire data logger causing a complete restart of the instrument.

DETAILED CIRCUIT ANALYSIS

Microprocessor

A 4-MHz Z-80 microprocessor, U25, is the main processor of the instrument. It receives it's clock from oscillator Y1.

The eight data lines from the processor are used to communicate with devices on the Controller Assembly and the Memory Assembly. The data bus is resistively terminated to the +5 volt supply using Z8 and buffered bi-directionally by U32, then sent to the motherboard as signals CD0 through CD7 (Controller Data 0 through 7).

The sixteen address signals from the processor are decoded on the Controller Assembly to enable various memory and input/output registers. The processor address signals are also used on the Memory Assembly. This address bus is resistively terminated to the +5 volt supply using Z6 and Z7 and buffered by U23 and U24 before leaving the assembly as signals CA0 through CA15 (Controller Address 0 through 15).

Oscillator

The 4-MHz master clock of the assembly is generated by Y1. This clock signal is also used to clock the microprocessor on the Advanced Math Option. It is buffered by parts of U15 before leaving the assembly as signal CKSRC (Clock Source).

Control Logic

MEMORY AND I/O ACCESSES

The Z80 microprocessor has two distinct address spaces, Memory Space and I/O Space. The type of memory or input/output operation to be performed by the microprocessor is determined by signals MREQ(L), IORQ(L), M1(L), RFSH(L), RD(L), and WR(L) (Memory Request, Input/Output Request, Machine Cycle One, Refresh, Read, and Write respectively). The operation corresponding to each signal is listed in Table 3-1. Timing diagrams for each type of access are given in Figures 3-10 through 3-15.

ROM (U26) and RAM (U27, U28) residing on the Controller Assembly and the Memory Assembly are accessed when the microprocessor generates Memory Space Addresses. All other parts of the mainframe are accessed via the microprocessor's I/O Space. Those parts are:

- PIO Bus (parallel I/O interface (U1))
- Serial Link UART (Universal Asynchronous Receiver/Transmitter (U4))
- Interrupt Mask Register (U11)
- Interrupt Source Register (U8)
- Controller Output Register (U33)
- Controller Status Register (U9)
- Non-Volatile Time of Day Clock (U39 or U41)

The same address and data busses are used for both I/O and memory accesses, but address decoding is different for the two cases. The results of the two separate decoding paths are given in Figure 3-16, the Memory Space Map, and Figure 3-17, the I/O Space Map.

Table 3-1. Memory and I/O Access Signals

MREQ(L)	IORQ(L)	M1(L)	RFSH(L)	RD(L)	WR(L)	Cycle Type
0	1	0	1	0	1	Instruction Fetch
0	1	1	1	0	1	Memory Read
0	1	1	1	1	0	Memory Write
0	1	1	0	1	1	Memory Refresh
1	0	1	1	0	1	I/O Input
1	0	1	1	1	0	I/O Output
1	0	0	1	1	1	Interrupt Acknowledge

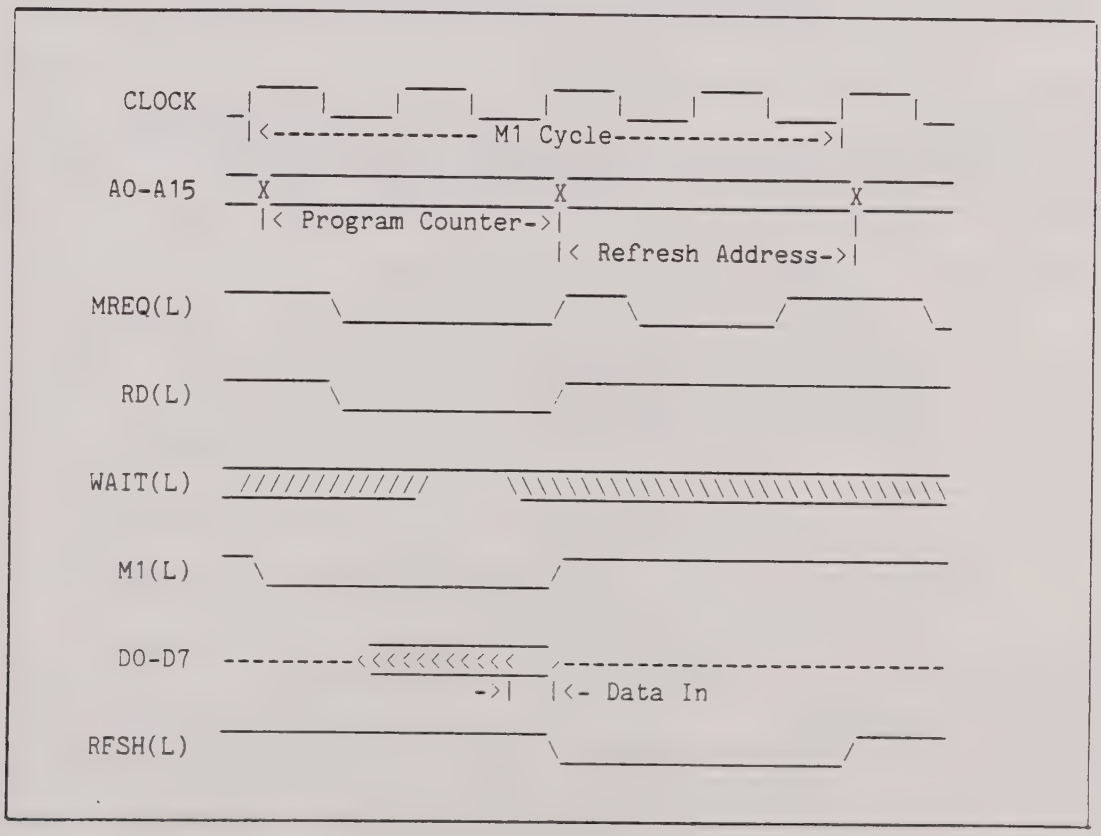


Figure 3-10. Instruction Opcode Fetch Without Wait States

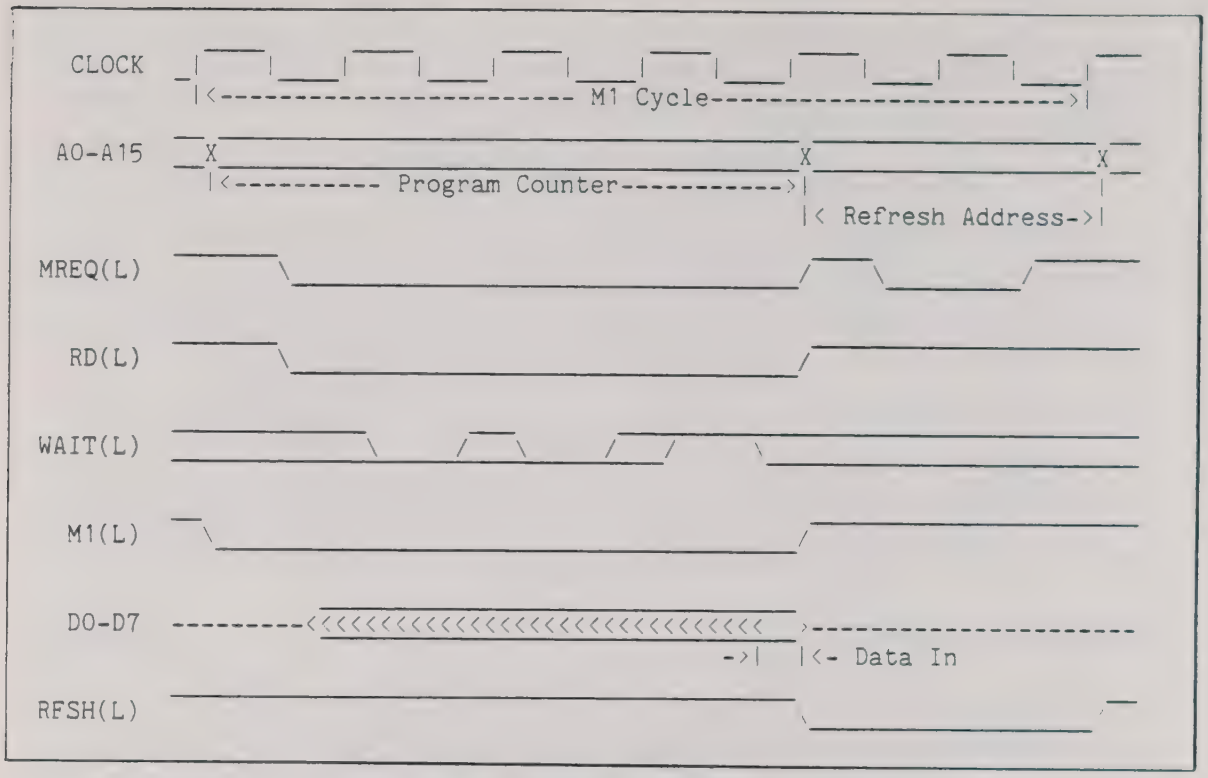


Figure 3-11. Instruction Opcode Fetch With Wait States

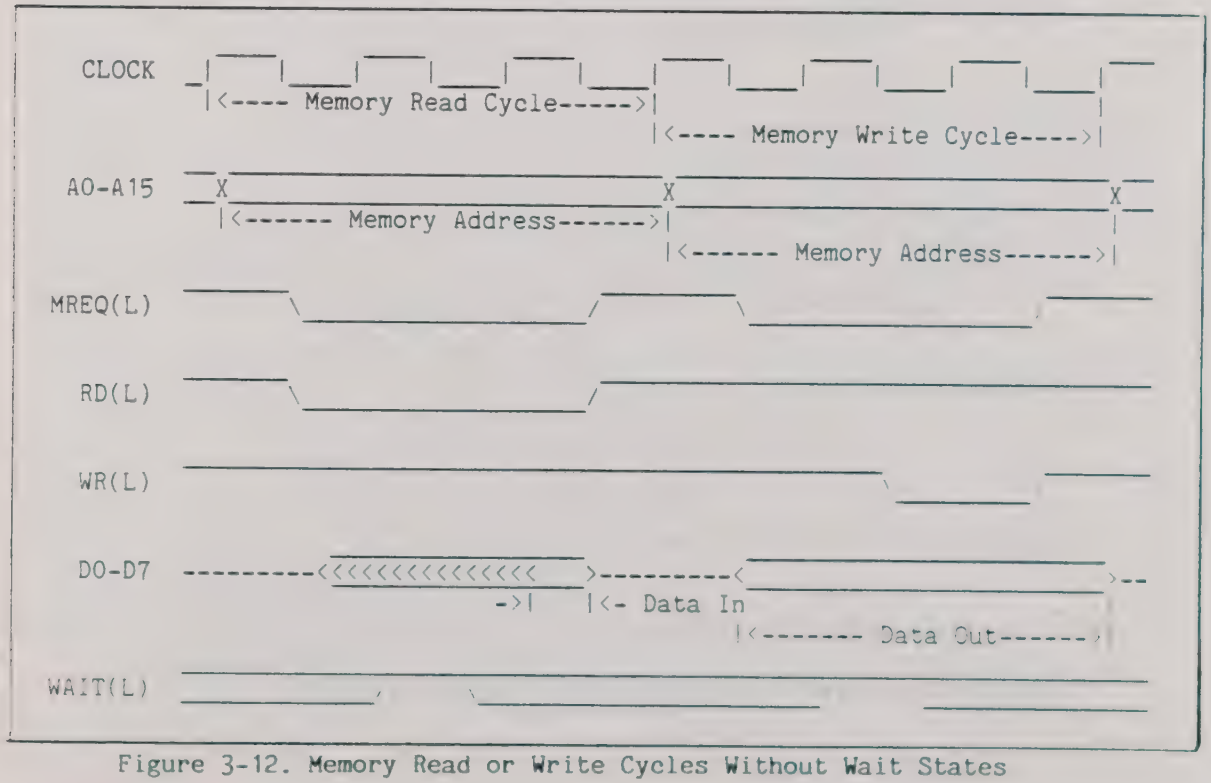


Figure 3-12. Memory Read or Write Cycles Without Wait States

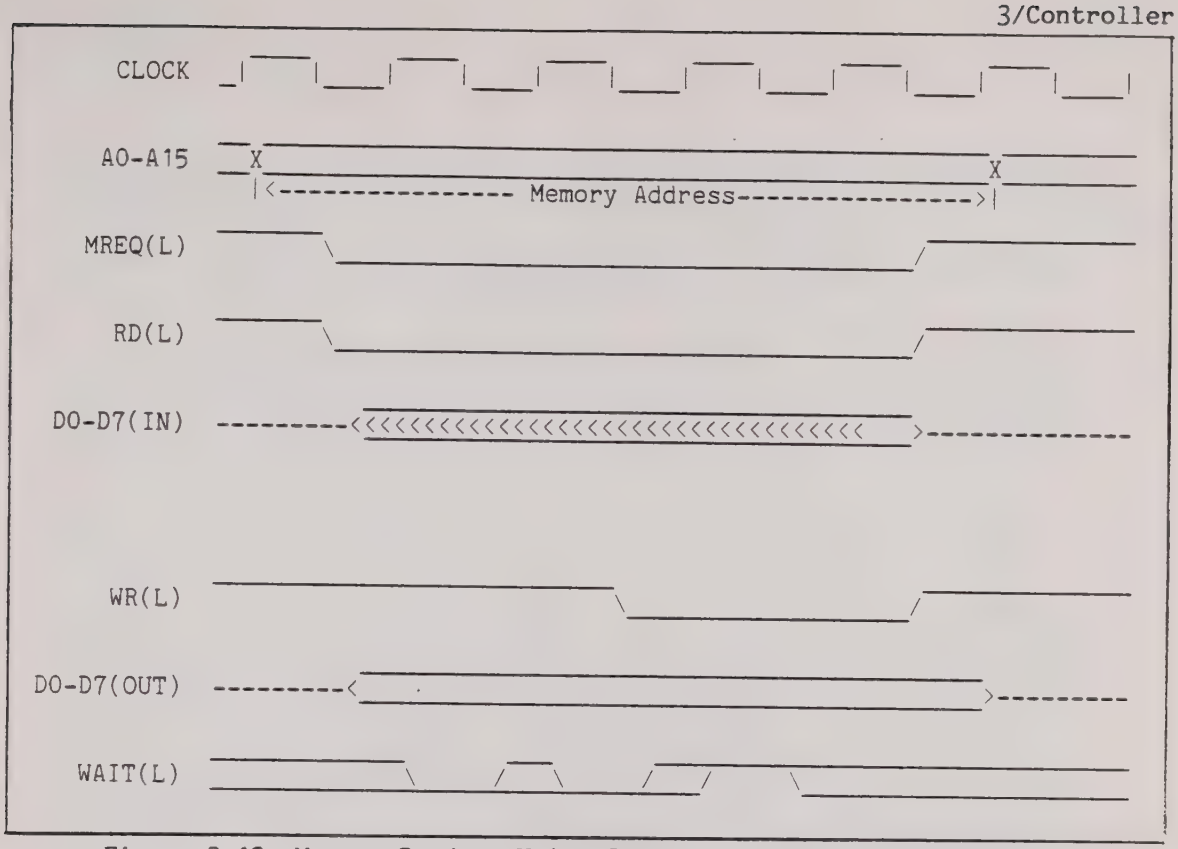


Figure 3-13. Memory Read or Write Cycles With Wait States

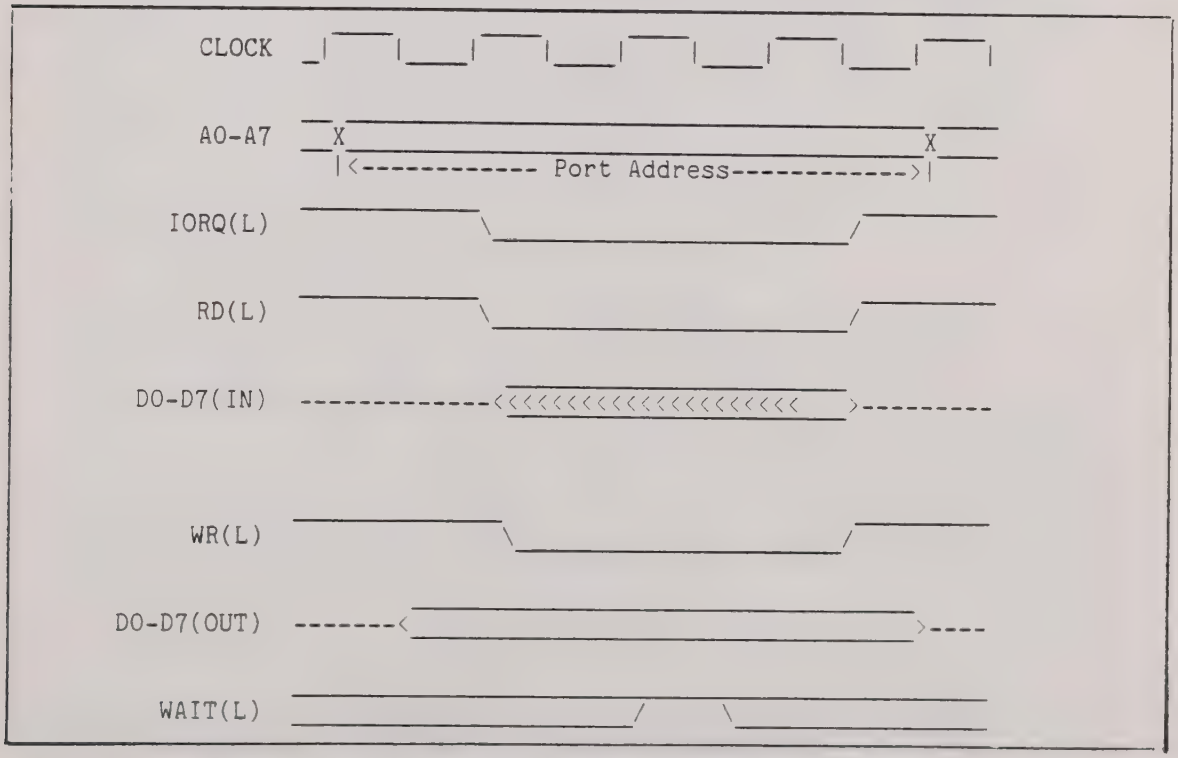


Figure 3-14. Input or Output Cycles Without Wait States

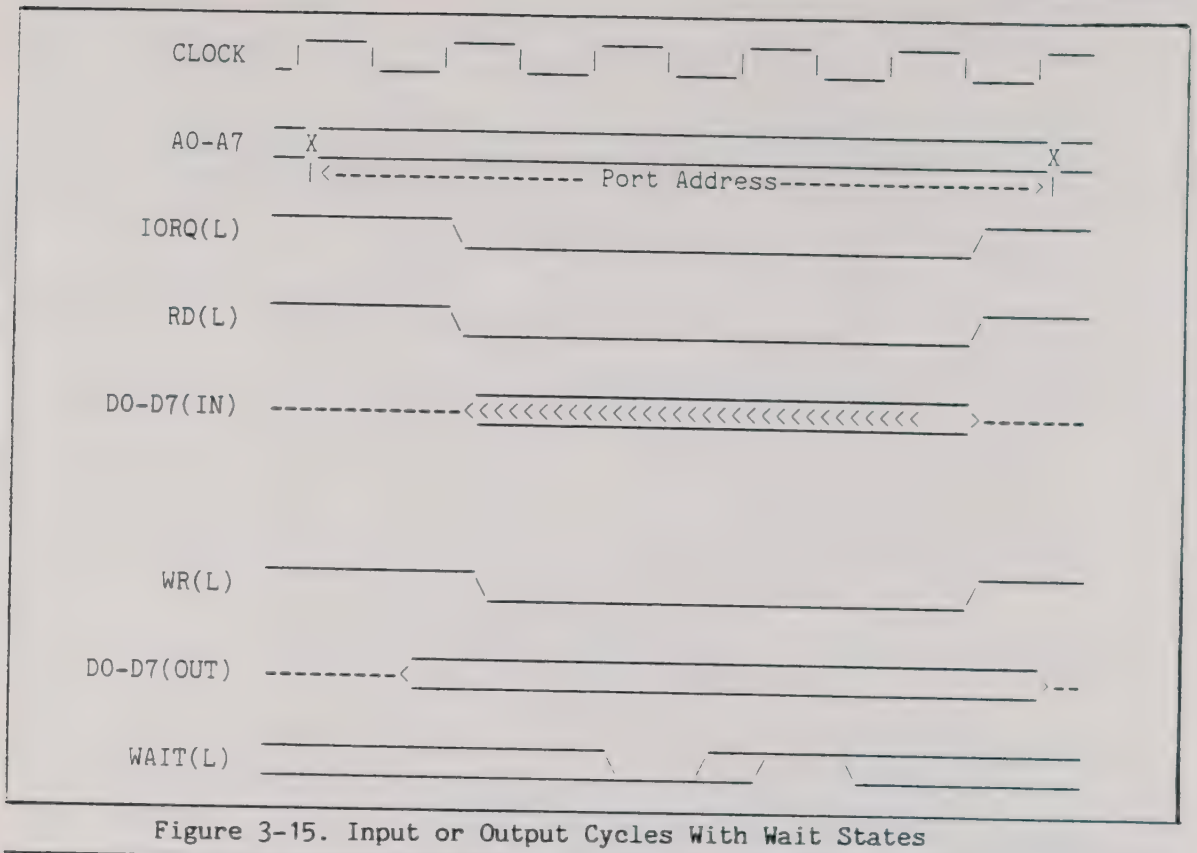


Figure 3-15. Input or Output Cycles With Wait States

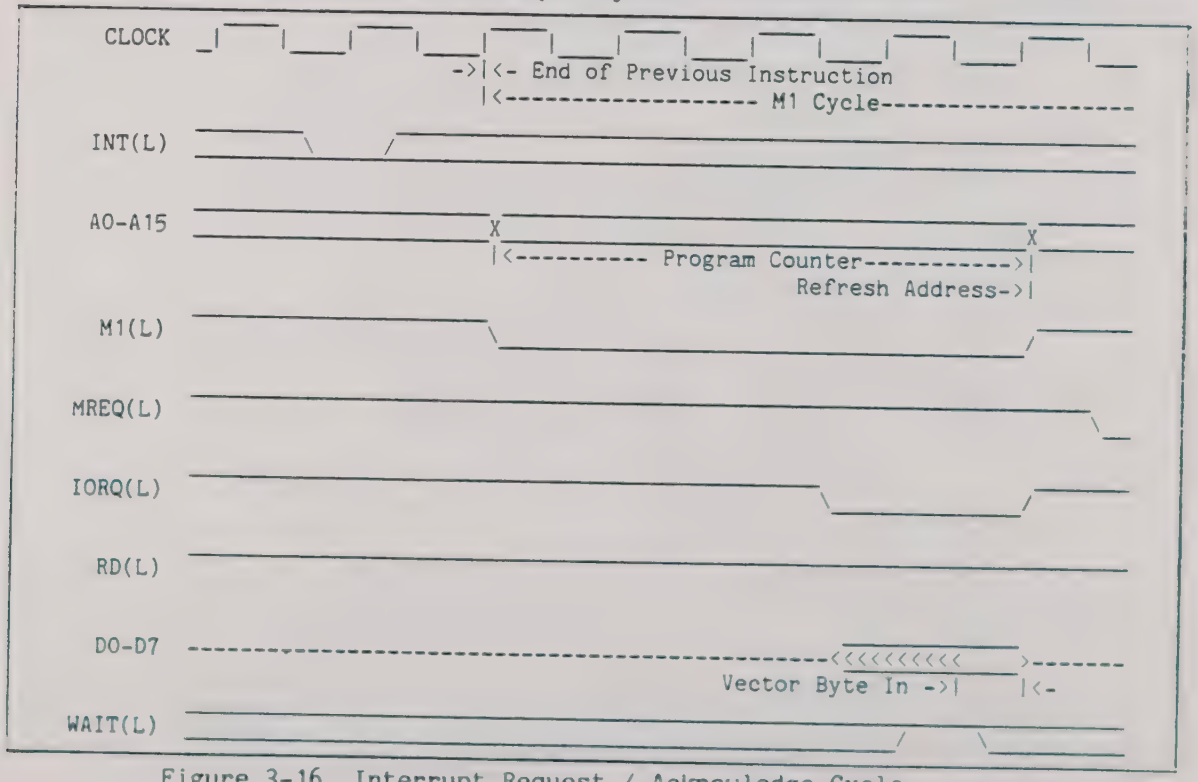


Figure 3-16. Interrupt Request / Acknowledge Cycle

Memory Accesses

An instruction fetch or simple read from ROM causes the Wait State Generator to introduce one wait state (see Figures 3-9 and 3-10). This added wait state compensates for the ROM's longer access time. A ROM access occurs when MREQ(L) and A15 are low. Accesses to RAM on the controller are performed without wait states. Accesses to RAM residing on the Memory Assembly incur zero or more wait states.

RAM on the Memory Assembly is accessible from two microprocessors: the microprocessor on the Controller Assembly and the one on the Advanced Math Assembly. Since the RAM's cannot be accessed simultaneously by two processors, circuitry exists to arbitrate the access to this shared memory.

Wait states in the memory access may also be introduced if an access to shared RAM is delayed by arbitration.

Memory Arbitration involves the Controller, Memory, and Advanced Math assemblies. Therefore, the logic circuitry to implement bus arbitration is spread across the three assemblies. This logic has two basic states, one granting memory access to the Advanced Math assembly and the other granting access to the Controller. Access requests from the Advanced Math and Controller Assemblies can be either active or inactive; combinations of the two yield four access request states. Thus, the entire arbitrator has eight possible combinations, corresponding to all combinations of four access request states and two access grant states.

Components U36, U17, U20, and U19 implement the controller portion of the memory arbitration logic. The microprocessor on the controller executes wait states until the controller on bus (COB(H)) signal is asserted true by the Advanced Math Assembly. If the Advanced Math Assembly is not installed, a resistor in Z4 places COB(H) in the true state and no arbitration or wait state generation due to shared memory conflicts occurs.

I/O Accesses

Large portions of I/O space are unused. Consequently, not all of the address lines are used to accomplish full decoding (a technique known as "sparse mapping"). Since addresses in I/O space are sparsely mapped, more than one address can be used to access the same physical hardware. For simplicity, the I/O Space Map shows only one of these addresses.

For some locations in I/O space, the data bus is ignored during a write cycle. For these locations, the write cycle is used to produce a strobe signal. All the locations that produce a strobe when written are labeled as such in the I/O Space Map (Figure 3-18).

	Read	Write	
Memory assy. RAM	FFFF 9000	FFFF 9000	Memory assy. RAM
Controller assy. RAM	8FFF 8000	8FFF 8000	Controller assy. RAM
Memory assy. ROM	7FFF 2000	7FFF	Not Used
Controller assy. ROM	1FFF 0000	0000	

Figure 3-17. Memory Space Map

	Read	Write	
		00D0	NMI(L) Reset Strobe
		00B2	CKINT Reset Strobe
		00B0	TGI Reset Strobe
		00A3	CKST Clock Reg.
		00A2	Interrupt Mask Reg.
		0097	Seg. D, Status Indicator
		0096	Seg. G, Status Indicator
		0095	Seg. A, Status Indicator
		0094	PRIR (H)
		0093	ABS (H)
		0092	MACK (H)
		0091	ALM (H)
		0090	BRST (H)
		0080	UART Xmit Buffer Reg.
Controller Status Reg.	0070		
Interrupt Source Reg.	0060		
National Clock Chip	0050		
National Clock Chip	0040		
UART Status Flags	0020		
UART Receiver Reg.	0010		
PIO Port B Control	0003		
PIO Port B Data	0002		
PIO Port A Control	0001		
PIO Port A Data	0000		

Figure 3-18. I/O Space Map

ADDRESS DECODING

The address decoding logic implements the Memory Space Map (Figure 3-17) and the I/O Space Map (Figure 3-18). Address lines A0 to A15 and control signals MREQ(L), IORQ(L), and M1(L) to select a unique location in memory or I/O space. The memory cycle is qualified by mutually exclusive control signals RD(L) and WR(L), which determine a read or write cycle, respectively.

Two outputs of a 3-line-to-8-line decoder (U38) select one of two RAM's (U27 or U28) on the controller assembly occupying the address range 8000 to 8FFF in memory space. A two-level cascade of OR gates (U34) selects the 8k byte ROM (U26) on the controller assembly occupying the address range 0000 to 1FFF in memory space. When a controller ROM or RAM is selected, OMS (on-board memory strobe) goes high for the duration of the memory cycle.

Two 3-line-to-8-line decoders control all I/O space accesses. One (U29) controls all I/O write cycles, and is enabled when A7 is high, WR(L) is low, and IORQ(L) is low. The other (U30) controls all I/O read cycles, and is enabled when A7 is low, M1(L) is high, and IORQ(L) is low.

Memory

Eight K-bytes of ROM are provided by U26. Gating in U34 generates the chip select for the ROM when it detects memory requests in the address range 0000 through 1FFF.

U27 and U28 together provide four K-bytes of RAM at addresses 8000 through 8FFF. U38 detects memory requests in this address range and generates the chip selects for the RAM's.

PIO Bus Communication

The PIO Bus is the interface through which the controller communicates with all logging and interface devices. The logging and interface devices include the printer, display and keyboard, DC100 Cartridge Tape Option, and the Port A and Port B communication options.

PIO BUS COMMUNICATION AND CONTROL

The PIO Bus consists of address lines, control lines, data lines, and interrupt lines. The address lines are IA0 through IA4 (Interface Address); the control lines are IC5 and IC6 (Interface Control), BUSY, RDRDY (Read Ready), RDSTB(L) (Read Strobe), WRRDY (Write Ready), and WRSTB(L) (Write Strobe); the data lines are ID0 through ID7 (Interface Data). The interrupt lines are BRMINT(L) (Port B Interrupt), ARMINT(L) (Port A Interrupt), KBINT(L) (Keyboard Interrupt), TPINT(L) (Cartridge Tape Interrupt) , and PTRINT(L) (Printer Interrupt). Except for the interrupt lines, all PIO Bus signals connect directly to the Z-80-PIO chip U1. Data lines ID0 to ID7 connect to PIO Port A of the Z-80-PIO, while IA0 to IA4, IC5, IC6, and BUSY connect to Port B of the Z-80-PIO

chip. All PIO Bus signals are resistively terminated to +5 volts by Z1, Z2, and Z3.

PIO BUS ADDRESSING AND MODE CONTROL

A two-out-of-five coding scheme is used to form valid PIO Bus addresses. Using this method, all valid addresses have two address lines low and three address lines high. The address assignments are listed in Table 3-2.

Table 3-2. PIO Bus Addresses

Address					Addressed PIO Bus Device
IA4	IA3	IA2	IA1	IA0	
1	1	1	0	0	Keyboard / Display Assembly
1	1	0	1	0	Printer Assembly
1	1	0	0	1	DC 100 Cartridge Tape Assembly
1	0	1	1	0	Port A I/O Assembly
1	0	1	0	1	Port B I/O Assembly
1	1	1	1	1	(No PIO Bus Device Addressed)

Along with the address information is a two-bit control code indicating the type of bus transaction in process. In order to avoid ambiguity, this control code is changed only when no devices are addressed (address signals IA0 through IA4 are all high). Four modes are possible (see Table 3-3). They are, Device Quiet, Device Write, Device Read, and Device Poll.

Device Quiet Transactions

A device quiet transaction forces a PIO Bus device to return its interrupt request line to the inactive state. Each PIO Bus device has a dedicated interrupt line (see Table 3-5). No data is transferred over data lines ID0 through ID7 during this transaction.

Table 3-3. PIO Bus Control Codes

IC6	IC5	PIO Bus Transaction Mode
0	0	Device Quiet
0	1	Device Write
1	0	Device Read
1	1	Device Poll

Device Write Transactions

A device write transaction transfers a byte from a PIO Bus device to the controller. The transfer is controlled by signals WRRDY (Write Ready) and WRSTB(L) (Write Strobe).

When WRRDY is true, the controller waits for a byte from the addressed PIO Bus device. The PIO Bus device responds by placing a byte on data lines ID0 through ID7, then pulsing WRSTB(L) low. Pulsing WRSTB(L) low causes the Z-80-PIO chip to take WRRDY false. The controller then de-addresses the PIO Bus device before reading the byte from the Z-80-PIO chip.

A device write transaction is initiated by a PIO Bus device that wishes to send a byte to the controller. To start, the PIO Bus device asserts a "Device Service Request" over its dedicated interrupt request line. Only one byte is sent to the controller during each cycle, so when a device has multiple bytes to send, it keeps the Device Service Request asserted until it has been addressed to send the last byte.

Device Read Transactions

A device read transaction transfers one or more bytes from the controller to an PIO Bus device. The transfer is controlled by signals RDRDY (Read Ready) and RDSTB(L) (Read Strobe).

When RDRDY is true, the controller has a byte to send to the addressed device. The device responds by setting RDSTB(L) low, reading the byte on data lines ID0 to ID7, and then setting RDSTB(L) high (in that sequence). Due to the nature of the Z-80-PIO chip, a valid byte is present on ID0 to ID7 only when RDSTB(L) is low.

Immediately after reading the byte, the device determines if it is able to accept any more bytes from the controller. If it cannot, it sets BUSY high; if it can, it sets BUSY low.

Pulsing RDSTB(L) low causes the Z-80-PIO chip to take RDRDY false. If the controller has another byte to send to the device and the BUSY line is false, then it writes a new byte to the Z-80-PIO chip, causing RDRDY to become true again. Otherwise, the controller de-addresses the device.

Device Poll Transactions

The controller determines if a device is free to accept bytes by doing a device poll transaction. If the BUSY line is true during a device poll transaction, then the addressed device is "busy" and cannot accept bytes; conversely, if the BUSY line is false, then it is not busy and the controller may do a device read transaction.

Device quiet and device write transactions are allowed regardless of an device's busy condition.

Serial Link Communication

The 2280 Series measurement and control option assemblies communicate with the controller over the serial link. Transmissions from the controller go out serially on the TXD (Transmit Data) signal line via the Power Supply Assembly to all devices; transmissions from each device are received by the controller on the RXD (Receive Data) signal line. These signals leave/enter the assembly via connector P6 as TTL levels. They are converted to (from) RS-422 signals on the Power Supply Assembly.

All measurement and control devices receive all transmissions from the controller, but since these devices share the same communication line back to the controller, only one of these devices can transmit at a time. A measurement and control device is granted permission to transmit by interpreting messages sent to or from the controller.

A standard UART (Universal Asynchronous Receiver/Transmitter), U4, acts as the interface between the serial link and the microprocessor bus.

The UART is configured to operate full-duplex with odd parity, 8 data bits, and 1 stop bit at a 25K-baud rate. Two buffer registers within the UART, the TBR (Transmitter Buffer Register) and the RBR (Receiver Buffer Register), hold the next byte to be transmitted on the TXD line and the last byte received on the RXD line, respectively. Two shift registers, TR (Transmitter Register) and RR (Receiver Register), hold the bytes currently being transmitted and received, if any. The clock inputs TRC (Transmitter Register Clock) and RRC (Receiver Register Clock) for these shift registers determine the transmit and receive baud rates, and are divided by 16 by prescalers in the UART. Both clock inputs are driven by the signal SLCLK (Serial Link Clock), which is the output of the 4-MHz oscillator, Y1, divided by 10 using U16.

If the Transmitter Buffer Register is full and the Transmitter Register is empty, the byte contained in the TBR is automatically transferred to the TR and begins transmission. When this happens, the TBRE (Transmitter Buffer Register Empty) output goes high.

After a byte has been received, it is transferred from the Receiver Register to the Receiver Buffer Register, and the DR (Data Received) output goes high. When the microprocessor reads the received byte, inputs DRR(L) (Data Received Reset) and RRD (Receiver Register Disable) are pulsed low. DRR (L) resets the DR output, and RRD drives the received byte onto the microprocessor data bus. If the previously received byte (if any) has not been read by the microprocessor when a new byte is transferred from the Receiver Register to the Receiver Buffer Register, the OE (Overrun Error) output goes high. Also, if an invalid parity bit or stop bit was detected, the PE (Parity Error) output or FE (Framing Error) output goes high, respectively.

Four UART outputs comprise the UART Status Flags Register in I/O Space: OE, FE, PE, and TRE (Transmitter Register Empty). These are available to the processor for reading when four buffers of U3 are enabled by the SFS(L) (Status Flag Select) signal.

Two outputs are used as interrupt signals; TBRE is used as the TXINT (Transmitter Interrupt) signal and DR is used as the RXINT (Receiver Interrupt) signal.

Interrupt Generation and Acknowledgement

The controller requests interrupts in program execution when either the IRQ(L) input or the NMI(L) input to the Z80 microprocessor is low. There are three possible ways that the Z80 can respond to IRQ(L), but only one is used in the 2280 Series. The interrupt method used requires the

source of the interrupt to place the lower half of an interrupt vector on the data bus during an interrupt acknowledge cycle (see Table 3-1 and Figure 3-16).

Note

A vector is a 16-bit address pointing to a location in memory containing the address of the beginning of the interrupt service routine.

The upper half of the vector is contained in a dedicated Z80 register. After the interrupt acknowledge cycle, the Z80 pushes the current program counter on the stack. If the Z80 is responding to NMI(L), then it branches to location 0066. Otherwise (responding to IRQ(L)), the Z80 reads the interrupt service routine starting address from the 2-byte location pointed to by the interrupt vector, and then it branches to that address.

The interrupt vector comes from one of two sources, the Z-80-PIO chip or the Interrupt Vector Generator. Only one of the two can actively request an interrupt at any given time. The vector is supplied by the active requester. Conceptually, there are two interrupt subsystems:

1. The Z-80-PIO chip

2. The Interrupt Mask Register, Interrupt Priority Encoder, and Interrupt Vector Generator.

The second subsystem has higher priority than the Z-80-PIO chip, so if both subsystems have interrupts pending simultaneously, the Z-80-PIO chip is inhibited (by the IEI, or Interrupt Enable Input, signal) from actively requesting an interrupt.

The Interrupt Mask Register (U11) selectively disables (masks) all interrupts except NMI(L) (non-maskable interrupt). For masking purposes, five different interrupts are distinguished:

- Z-80-PIO Interrupts
- 32-Hz Clock Interrupt
- Serial Link UART Transmitter Interrupt
- Serial Link UART Receiver Interrupt
- PIO Bus Device Interrupt

The PIO Bus Device Interrupt is active when any of the following devices requests an interrupt: the Advanced Math optional assembly, Port B communication device, Port A communication device, display and keyboard assembly, DC100 Cartridge Tape optional assembly, or the printer assembly. While these are combined to form a single maskable interrupt, it is still possible to distinguish them by reading the Interrupt Source Register.

Except for NMI(L) and Z-80-PIO chip interrupts, interrupts not disabled by the Interrupt Mask Register are passed on through enabling gates U12 and synchronization latch U7 to the Interrupt Priority Encoder (U6).

The Interrupt Priority Encoder has two outputs, an interrupt request line and a priority code. If its interrupt request line is active, the Z-80-PIO chip's interrupt request line is forced inactive by the Interrupt Enable Input to the Z-80-PIO chip. The priority code (a binary code representing the pending interrupt with the highest priority) is converted to the lower byte of a vector address by the Interrupt Vector Generator (U5) and placed on the data bus during an interrupt acknowledge cycle.

If the Z-80-PIO chip interrupt is not masked out by the Interrupt Mask Register and no active interrupts are pending at the Interrupt Priority Encoder inputs, then the Interrupt Enable Input to the Z-80-PIO chip goes true. When the Interrupt Enable Input goes true, the Z-80-PIO chip is allowed to generate interrupt requests.

Active interrupt requests are reset in several ways. After the Z-80-PIO chip has supplied an interrupt vector during an interrupt acknowledge cycle, the interrupt request is reset. While being serviced, the Z-80-PIO monitors the data bus, resetting its "under service" state when it detects a Z-80 "return from interrupt" instruction. The Z-80-PIO does not request another interrupt until the current interrupt being serviced is acknowledged. PIO Bus Device interrupts are generated by intelligent subsystems, and are reset in accordance with an intra-system communication protocol. serial link UART interrupts are generated when a byte has been transmitted or received, and are reset when a new byte is loaded into the transmitter or the received byte is read, respectively. Finally, the 32-Hz clock interrupt and the non-maskable interrupt (generated by the watch-dog timer) remain active until forcibly reset by the CKINT Reset Strobe and the NMI(L) Reset Strobe, respectively.

Interrupt Mask Register

The Interrupt Mask Register allows the processor to selectively enable and disable certain interrupts. Table 3-4 shows the mapping of each interrupt to a particular data bus line. An I/O write cycle to the Interrupt Mask Register with a particular data bit set to one enables the corresponding interrupt; set to zero, it disables the interrupt. The Interrupt Mask Register consists of a hex D-type latch (U11), four NAND gates (U12), and an AND gate (U20).

Table 3-4. Interrupt Mask Register

Data Bus Line	Corresponding Interrupt
D0	Z-80-PIO Chip Interrupts
D1	PIO Bus Device Interrupts
D2	32 Hz Clock Interrupt
D3	UART Transmitter Interrupt
D4	UART Receiver Interrupt

Interrupt Source Register

The Interrupt Source Register is a hex tri-state buffer (U8) that allows the processor to determine which I/O device caused an I/O device interrupt. An I/O read cycle of the register drives the current status of the dedicated I/O device interrupt lines onto the data bus, according to the mapping in Table 3-5.

Interrupt Priority Encoder

A hex D-type latch (U7) and an 8-line-to-3-line priority encoder (U6) comprise the Interrupt Priority Encoder. Interrupts that have been masked by the Interrupt Mask Register drive the Interrupt Priority Encoder. If any of the four is active and is enabled by the Interrupt Mask Register, the Interrupt Priority Encoder outputs a priority code (see Table 3-6) and drives its GS(L) output low. If GS(L) is low, Z-80-PIO chip interrupts are disabled by the IEI (Interrupt Enable Input) to the Z-80-PIO chip. The priority code is sent to the Interrupt Vector Generator. The UART Receive Interrupt has the highest priority.

Table 3-5. Interrupt Source Register

Interrupt Signal	Device	Data Bus Line
PTRINT(L)	Printer	D0
TPINT(L)	Cartridge Tape	D1
KBINT(L)	Display / Keyboard	D2
ARMINT(L)	Port A	D3
BRMINT(L)	Port B	D4
MINT(L)	Advanced Math	D5

Table 3-6. Interrupt Priority Codes

Interrupt Signals				Priority Code		
(i)	(ii)	(iii)	(iv)	A2	A1	A0
0	1	1	1	0	0	1
X	0	1	1	0	1	0
X	X	0	1	0	1	1
X	X	X	0	1	0	0

(i) = Printer, Cartridge Tape, Display/Keyboard, Port A, Port B, or Advanced Math Interrupts
(ii) = 32 Hz Clock Interrupt
(iii) = UART Transmitter Interrupt
(iv) = UART Receiver Interrupt

0 = Interrupt active and enabled
1 = Interrupt inactive or disabled
X = Don't care

Interrupt Vector Generator

If the GS(L) output of the Interrupt Priority Encoder is low during an interrupt acknowledge cycle, the Interrupt Vector Generator (U5) places the lower byte of an interrupt vector on the data bus. The Interrupt Vector Generator simply shifts the priority code up one bit position (e.g., multiplies it by two) to ensure that the vector has an even address, and drives data lines D0, D4, D5, D6 and D7 low.

Controller Status Input and Output

CONTROLLER OUTPUT REGISTER

The controller output register is an 8-bit, bit-addressable register (U33) used for several single-bit outputs:

- Test Status Indicator LED segments A, D, and G
- PRIR(L) (Priority), which forces the shared RAM arbitrator to grant access to the controller
- ABS (Arm Bank Select), which arms the Bank Select Register on the memory assembly
- MACK(L) (Math Acknowledge), which causes a non-maskable interrupt on the Advanced Math option and is used as an acknowledgement
- ALM (Alarm), which controls an external alarm output
- BRST(L) (Bus Reset), which resets the Advanced Math option and all assemblies residing on the PIO bus.

Each bit in the controller output register has a unique address. A0, A1 and A2 select which bit is to be written and the D0 input provides the data.

CONTROLLER STATUS REGISTER

The controller status register is a hex tri-state buffer (U9) read by the microprocessor to determine the status of the signals listed in Table 3-7.

The CKOUT (Clock Out) signal is the serial data output of real time clock chip U41.

When high, TGIL (Trigger Input Latched) indicates that a positive edge occurred on the input TGI (Trigger Input), which is an external input used for triggering scan cycles. Signal TGIL is reset by the TGI Reset Strobe (see Figure 3-18).

When high, PPOK(L) (Primary Power OK) indicates that primary power to the instrument is no longer sufficient to guarantee continued operation.

Input SW (Switch) indicates whether the front panel key switch is in the "RUN" (SW = 1) or in the "PROGRAM" position (SW = 0).

The CCT (Clock Chip Type) signal indicates whether clock chip U39 (CCT = 1) or clock chip U41 (CCT = 0) is installed. The state of CCT is determined by the presence or absence of optional resistor R2.

Table 3-7. Controller Status Register

Status Signal	Data Bus Line
CKOUT	D0
TGIL	D1
PPOK(L)	D2
SW	D3
CCT	D4

TEST STATUS INDICATOR

The Test Status Indicator (DS1) is a 7-segment LED display used to indicate the status of both hardware and software during testing. Segments A, D, and G are driven by the controller output register. Segment B is driven by the PPOK(L) (Primary Power OK) signal, segment E is driven by the NMI(L) (Non-maskable Interrupt) signal, and segment F is driven by the PORST(L) (Power-on Reset) signal. Segment C is always on. Figure 3-19 shows each segment and what it signifies, and a summary of the function of each segment follows:

Segment A

Segment A is forced by hardware to be lit at power-up. If operating properly, the microprocessor extinguish this segment soon after power is applied. The normal operating condition of this indicator is off.

Segment B

Segment B is illuminated when Primary Power is correct, therefore it is normally lit.

Segment C

Segment C is lit when the +5 volt dc supply is operating.

Segment D

Segment D is lit if the 2280 fails the RAM test at power up. It should normally be off.

Segment E

Segment E flashes at a 2 Hz rate if the processor has failed to service the watchdog timeout interrupt. It should normally be off.

Segment F

Segment F is lit while the power on reset signal is active.

Segment G

Segment G is lit if the ROM checksum test performed at power up failed. It should normally be off.

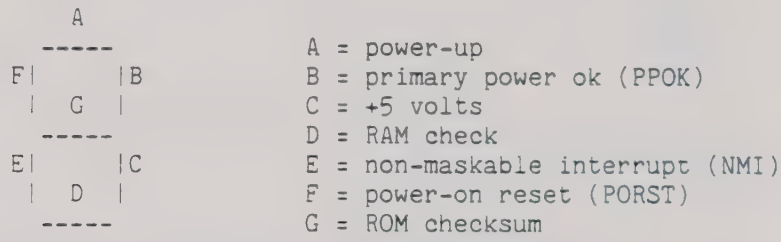


Figure 3-19. Controller and Memory Test LED

Time of Day Oscillator and Clock

The real-time clock keeps track of the current year, month, day, hour, minute, and second. One of two possible types of clock chip is installed (either U39 or U41). Both are powered by the non-volatile battery-backed supply to keep the clock running when power is off.

Both clock chips derive their timebase from a 32.768 kHz crystal oscillator (U31, Y2). This oscillator also functions as a frequency divider, supplying the watchdog timer with a 2 Hz clock and providing the Z80 microprocessor with 32 interrupts each second.

Watchdog Timer

During normal operation, the 2280 Series operating software periodically resets the watchdog timer with the NMI(L) Reset Strobe. Every half second the watchdog timer produces a non-maskable interrupt, which causes the software to respond with the NMI(L) Reset Strobe.

The watchdog timer takes further action if abnormal operation is detected. This occurs if the processor fails to vector to the non-maskable interrupt routine, or if the operating software detects a fatal error and foregoes resetting the watchdog timer. In this case, the watchdog timer pulls CPURST(L) low one-half second after NMI(L) becomes active. Signal CPURST(L) remains low for one-half second, then goes high again. This sequence resets most of the circuitry on the controller and sends BRST(L) low (which resets the Advanced Math assembly and all the assemblies on the PIO bus). The general effect is a complete restart of the data logger. The D-type flip-flops of U18 clocked with the 2 Hz output of U31 perform this function.

Memory

FUNCTIONAL DESCRIPTION

The Memory Assembly contains most of the ROM accessed by the microprocessor on the Controller Assembly , and all the RAM accessible to the Controller Assembly and the Advanced Math option . The ROM and RAM portions are separate, so the Controller Assembly can access the ROM at the same time the Advanced Math option accesses shared RAM. Simultaneous access of shared RAM by both the Advanced Math option and Controller Assembly is not allowed, and to prevent this, a bus arbitration circuit forces one of the two simultaneous requesters into a waiting state.

BLOCK DIAGRAM ANALYSIS

- ROM Bank Array

  The ROM portion consists of five 24 k-byte banks, or pages, each occupying the controller address range 2000 to 7FFF. Each bank consists of three 8 k-byte ROM chips. Only one bank at a time is accessible to the controller.

  A valid controller address in the range 2000 to 7FFF during a read cycle selects a location in the currently active ROM bank. The data contained in that ROM location is returned over the controller data bus.

- Bank Select Register

  The active ROM bank is determined by the Bank Select Register, which can be changed by the controller.

- ROM Address Decoder

  The ROM Address Decoding receives address inputs from the controller and the Bank Select Register and generates the chip select signals for individual ROM chips.

- Shared RAM Array

  Shared RAM consists of up to fourteen 2 k-byte RAM chips (28K-bytes) occupying address range of 9000 to FFFF. The RAM chips are powered from the battery supply so the information stored within them is maintained while power is off.

- Shared RAM Address Decoder

  The RAM Address Decoder receives addresses from the controller or Advanced Math Assembly and generates the chip select signals for individual RAM chips.

- Shared RAM Bus Switch

  An attempt to read from or write to a memory location at any address

between 9000 and FFFF constitutes a "shared RAM access request." Requests are generated by the Advanced Math option and the Controller Assembly; only one of which is granted access. Simultaneous requests force one requester into a waiting state until the requester that was granted access relinquishes it.

A bus arbitration circuit grants access to shared RAM to either the Controller Assembly or the Advanced Math option, and resolves simultaneous access requests. Parts of this circuit reside on the Advanced Math option, Controller Assembly, and Memory Assembly. If the Advanced Math option is not installed, no bus arbitration is necessary and the remaining pieces on the Controller Assembly and Memory Assembly permanently assign access to the Controller Assembly.

The Controller Assembly has the option of asserting a priority line, which forces the arbitrator to grant access to it. This can have dire effects on any current access by the Advanced Math option; consequently, it is used only in order to survive abnormal operating conditions (for example, a non-functional Advanced Math option or a partially non-functional arbitrator.)

- Write Lockout Circuit

  The write lockout circuitry inhibits writing into RAM when the internal dc supplies are not at their proper levels.

CIRCUIT ANALYSIS

Bank Select Register

The Bank Select Register (U35) controls the activation of one of the five 24K-byte ROM banks accessible to the controller. When the ABS (Arm Bank Select) signal is high, any controller write cycle changes the contents of the Bank Select Register to the data present on the controller data bus lines CD0 to CD5. The ABS signal is driven by the controller, and is normally low except when the controller is selecting a different ROM bank to be the active bank.

ROM Bank Array

The ROM array, U2-U11 and U13-U17, is split into five banks; each bank consists of three 8 K-byte ROM chips. Bank selection is determined by the Bank Select register, while individual ROM selection within a bank is determined by controller address lines CA13 to CA15. Each ROM has two control inputs, CS(L) (Chip Select) and OE(L) (Output Enable). The ROM data outputs are enabled when both CS(L) and OE(L) are low. The data outputs are buffer back to the controller assembly through U18. The CS(L) input for each ROM is driven by an output of the ROM Address Decoder, while the OE(L) input is driven low to all ROM's when CRD(L) (controller read), MREQ(L) (memory request), and CA15 are all low.

Provision has been made for the assembly to accept 16 K-byte ROM chips in the same positions as the 8 K-byte chips. To accomplish this, one output from the Bank Select Register (Q3) drives address bit position A13 on the

ROM chips. On the 8 K-byte chips this is an unused connection; on the 16 K-byte chips it is an address connection. This effectively allows the assembly to have 10 banks with 24 K-bytes each if this becomes necessary in the future.

ROM Address Decoder

If the controller address lies between 2000 and 7FFF, the ROM Address Decoder (U28 pins 8, 9, 10; U44 8, 9, 10; U21; U22; and U29) selects (with the ROM CE(L) input) a unique ROM based on the contents of the Bank Select Register and controller address lines CA13 to CA15. The ROM selected for each valid combination is given in Table 3-7.

Shared RAM Array

The shared RAM array consists of a maximum of fourteen 2 K-byte RAM chips (U25, U26, U30, U31, U32, U38, U39, U40, U45, U46, U47, U50, U51, and U52) organized in a contiguous fashion between addresses 9000 and FFFF. The RAM is backed up by a battery which is located on the power supply assembly. The battery preserves RAM contents when main instrument power is turned off.

Each RAM chip is controlled by a CS(L) (Chip Select) input, an OE(L) (Output Enable) input, a WE(L) (Write Enable) input, and address lines S0 to S10. A unique RAM in the array is selected by the CS(L) input by the Shared RAM Address Decoder, while the OE(L) and WE(L) inputs of all RAM's are driven in parallel.

During a read cycle of shared RAM by either the Advanced Math option or the controller, the OE(L) input to all RAM's is low and the CS(L) input to one RAM is low. The contents of the cell within that RAM determined by address lines S0 to S10 is driven onto data lines XD0 to XD7.

During a write cycle, the WE(L) input to all RAM's is low and the CS(L) input to one RAM is low. The data present on data lines XD0 to XD7 is written into the location selected by address lines S0 to S10.

Table 3-7. ROM Usage

Bank Select Register Outputs			Controller Address Lines			ROM Selected	
Q2 pin 2	Q1 pin 5	Q0 pin 7	CA15	CA14	CA13		
0	0	0	0	0	1	U2	
0	0	0	0	1	0	U7	Bank 0
0	0	0	0	0	1	U13	
0	0	1	0	0	1	U3	
0	0	1	0	1	0	U8	Bank 1
0	0	1	0	0	1	U14	
0	1	0	0	0	1	U4	
0	1	0	0	1	0	U9	Bank 2
0	1	0	0	0	1	U15	
0	1	1	0	0	1	U5	
0	1	1	0	1	0	U10	Bank 3
0	1	1	0	0	1	U16	
1	0	0	0	0	1	U6	
1	0	0	0	1	0	U11	Bank 4
1	0	0	0	0	1	U17	

Shared RAM Address Decoder

If the address output by the Shared RAM Bus Switch lies between 9000 and FFFF, the Shared RAM Address Decoder (U44- pins 1, 2, 3; U42; and U49) selects (with the RAM CS(L) input) a unique RAM based on address lines S11 to S15. The RAM selected for each valid address line combination is given in Table 3-8.

When instrument power is turned off, the chip select outputs of the decoder are isolated from the instrument by transistors Q2 to Q15 in order to prevent current leakage from the battery-back-up supply. In addition, the chip select outputs are pulled up through 560 ohm resistors to the battery supply, which minimizes RAM chip power consumption.

Table 3-8. RAM Usage

Shared Address Lines					Selected RAM	Active Chip Select
S15	S14	S13	S12	S11		
1	0	0	1	0	U25	CS2(L)
1	0	0	1	1	U26	CS3(L)
1	0	1	0	0	U30	CS4(L)
1	0	1	0	1	U31	CS5(L)
1	0	1	1	0	U32	CS6(L)
1	0	1	1	1	U38	CS7(L)
1	1	0	0	0	U39	CS8(L)
1	1	0	0	1	U40	CS9(L)
1	1	0	1	0	U45	CS10(L)
1	1	0	1	1	U46	CS11(L)
1	1	1	0	0	U47	CS12(L)
1	1	1	0	1	U50	CS13(L)
1	1	1	1	0	U51	CS14(L)
1	1	1	1	1	U52	CS15(L)

Shared RAM Bus Switch

The COB (controller on bus) output of the shared RAM arbitrator (located primarily on the Advanced Math option) controls the Shared RAM Bus Switch. This switch routes either the math or controller memory signals (address lines, data lines, write control signal, and read control signal) to the Shared RAM Array, the Shared RAM Address Decoder, and the Write Lockout Circuit. The data lines are switched by a pair of tri-state octal transceivers (U27, U33). The address lines are switched by a set of two-to-one data selectors (U36, U41, U43, U48). The write signal is switched by a pair of tri-state gates (U37 pins 2, 3, 9, 8), and the read signal is switched by another pair of tri-state gates (U37 pins 12, 11, 5, 6).

Write Lockout Circuit

When instrument power is off, the WE(L) input to all RAM chips (BWR(L)) is isolated by Q1 from the Shared RAM Bus Switch. The BWR(L) signal is pulled up to the battery supply by a 470 ohm resistor for further protection while power is off.

Display

FUNCTIONAL DESCRIPTION

The Data Logger display board communicates with the controller over the device bus. Its three functions include controlling the vacuum Fluorescent display, controlling the beeper, and scanning the keyboard to detect key entries. These three functions are accomplished by nine separate circuit sections:

- PIO Interface
- Microprocessor
- Keyboard Control
- Beeper
- Power Supply
- Display I/O
- Dot Select Logic
- Character Select Logic
- Vacuum Fluorescent Display Tube

Figure 3-20, the Display Assembly Block Diagram, shows how the nine blocks of the display assembly work together. A brief description of each block follows in the block diagram analysis.

BLOCK DIAGRAM ANALYSIS

- PIO Interface

  The PIO interface is a parallel interface through which all communication with the system controller occurs. In addition to the eight-bit bus through which all data is transferred, eleven lines are used to control the exchange of data. Two of these provide the board address, two define the type of transaction which is to occur, four allow for handshaking, one is an interrupt line, one is a reset line, and one is a busy line.

- Microprocessor

  The microprocessor on the display assembly is a high speed 8749. This enables display refresh operations to be done entirely through software, while also handling all other communication and control.

- Keyboard Control

  This circuitry is used by the microprocessor to control the front panel LED's and interrogate the keyboard to determine if any keys have been pressed. Sets of lines are sent to the keyboard to strobe the keys, to read back the state of the keys, and to turn on the LED's.

- Beeper

  The beeper circuitry generates the audio tone that is emitted during keyboard entries.

o Display Power Supply

The display power develops +55 volts DC and 8.9 volts AC from the mainframe +24 volts, with the supply drive logic running on +5 volts. The power supply drive signals are derived from the microprocessor generated address latch enable (ALE) signal.

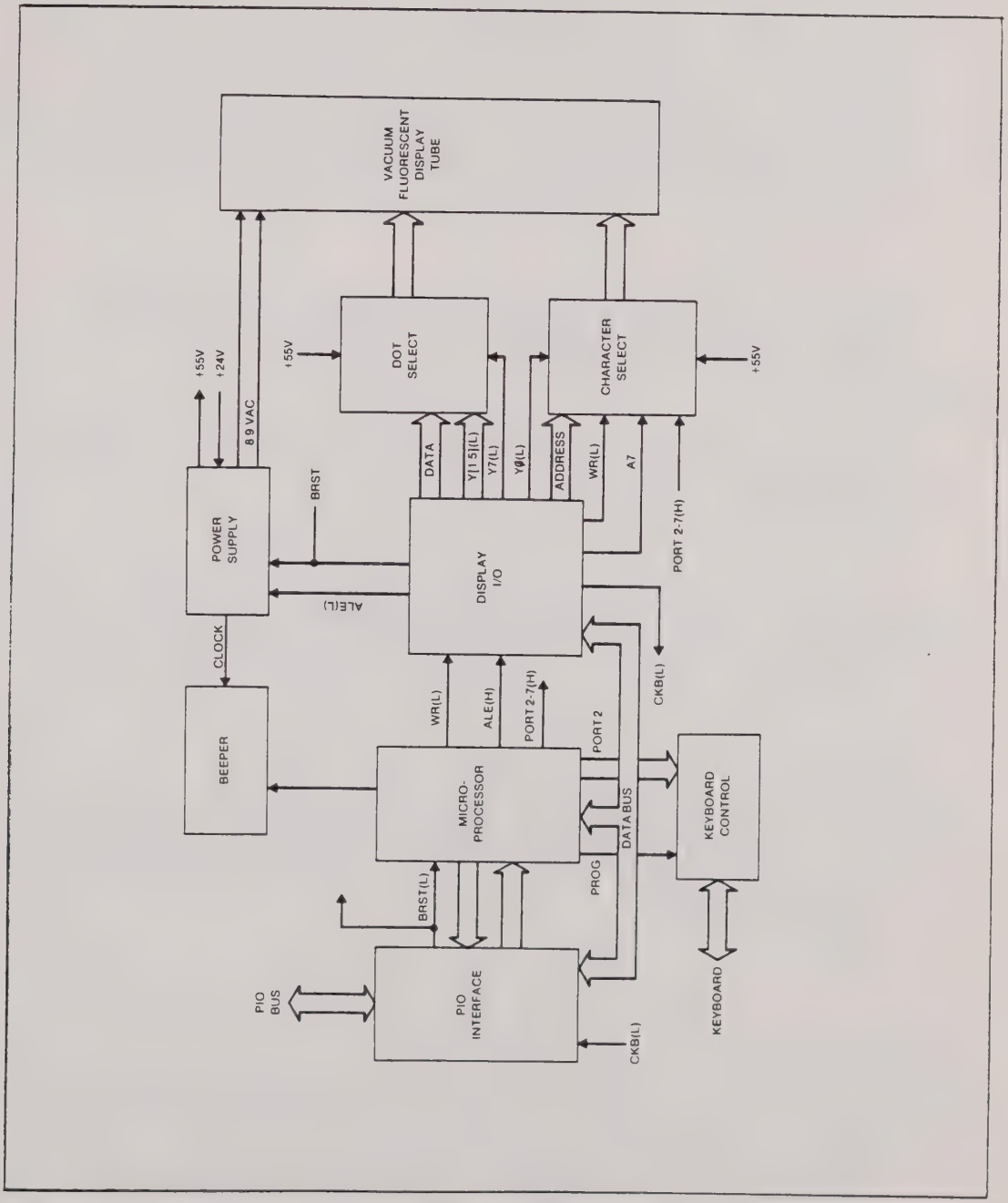


Figure 3-20. Display Assembly Block Diagram

- Display I/O

  This section of circuitry controls the flow of addresses and data to and from the microprocessor. Included are buffers for the data bus lines, and address latches and decoders.

- Dot Select

  The dot select logic is used to excite the appropriate dots within a selected character in the vacuum Fluorescent display.

- Character Select

  The character select logic is used to select and drive one of the 40 characters in the display.

- Vacuum Fluorescent Display Tube

  The vacuum tube contains 40 characters made up of 5 by 7 dot matrices, where each character is selectable. The dots of the characters are wired in parallel.

CIRCUIT ANALYSIS

The following analyses are based on the simplified schematic diagram for the display board, Figure 3-xx.

PIO Interface

Control lines IC5, IC6, RDRDY(H), and WRRDY(H) are terminated with series resistors in Z3, buffered by U25, and read directly by the processor through port 1. When both address lines IA0 and IA1 are driven low by the controller board through Z4, U23 asserts ADDRESSED(L), enabling the tri-state buffers of U24 to output processor-generated signals RDSTB(L), WRSTB(L), and BUSY(H). Mainframe signal BRST(L), which is pulled up and terminated by Z4, drives U25 and U28, holding the display board logic in a reset state until BRST(L) is released by the controller board. Data is sent out on the PIO bus by first clocking and latching it into U30 with CKB(L) from U5, and then enabling its tri-state outputs with U23. U30 is enabled onto the PIO bus when ADDRESSED(L) is asserted, and port 2-5 of U22 is low. Incoming data is read from the PIO bus through Z6 and Z7 when U29 is enabled by READ(L).

Microprocessor

The 8749, U22, has onboard EPROM and RAM, and uses an 11 MHz crystal. Port 1 is used for PIO bus communication, while port 2 controls the beeper, keyboard communication, character selection, and PIO communication. The processor is placed in reset mode when BRST is asserted, and processor-generated signals ALE, READ, and WRITE are all utilized to implement display board operations.

Keyboard Control

Communication with the keyboard assembly is managed by U36, an I/O expander IC. Four outputs of U36 are decoded by U35 to set 1 of 16 lines low. By monitoring the four row read lines while strobing the 16 columns, keys on the 16 by 4 matrix keyboard that have been pushed can be identified. The I/O expander also controls LED driver U34, which drives the keyboard LED's through current setting resistors R14 to R19.

Beeper

Flip-flop U26 takes a 5.72 kHz clock generated by U33 from ALE, and divides it by two whenever port 2-6 of U22 is low. The output of U26 turns FET switch Q1 on and off, driving the electro-magnetic beeper LS1. R2 sets the output volume, R1 limits the current through LS1, and CR4 protects Q1 from voltage spikes on turn-off.

Display Power Supply

The power supply drive signals are derived from the 733 kHz ALE. This is divided down by U31 when it ANDs three outputs of counter U33 together to produce a 91.7 kHz, 1/8-duty-cycle clock. The resulting output toggles flip flop U26, and is also ANDed with the outputs of the flip flop by U31 to generate the bi-phase, non-overlapping, 7/16 duty cycle signal used to alternately drive Q2 and Q3. If BRST is asserted, U31 keeps Q2 and Q3 off. These transistors drive each end of a center-tapped winding in T1, whose center-tap is tied to +24 volts through fuse F1. One secondary output of T1 is full-wave rectified by CR1, CR2 and C2 to produce +55 volts dc for the display anodes and grids, while the other secondary winding of the transformer generates 8.9 volts ac for the display filaments. The filament supply is biased at a +10 volt dc potential by CR3 and R3, allowing the display tube drivers to pull the anodes and grids to 10 volts below the filament dc voltage, thereby turning the display fully off.

Display I/O

Since the 8749 uses a multiplexed address and data bus for external I/O transactions, U4, the address latch, holds the address. The ALE signal of the microprocessor clocks the address into U4. The most significant bit of address latch U4, A7, in combination with the WRITE(L) line enables either the I/O address decoder U5 or the character select latches. The Y1 to Y5 outputs of address decoder U5 clock and latch dot information into the dot latches, while Y6 clocks data into PIO bus latch U30, Y7 clears all dot latches, and Y0 clears the character select latches.

Dot Select Circuitry

To light up a selected character, +55 volts must be applied to the anode of each dot in the 5 by 7 pattern desired. To select the dots, five bytes, each containing information for seven dots, are clocked out to dot latches U8, U9, U10, U13, and U14. The outputs of these latches control dot drivers U1, U2, U3, U6, and U7 respectively, which convert the TTL-level inputs to 0 or +55 volts to drive the 35 display anodes.

Character Select Circuitry

Character selection is performed by a set of addressable latches and high-voltage drivers which drive the grid of the one character of 40 desired. Each grid is selected by the six bit address that corresponds to the number of the grid desired. The upper three bits are sent to U12, which acts as a data steering decoder, sending the data bit received from port 2-7 of the microprocessor on to latch U18, U19, U27, U32, or U37, depending on the address. The lower three bits plus the data bit are latched into the character select latches by U23, which looks at A7 and WRITE. In this way, a high bit is steered from port 2-7 to one of five latches, of which one output of 8 is chosen by the lower three address bits, and one output is enabled. This output allows one of the 40 drivers in U15, U16, U17, U20, or U21, to drive the desired character grid to +55 volts. The character is cleared when Y0 of U5 clears the character select latches.

DISPLAY REFRESH CYCLE

The display of all 40 characters is refreshed every 10 milliseconds, giving a 100 Hz refresh rate per character. Within one character refresh cycle, the following events take place:

1. Dot information for the character to be refreshed is fetched from data memory.

2. Y7 of U5 is pulsed to clear the previous dot data from the five dot latches.

3. Y0 of U5 is pulsed to clear the five character select latches.

4. The address of the character to be enabled is written out, with port 2-7 held low to prevent selecting a grid driver, and thereby prevent "ghosting" of the display.

5. Five bytes of dot information are latched out into the dot latches using Y1 to Y5 of U5 to clock in the data.

6. The address of the character grid to be enabled is written out, this time with port 2-7 high, so that the character lignts up.

7. The character is left on until the next character is refreshed.

Vacuum Fluorescent Display Tube

The display consists of 40 characters, each a 5 by 7 dot matrix. Filament wires, which run the length of the display tube carry an ac voltage that boils off electrons. A character is selected by taking one of 40 grids to a +55 volt level, causing electrons to accelerate through the selected grid. These electrons then strike the individual dots or anodes which have been set to +55 volts, causing their phosphorescent material to emit light. Since the anodes of each character are in parallel, the characters must be multiplexed, as described in the previous sections.

Printer

FUNCTIONAL DESCRIPTION

The Data Logger printer is 40-column thermal printer with automatic paper takeup. Two assemblies control the printer: the Printer Interface Assembly and the Printer Driver Assembly. The Printer Interface Assembly receives the information to be printed from the controller assembly over the PIO Bus. The two assemblies together control all aspects of printing, including: enabling power to the printer motor, formatting and assembling individual rows of dots to be printed, enabling drive current to the thermal printhead elements, sensing operator switches to feed paper and disable the paper takeup, and communicate out of paper conditions to the controller assembly. These functions are accomplished by the major circuit blocks shown in Figure 3-21, the Printer Block Diagram, and discussed in the following paragraphs.

BLOCK DIAGRAM ANALYSIS

- Microprocessor and ROM

  The microprocessor on the Printer Interface assembly is an 8039 running at a frequency of 6 MHz. The microprocessor's program is stored in a 2 K-byte EPROM. This EPROM also contains the dot-matrix character generation tables.

- PIO Bus Interface

  The PIO Bus is a parallel interface through which all communication with the controller assembly takes place. In addition to the eight-bit bus to transfer data, there are two lines that address the assembly, two lines that identify the type of bus transaction, one interrupt line, and a few handshake signals.

- Power Supply Arbitration Logic

  To reduce the power consumption of the instrument, the printer is not allowed to print while the cartridge tape option is in operation. This logic allows the printer and cartridge tape subsystems to coordinate usage of the power supply.

- Printer Mechanism

  A dot-matrix thermal printer mechanism is used in the Data Logger. A dot is printed on the thermal sensitive paper when a resistive element in contact with the paper heats up. The printer has 40 such thermal elements, each responsible for printing all the dots for one character, one dot at a time. The thermal printing elements are mounted on a mobile print head which is moved back and forth over the paper by an eccentric cam attached to the printer motor shaft.

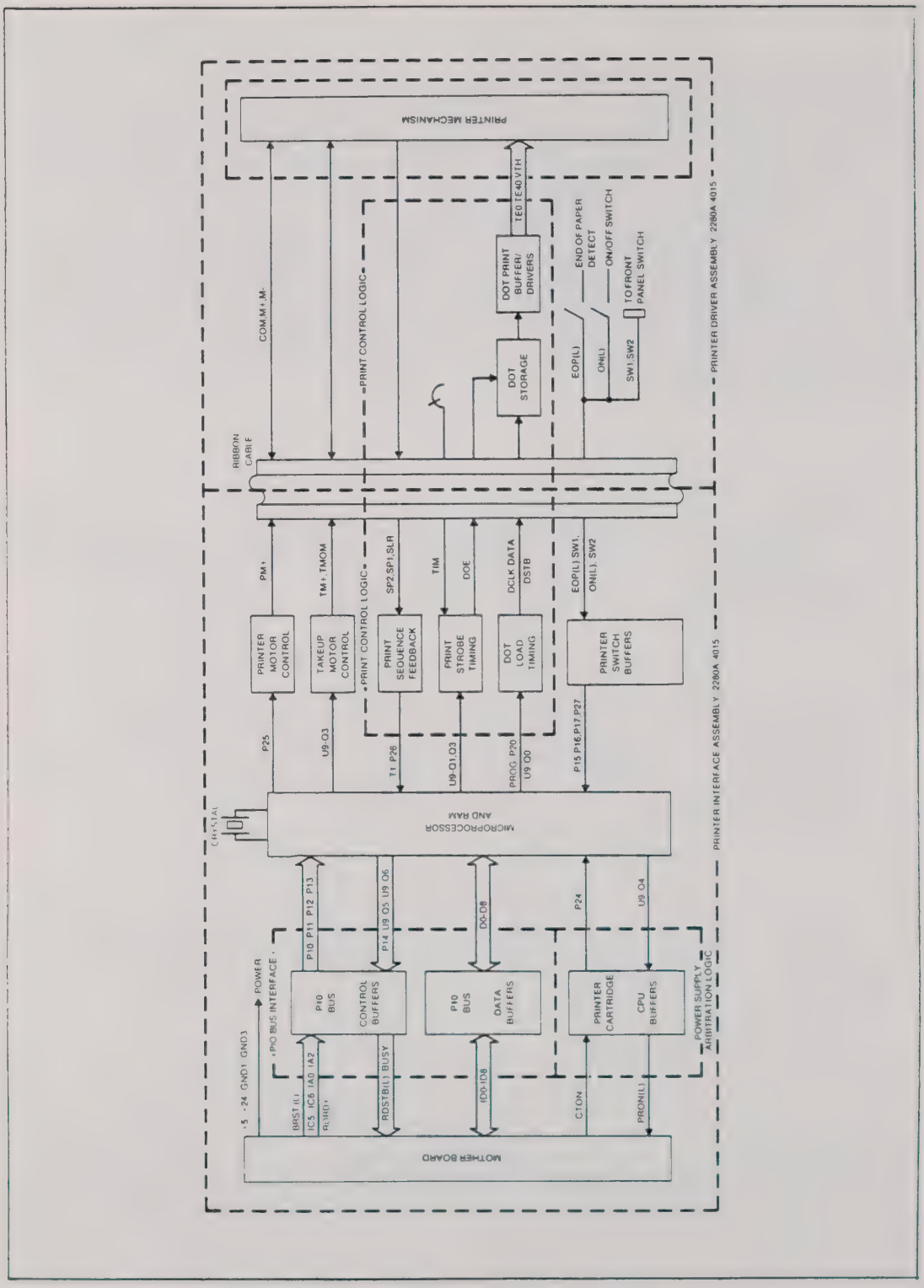


Figure 3-21. Printer Block Diagram

- Printer Control Logic

  This logic provides the timing and synchronization required to receive printhead location information from the printer mechanism and in turn generate the signals to enable and time the current drive to the thermal print elements.

- Printer Motor Control

  The printer motor speed is important to achieve good print quality. An adjustable voltage regulation circuit allows the assembly to accommodate the mechanical variations in printer mechanisms. This circuitry also allows the microprocessor to turn the motor off and on.

- Take-up Motor

  A simple motor driven take-up spool is provided to store printed paper for later reading. This take-up motor can be disabled by a front panel switch thereby allowing the user to pull out and review printouts. When the take-up motor is enabled, the paper will automatically be stored on the take-up spool.

- User Interface Switches

  A single multi-position front panel switch allows the operator to enable and disable the paper take-up and advance the paper.

  A switch mounted on the Printer Interface assembly (behind the front panel of the Data Logger) causes a test pattern to be printed. This is used when making intensity or timing adjustments.

- Out Of Paper Detect

  A switch mounted in the path of the paper allows the microprocessor to detect out of paper conditions and report them to the controller assembly and in turn inform the operator.

DETAILED CIRCUIT ANALYSIS

Microprocessor and ROM

The 8039 microprocessor (U6) executes instructions and reads character generation data from EPROM (U8). The lower eight bits of the address to the EPROM is captured in an octal latch (U7) by signal ALE (Address Latch Enable) and the EPROM data is read when the processor generates PSEN (Program Store Enable).

The microprocessor contains two 8-bit input/output ports, referred to in this circuit analysis as p1 and p2. The lower 3 bits of p2 (p2 bits 0, 1 and 2) provide the most significant address lines to EPROM (U8). The remainder of the lines have dedicated purposes, either as status lines read by the processor, or control signals output from it. There are also two input lines, T0 and T1, and an output line PROG, that have dedicated purposes.

There is also an 8-bit addressable latch (U9) containing more control signals. The value of a bit is changed with a pulse on WR(L). As the pulse occurs, data bits DB1 to DB3 select which bit to change, and DB0 gives its new value.

Table 3-9 summarizes the control and status lines and what they do. Capitalized names appear on the schematic; those in lower case are provided for clarity.

Table 3-9. Printer Control and Status Lines

LINE	IN/OUT	NAME	WHERE DESCRIBED
P1-0	IN	IC5	Device Bus Interface
P1-1	In	IC6	Device Bus Interface
P1-2	In	RDRDY	Device Bus Interface
P1-3	In	Addressed	Device Bus Interface
P1-4	Out	PTRINT (L)	Device Bus Interface
P1-5	In	SW1 (L)	User Interface Switches
P1-6	In	SW2 (L)	User Interface Switches
P1-7	In	ON/OFF	User Interface Switches
P2-0	Out	A8	User Interface Switches
P2-1	Out	A9	User Interface Switches
P2-2	Out	A10	User Interface Switches
P2-3	Unused		
P2-4	In	CTON	Communication With Cartridge Bd.
P2-5	Out	Motor On	Printer Motor Control
P2-6	In	Latch	Printer Operation
P2-7	In	EOP (L)	End of Paper Detect
T0	In	Test Switch	Self Test
T1	In	sp1/sp2	Printer Operation
INT	In	Doe Held Off	Printer Operation
PROG	Out	DCLK (L)	Printer Operation
U9,Q0	Out	DSTB	Printer Operation
U9,Q1	Out	Start Doe	Printer Operation
U9,Q2	Out	Out of Doe	Printer Operation
U9.Q3	Out	TMON	Take Up Motor
U9,Q4	Out	PRON	Communication With Cartridge Bd.
U9,Q5	Out	RDSTB (L)	Device Bus Interface
U9,Q6	Out	BUSY	Device Bus Interface
U9,Q7	Unused		

PIO Bus Interface

Unlike all other logging and interface assemblies that communicate with the Controller Assembly using the PIO Bus, the printer only receives information from the controller; it cannot send information to the controller. The control lines IC5, IC6 (Interface Control), and RDRDY (Read Ready) are read through buffers by the microprocessor at p1 bits 0, and 2. When address lines IA0 and IA2 (Interface Address) are simultaneously driven low by the controller, p1-3 goes to a logic zero, enabling the tri-state buffers (U5, pins 11 and 13) for BUSY and RDSTB(L) (Read Strobe) onto the PIO Bus. Signals BUSY and RDSTB(L) are set by U9,Q6 and U9,Q5. Signal PTRINT(L) (Printer Interrupt), driven by p1 bit 4, is asserted whenever BUSY is changed from a logic one to a logic zero, or when the printer runs out of paper (see heading Out of Paper Detect).

Data is accepted from the PIO Bus when the processor asserts RD(L) (Read), enabling data from the PIO Bus onto the internal data bus (drivers U5 and U12).

Power Supply Arbitration Logic

To reduce maximum power consumption, the printer does not print while the cartridge drive is in operation. The PRON (Printer On) and CTON (Cartridge On) signals are used by the two devices to make this possible. PRON is generated by the printer interface board (U9,Q4) and CTON is generated by the cartridge interface board (read at p2 bit 4).

If the printer is ready to print a line, it waits for CTON to be retracted before proceeding. Once CTON is low, the printer asserts PRON high and checks CTON again, just in case the cartridge asserted it while the printer was asserting PRON. If CTON is now asserted, the printer retracts PRON and waits again; otherwise, the printer prints the line.

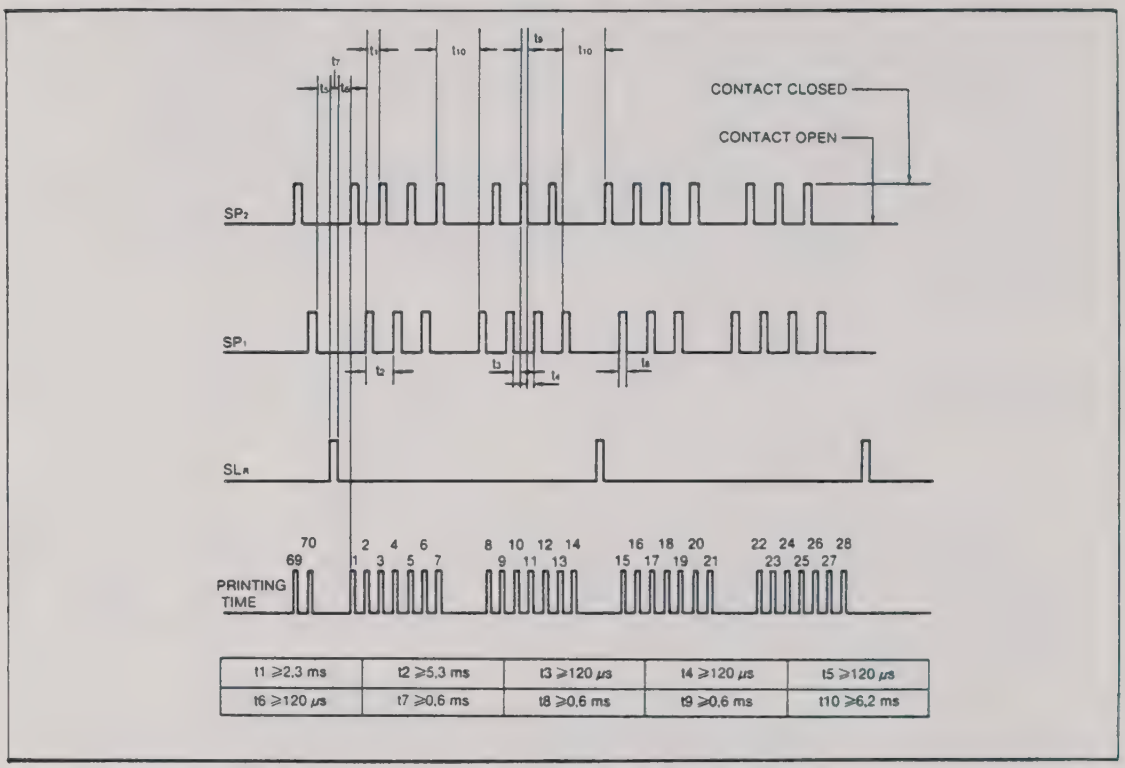
When it is ready to run the tape drive motor, the cartridge asserts CTON and waits for PRON to go low. This handshake scheme gives the cartridge priority over the printer.

Printer Mechanism

The printer used by the Data Logger is a dot-matrix thermal printer.

Signals SLR, SP1, and SP2 are generated by the printer to inform the control logic of the printhead location. The microprocessor uses these signals to synchronize current to the resistive thermal elements with the print head position. Signal SLR occurs when the print head is at its rightmost position. Signals SP1 and SP2 then take turns indicating when it is time to print another dot. There are seven dot positions per row. Signal SP2 occurs first on a right-to-left sweep of the print head; SP1 occurs first in the other direction.

Figure 3-22 shows the timing relationship of signals SLR, SP1, and SP2. The graphic representation of SLR can be used as a scale for the other signals. Pulses of signal SLR occur approximately 55 milliseconds apart when the printer is properly calibrated.



t1 ≥2,3 ms	t2 ≥5,3 ms	t3 ≥120 µs	t4 ≥120 µs	t5 ≥120 µs
t6 ≥120 µs	t7 ≥0,6 ms	t8 ≥0,6 ms	t9 ≥0,6 ms	t10 ≥6,2 ms

Figure 3-22. Printer Pulse Timing Relationships

The print head position signals are first debounced by flip-flops (U10) clocked by the ALE signal from the processor (400 kHz), then read by the processor. The debounced SLR is read at p2 pin 6. Signals SP1 and SP2 toggle a J-K flip-flop, read at T1 which goes high when SP1 occurs, and low when SP2 occurs. The flip-flop maintains its previous state when either signal is retracted. Dots are printed in the order represented in Figure 3-23.

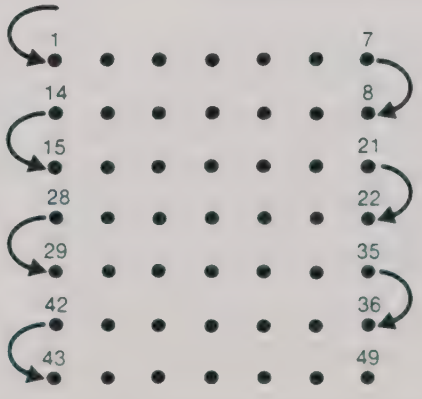


Figure 3-23. Sequence for Dot Printing

Printer Control Logic

All information required for forming characters and symbols is stored in the EPROM, as is the control program for the 8039 microprocessor. Dot data for the next 40 dots to be printed (one for each element) is clocked serially to the dot registers on the driver board by pulses on DCLK (Data Clock) which is derived from the PROG line from the processor. The next dot to be clocked is presented on p2 bit 0. The D flip-flop (U4) on the interface board adds an additional serial stage to the data train to the driver board. In this manner, 41 pulses are required to load the 40 dots into the registers.

After the data has been clocked out in this fashion, a pulse on DSTB (Data Strobe) (U9, Q0) moves the data from the serial portion of the dot registers (U2, U3, U5, U6, and U7 on the Printer Driver Assembly) to their outputs. A positive pulse on DOE (Data Output Enable) takes the registers out of tri-state, causing a row of dots to be printed. Each dot register is coupled to a thermal element through a Darlington-transistor driver (U1, U4, U8, U9, U10, and U11 on the Printer Driver Board) that provides the current necessary to turn on the element. A logic one causes a dot to be printed. Each thermal element has a series resistor to reduce the effect of thermal element resistance on the darkness of the dots in one character position.

A pulse of DOE is initiated by a pulse on U9 and Q1. If R16 is placed at R16A, DOE is held off for the pulse width of a one-shot (U11, pins 1 to 6), that is controlled by potentiometer R13. Placing R16 in the other position, R16B, disables this hold-off entirely by removing this one-shot from the circuit. This hold-off allows adjustment of the alignment of consecutive rows of dots. The adjustment of R13 is required because of variations in the cam-and-spring arrangement that moves the print head back and forth.

After the one-shot has timed out (or immediately if R16 is placed at R16B) a second one-shot (U11, pins 10 to 15) fires, asserting DOE. The darkness of the printing is determined by the length of DOE, which can be varied by potentiometer R5 on the driver board. The processor limits the pulse width to a maximum of 1.7 milliseconds by forcing the DOE one-shot to the reset state (U9, Q2). The INT (Interrupt) input to the microprocessor indicates that DOE has started by changing to a logic zero state, enabling the processor to accurately gauge the length of DOE. A DOE pulse width of greater than 1.7 milliseconds exceeds a safe operation specification for the thermal elements.

Printer Motor Control

The printer motor is controlled by the voltage regulation network consisting of Q1 to 3, R3 to 5, R10 to 12, CR1 and CR2, and C11. A logic one at p2 bit 5 turns the motor on, and a logic zero turns it off. When p2 bit 5 is turned off, Q1 acts as a brake by drawing current from the motor at PM+ (J15,18). Potentiometer R11 adjusts the motor voltage, and thus the speed of printing. The motor voltage has an adjustment range 12 to 19.5 volts.

The motor speed has an effect on the alignment of printing because of the dynamic response of the print head moving assembly. That is why the adjustment procedure in Section 4 specifies that R11 be set for the proper value before R13 is adjusted.

Take-up Motor

The printer take-up motor is controlled by TMON (U9,Q3) (Take-up Motor On). A logic one turns the motor on by turning on a Darlington transistor (U11, pin 6,11) on the driver board.

User Interface Switches

Two user-interface switches are mounted on the printer assembly. One is mounted on the printer front panel; the other is mounted on the printer driver board.

The front panel switch has three positions labeled TAKE-UP OFF, TAKE-UP ON, and PAPER ADVANCE. When the switch is in the first position, the take-up motor is turned off. In the other two positions, the take-up motor is turned on. The paper-advance position is a momentary-contact position that causes the paper to advance smoothly in increments equal to the height of a printed line. The position of the switch is indicated on the schematic by the lines SW1 and SW2 (J15, 16, and 10).

The switch mounted on the printer driver board is the printer on/off switch. When the switch is in the off position, only the paper-advance function works. While the printer is off, anything that would ordinarily be printed is discarded. The position of this switch is indicated on the schematic as ON/OFF (J15,19).

The printer self-test switch S1 is monitored by processor signal TO. When the printer self-test switch is pushed in, the printer enters the self-test mode. In the self-test mode, the printer prints a test pattern consisting of full rows of the capital letter "I". Pushing the switch again causes the printer to exit the self-test mode and stop printing the test pattern. The printer user-interface switches retain their usual function while the printer is in the self-test mode.

Out Of Paper Detect

A microswitch mounted on the driver board detects the presence of paper feeding the printer. Signal EOP(L) (End of Paper) reflects the status of this switch, assuming a value of logic zero when the printer is out of paper. If this switch is in the "up" position, the printer signals the controller of the condition by driving the PTRINT (Printer Interrupt) line low and the BUSY line high. The controller acknowledges the lack of paper by addressing the printer to write to the controller. When this is done, the PTRINT line is retracted. All subsequent lines to be printed are discarded and all printer activity ceases until a new roll of paper has been loaded.

Details Of Interprocessor Communication

The flow of communication between the Data Logger mainframe assemblies is accomplished through two bus structures: the PIO Bus and the Serial Link Bus. These two busses are described in the overview below. Refer to the Data Logger Mainframe Block Diagram, Figures 3-1.

PIO BUS

The PIO bus is one of the three busses in the Data Logger. The other two are the serial link and shared memory busses. The PIO bus is an 8-bit parallel bus that carries interprocessor messages between the controller and the primary data input/output devices and interfaces of the Data Logger. The primary I/O devices are the keyboard/display, printer, Option 2280A-214 Cartridge Tape Drive, and the remote interfaces.

Two slots for the remote interfaces (either the RS-232-C or IEEE-488) are in the rear of the Data Logger, one of which can be used to externally program and remotely operate the Data Logger. These slots are referred to as Port A (the remote control port) and Port B (the output only port), respectively.

The logic portion of the PIO bus is controlled by a Z80-PI/O interface chip resident on the controller. The device interfaces to the bus are similar, but not identical, to each other and involve a mix of gating, buffered logic and connections to the microprocessors involved. Table 3-10 lists the pin assignments of the card-edge connectors.

(NC) signifies that a line is not used globally. Some of these lines are used on a local basis. For instance, the CTON and PRONB lines which run between the cartridge tape and the printer utilize 2 of these pins.

SHLD is the shield line for the bus.

Power Supplies

Pins 1 through 14 of the connectors (J3, J4, J5, J9, J10A, and J10B) are power supplies for devices on the bus.

Line +5 uses GND1 as a reference and provides power for all digital logic for the devices. Lines +24 and -12 use GND 3 as a reference and provide power for interface hardware such as RS-232-C drivers, printer thermal elements and take-up motor and the vacuum Fluorescent display. Line +5b provides power to the non-volatile RAM on the memory card and is not used much, if at all, on the PIO bus.

Logic Signals

All lines on the bus that aren't power supplies are TTL level logic lines. They are driven and buffered by MOS and CMOS devices. All of these lines are pulled up to +5V through resistors on the controller board. Table 3-11 describes each of the logic signals on the PIO bus.

Table 3-10. Pin Assignments for Connectors J3, J4, J5, J9, J10A, and J10B

PIN	NAME	PIN	NAME
1	+24	2	+24
3	GND3	4	GND3
5	+5	6	+5
7	GND1	8	GND1
9	GND1	10	GND1
11	+5B	12	+5B
13	-12	14	-12
15	NC	16	NC
17	NC	18	NC
19	IA0	20	IA1
21	IA2	22	IA3
23	IA4	24	BUSY
25	IC5	26	IC6
27	SHLD	28	KBINT(L)
29	ID0	30	ID1
31	ID2	32	ID3
33	ID4	34	ID5
35	ID6	36	ID7
37	RDRDY	38	RDSTB(L)
39	WRRDY	40	WRSTB(L)
41	PTRINT(L)	42	TPINT(L)
43	ORMINT(L)	44	1RMINT(L)

Table 3-11. PIO Bus Signal Lines

SIGNAL NAME	DIRECTION	FUNCTION
POR1(L)	To devices From controller	When low, forces all devices to their power-up state.
IA0-IA4	To devices From controller	These signals specify which device is talking with the controller. A 2-of-5 negative encoding scheme is used for choosing device addresses.
BUSY	To controller From devices	A high value on this line indicates the device addressed is busy and unable to receive any messages from the controller.
IC5,IC6	To devices	These lines specify the nature of the transaction taking place between the controller and the addressed device, as specified below. IC6 IC5 TRANSACTION 0 0 DEVICE QUIET 0 1 DEVICE WRITE 1 0 DEVICE READ 1 1 DEVICE POLL Device quiet instructs the device not to assert its interrupt line until instructed otherwise. Device write and device read specify a data transfer, the direction of which is denoted from the device's viewpoint. Device poll does nothing but cause the addressed device to gate its BUSY line onto the bus.

Table 3-11. PIO Bus Signal Lines, cont.

SIGNAL NAME	DIRECTION	FUNCTION
KBINT(L)	Display to controller	Each device has its own interrupt line. A TTL low voltage on a device interrupt line indicates that the device has a message to send to the controller. This can be suppressed by the controller as indicated in the IC5, IC6 description above.
PRTINT(L)	Printer to controller	
TPINT(L)	Cartridge tape to controller	see entry above
ORMINT(L)	Port A to controller	see entry above
1RMINT(L)	Port B to controller	see entry above
ID0-ID7	Bi-directional between devices and controller	This is where the 8 bits of data go when they are transferred between the devices and the controller.
RDRDY	Controller to device	These lines provide a handshake facility for the transfer of data over the bus. See the timing diagrams provided for a clearer idea of how this handshake works. Basically, RDRDY indicates the controller has a byte for the device to read and the RDSTB reads it; WRRDY indicates the controller can hold a byte sent by the device and WRSTB sends it.
RDSTB(L)	Device to controller	
WRRDY	Controller to device	
WRSTB(L)	Device to controller	

SERIAL LINK

Hardware

The serial link connects the 2280 Series mainframe CPU assembly with all remote interface options, A/D Converters, digital I/O options, and analog I/O options in the Data Logger system. In this theory of operation discussion, the mainframe CPU is called the serial link controller and the data acquisition and control options are collectively called devices.

The serial link translates TTL-level signals from the controller into RS-422 signals for communication with the devices. The RS-422 signals are sent and received over two twisted pairs of conductors. On one pair, the controller transmits while all devices listen. On the other pair, a device selected by the controller can transmit characters to the controller, but never to other devices.

Devices on the serial link may be physically located inside the Data Logger or in an extender chassis. The serial link is routed through each device in such a way that if power is removed from any of them, communication through the link remains unbroken. The controller is equipped with a real-time interrupt having a resolution of 31 ms. The devices have no sense of elapsed time.

General Protocol

This description deals only with the elements of the serial link protocol which are device independent. Because of the diversity of devices, this covers the most basic protocol.

Information is sent over the serial link bit-serially in the form of ASCII characters at a rate of 25K-baud. Each character consists of:

1 Start Bit
8 information bits
1 odd parity bit
1 stop bit

When the controller sends a message, the addressed device replies with (depending on the message type) either an acknowledgement or a response message. A device never initiates an exchange.

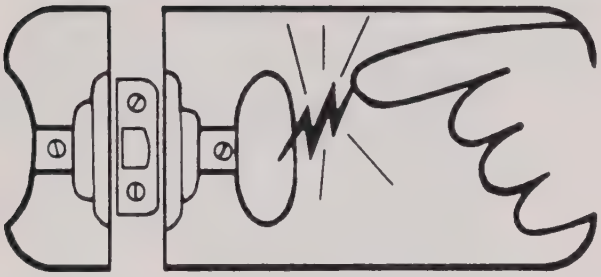
A message is sent in one or more groups. The group is the basic protocol unit and consists of four characters: three information characters followed by a check character. Some controller messages require the device to reply with an acknowledgement. The acknowledgement is a single character and can have one of only two values: ready (hex 3C), and not ready (hex C3)

Although the serial link is protected against occasional errors in transmission by a two-stage error recovery system. The check bits (character parity and longitudinal parity) first detect an error. The protocol then recovers by repeating the transmission.

static awareness

A Message From

John Fluke Mfg. Co., Inc.

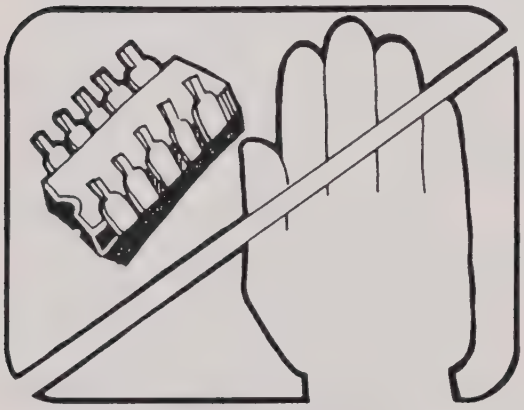


Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

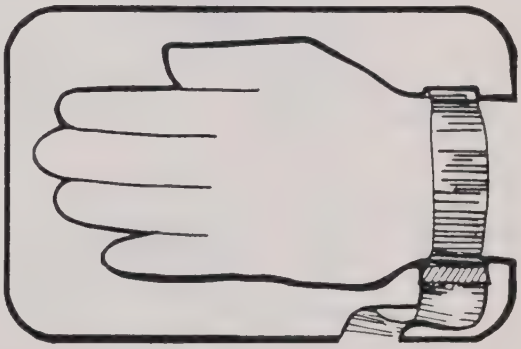
1. Knowing that there is a problem.
2. Learning the guidelines for handling them.
3. Using the procedures, and packaging and bench techniques that are recommended.

The Static Sensitive (S.S.) devices are identified in the Fluke technical manual parts list with the symbol "⊗"

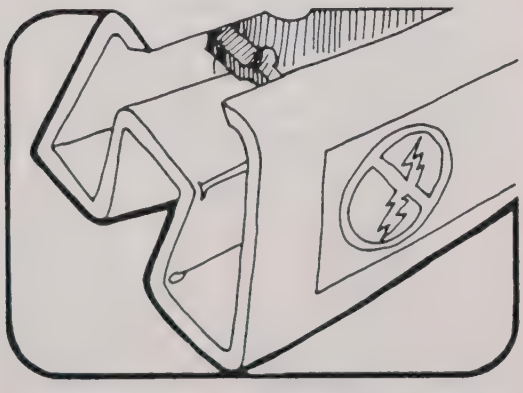
The following practices should be followed to minimize damage to S.S. devices.



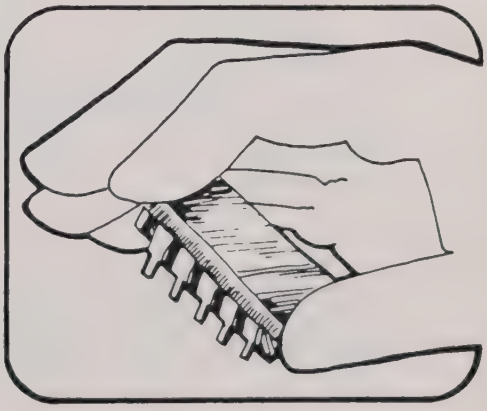
1. MINIMIZE HANDLING



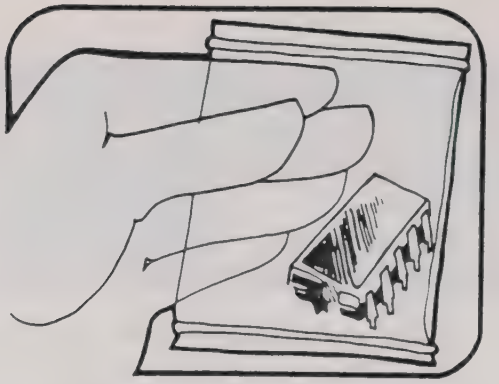
3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES



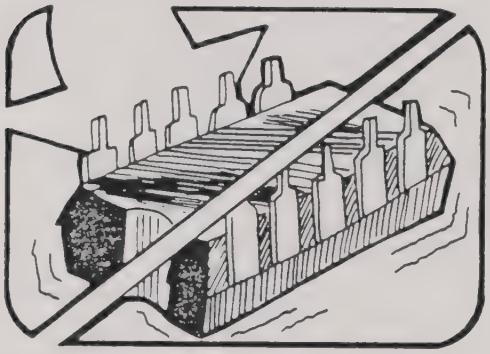
2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



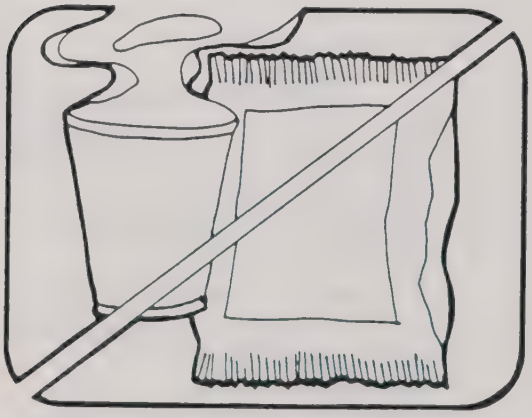
4. HANDLE S.S. DEVICES BY THE BODY



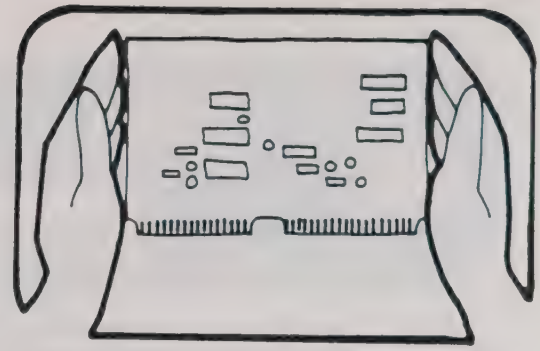
5. USE ANTI-STATIC CONTAINERS FOR HANDLING AND TRANSPORT



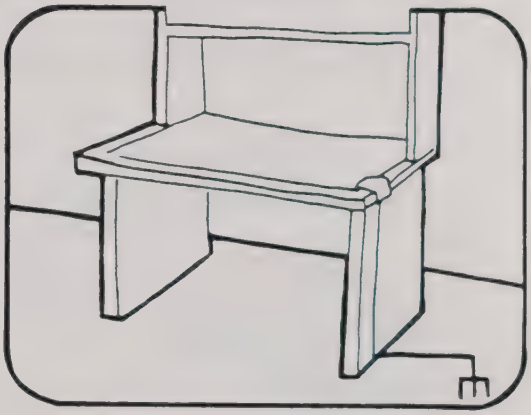
6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE



7. AVOID PLASTIC, VINYL AND STYROFOAM® IN WORK AREA



8. WHEN REMOVING PLUG-IN ASSEMBLIES, HANDLE ONLY BY NON-CONDUCTIVE EDGES AND NEVER TOUCH OPEN EDGE CONNECTOR EXCEPT AT STATIC-FREE WORK STATION. PLACING SHORTING STRIPS ON EDGE CONNECTOR USUALLY PROVIDES COMPLETE PROTECTION TO INSTALLED SS DEVICES.



9. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION
10. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.
11. ONLY GROUNDED TIP SOLDERING IRONS SHOULD BE USED.

Anti-static bags, for storing S.S. devices or pcbs with these devices on them, can be ordered from the John Fluke Mfg. Co., Inc.. See section 5 in any Fluke technical manual for ordering instructions. Use the following part numbers when ordering these special bags.

John Fluke Part No.	Description
453522	6" X 8" Bag
453530	8" X 12" Bag
453548	16" X 24" Bag
454025	12" X 15" Bag
Pink Poly Sheet 30"x60"x60 Mil P/N RC-AS-1200 $20.00	Wrist Strap P/N TL6-60 $7.00

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AND GENERAL DYNAMICS, POMONA DIV.

• Dow Chemical

J00898-07U7810/SE EN Litho in U.S.A.

SECTION 4

MAINTENANCE

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INTRODUCTION

This section of the 2280 Series Service Manual contains internal access procedures for all major assemblies, performance test procedures, and cleaning and lubrication instructions for the Data Logger standard mainframe assemblies. The performance test is recommended as an acceptance test when the instrument is first received, and later as a preventive-maintenance tool to verify proper operation and performance accuracy. A summary of test equipment required for all procedures in this manual is given in Table 2-1 in Section 2. Test equipment unique to each procedure is specified with the procedure in which it is used.

GENERAL MAINTENANCE

Line Voltage Selection

The Data Logger will operate from any of four ac line voltages at either 50 or 60 Hz. Two switches located on the Transformer Assembly must be preset to configure the Data Logger to operate from a specific ac line voltage. Fuse F1 must have the proper rating for the ac input voltage selected.

To gain access to the line voltage switches, follow the steps for Transformer Assembly Access. Figure 4-1 shows the location of the line voltage select switches. Set the switches to the positions given in Table 4-1. Whenever the line voltage switches are checked or set, make sure that the fuse rating is the same as that shown in Table 4-1.

Fuse Replacement

There are two fuses located just above the ac power input connector on the extreme lower left of the Data Logger rear panel. Fuse F1 is the ac input fuse and fuse F2 is the dc input fuse. Refer to the rear panel decal or Table 4-1 for correct fuse ratings for each voltage range.

To check or replace the fuses, unscrew the fuse covers with a slotted screwdriver or adjustment tool. After each fuse has been checked or replaced, reinstall the fuse covers.

Table 4-1. Fuse Ratings and Line Voltage Select Switches

AC INPUT VOLTAGE	F1 VALUE	S1 POSITION (DOT SHOWING)	S2 POSITION (DOT SHOWING)
90-110V ac	1.5A Slow	Red Dot (up)	White Dot (down)
108-132V ac	1.5A Slow	Red Dot (up)	Red Dot (up)
198-242V ac	.75A Slow	White Dot (down)	White Dot (down)
216-250V ac	.75A Slow	White Dot (down)	Red Dot (up)

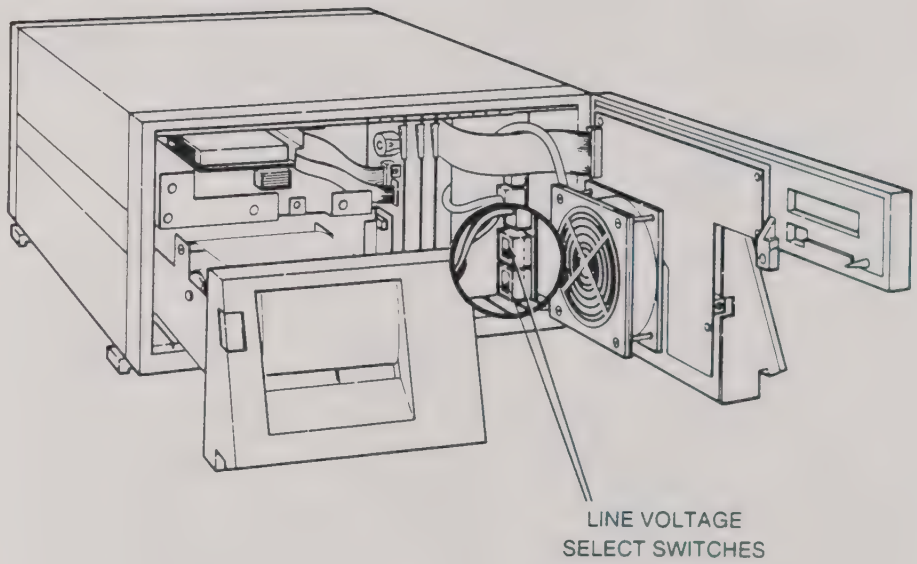

Figure 4-1. Line Voltage Select Switches

General Cleaning

Before cleaning any part of the Data Logger, read the following words of caution:

- Do not use aromatic hydrocarbons or chlorinated solvents for cleaning. They may damage plastic materials used in the instrument.
- Do not handle the PCA's by the connector pins; handle them by the edges. Oil from the skin contaminates the PCA and will degrade measurement accuracy.
- Improper handling may also cause instantaneous or delayed electrostatic discharge damage. The yellow "Static Awareness" sheet inserted near the front of this manual explains some of the hazards associated with static electricity and sensitive components.
- Do not use a static-inducing vacuum brush to clean PCA's. Possible electrostatic discharge can damage sensitive components.

Clean the Data Logger periodically to remove dust, grease, and other contamination. The Data Logger case may be cleaned using a soft cloth dampened with a mild solution of detergent and water. Dry the case after cleaning.

PCA Cleaning

If visual inspection reveals significant contamination on printed circuit board surfaces, dust may be blown off using low pressure (<20psi) air. If air is not available, clean the PCA's with commercial water-based cleaning equipment.

If commercial water-based cleaning equipment is not available, clean the PCA's by holding them under warm, running water. Observe the following precautions when using water-based cleaning equipment:

1. Read all precautions listed above under General Cleaning.
2. If hand washing, gently brush the board surfaces under running water with a very clean bristle paint brush.
3. Remove all PCA shielding covers and relay piggy-back assemblies.
4. In areas with hard water, use either deionized or distilled water for a final wash to remove ions left by the hard water wash.
5. Dry all PCA's thoroughly. Use a low-temperature drying chamber or an infrared drying rack with a temperature range between 38 to and 46 degrees C (100 and 120 degrees F).
6. If a drying chamber or infrared drying rack is not available, air-dry the PCA's at room temperature for a minimum of 48 hours before reassembling.
7. Use a mixture of 70% isopropyl alcohol and 30% water and a

lint-free cloth to clean edge connector contacts. Never use an eraser to clean connector contacts; it will generate static or abrade the gold plating on the contacts.

Fan Filter Cleaning

The fan filter should be cleaned periodically to ensure adequate ventilation and clean air. To gain access to the fan filter, follow the steps under the heading Fan Motor and Display Assembly Access. Then use the following procedure to clean the fan filter:

1. Remove the center grill from the plastic fan-filter holder by snapping it out of the surrounding plastic shell as shown in Figure 4-2.

2. Remove the filter element from the plastic shell, and wash it in a solution of mild detergent and water.

3. Dry the filter element thoroughly.

4. Replace the filter element in the plastic shell, then reinstall the center grill section over the filter element.

5. Close and secure the front panel.

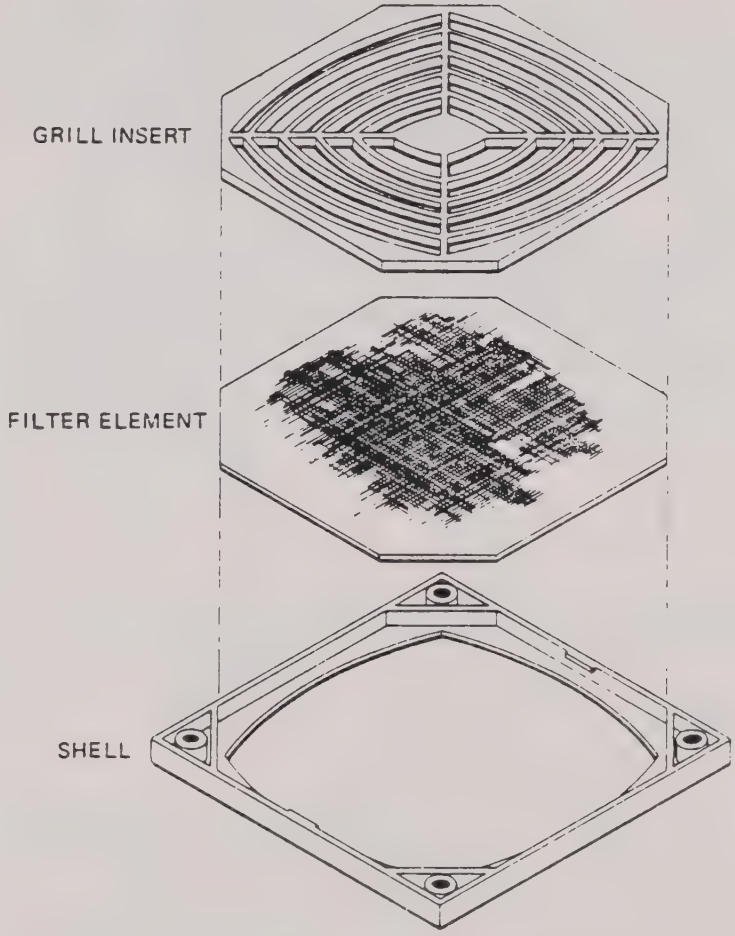

Figure 4-2. Fan Filter Assembly

ACCESS PROCEDURES

The following procedures provide step-by-step instructions for gaining access to all major assemblies and various internal switches in the Data Logger. Refer to Figure 4-3 for the location of the major assemblies on the Data Logger chassis.

WARNING

THE DATA LOGGER CONTAINS HIGH VOLTAGES WHICH CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE EQUIPMENT. TURN OFF THE 2280B AND REMOVE ALL POWER SOURCES BEFORE PERFORMING ANY OF THE FOLLOWING ACCESS PROCEDURES.

Access To Options

Interface, measurement and control, and connector options for the Data Logger are accessible from the rear of the instrument. An option PCA or connector option may be removed by loosening the two retaining screws, one on each side, and pulling the option PCA out of the back of the data logger. Measurement and control options and A/D Converters mount in the horizontal slots in the rear of the data logger. Interface options, such as the RS-232-C and IEEE-488 options, mount in the two vertical option slots just to the left of the horizontal option slots (viewed from the rear).

Top And Bottom Cover Removal

Some of the access procedures require removing the top or bottom covers, or both. Use the following procedure to remove the covers:

1. Locate the single retaining screw in the rear edge of each cover, at the center of the cover.

2. Remove the two retaining screws.

3. Remove the 4 screws at the ends of both side handles, and remove the two handles.

4. Remove the 10 screws from the center of both sides.

5. Slide the cover toward the rear of the case to release the front edge of the cover. (The front edge of the cover is fitted under the bezel at the front of the Data Logger.)

6. Flex the sides slightly outward and lift the cover clear of the chassis, being careful not to scratch the rear bezel.

7. To reinstall the cover, reverse the preceding steps.

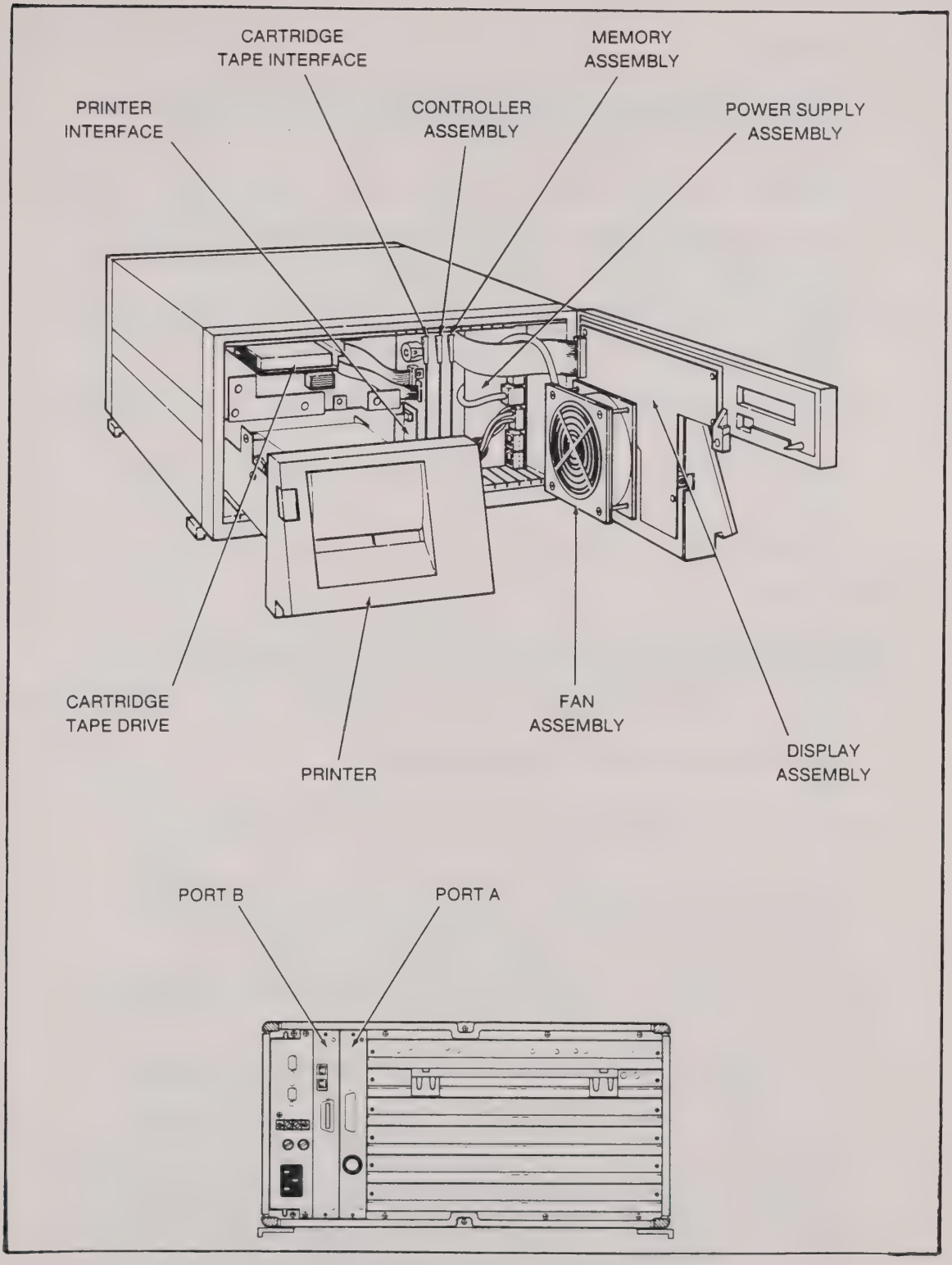

Figure 4-3. Major Assemblies on the 2280B Chassis

Power Supply Access

Power supply circuitry is mounted on a PCA installed behind the left-most rear panel section, as viewed from the rear. To remove the power supply PCA, use the following procedure:

1. Disconnect the line power cord from the rear panel input connector.

2. Remove the single screw located below and to the right of the lower rear panel D-connector (J25), or on newer units, remove the 4 jacksocket screws that fasten the panel to J23 and J25.

3. Remove the two screws (one at the top and one at the bottom) that secure the panel to the Data Logger chassis.

4. Pull the panel out slightly and move it to the left, being careful not to strain the connected wiring.

5. Pull the power supply PCA's out of the chassis, past the rear panel.

6. Reverse the previous steps to reinstall the power supply PCA.

Front Panel Access

To reach the Printer Interface Assembly, Controller Assembly, Memory Assembly, Display Board, or Transformer Assembly, the front panel must be opened. To gain access to any of these assemblies, use the following procedure:

1. Open the door over the tape drive unit.

2. Loosen the captive screw located below the left end of the tape slot.

3. Pull the printer unit out until the slide is fully extended.

4. Loosen the captive screw just below the right edge of the tape drive unit, at the top edge of the printer opening.

5. Loosen the captive screw located just below the programming keys, at the bottom of the front panel.

6. Pull on the tape slot end of the front panel, and swing the front panel open.

7. There may be up to six PCA's mounted in slots behind the front panel. From left to right, viewed from the front, they are: Printer Interface Assembly, Cartridge Interface Assembly, Controller Assembly, Memory Assembly, Advanced Math Assembly, and, mounted on the right side of the chassis, the Transformer Assembly. The Cartridge Interface and the Advanced Math Assemblies are options, and need not be in place for basic instrument operation.

Transformer Assembly Access

WARNING
TO PREVENT ELECTRIC SHOCK, REMOVE ALL LINE POWER AND INPUT SIGNAL LINES BEFORE STARTING THIS PROCEDURE.

To gain access to the Transformer Assembly, perform the following steps:

1. Remove the top and bottom covers using the procedure given previously.
2. The Transformer Assembly is mounted on the right side of the chassis, behind the front panel. Follow the preceding steps to open the instrument front panel.
3. Remove the fan motor mounted on the inside of the front panel by removing the two bottom and the top-right fan mounting screws.
4. Unplug all connectors attached to the front of the Transformer Assembly.
5. Remove both the top and bottom screws that hold the assembly to the chassis.
6. Pull the assembly out the front of the instrument.
7. Reverse the previous steps to reinstall the transformer assembly.

Printer Access

To remove the printer from the Data Logger chassis, use the following procedure:

1. Remove the top and bottom covers as instructed in the cover removal procedure.
2. Press the latch at the left side of the printer to release it, and pull the printer out until the printer slide is fully extended.
3. Open the front access panel (refer to the front panel access procedure), and disconnect the printer cable clamp from the top of the chassis.
4. Remove the PCA retainer from the Printer Interface PCA.
5. Remove the Cartridge Tape Drive PCA if one is installed (refer to the Option 2280A-214 subsection for removal instructions).
6. Slide the Printer Interface PCA out far enough to disconnect the printer cable, then disconnect the printer cable.
7. Remove the Printer Interface PCA.

8. Push the printer cable behind the sheet-metal partition and out through the printer opening.

9. From the bottom of the unit, remove the three screws that secure the printer to the printer slide.

10. To reinstall the printer, reverse the previous steps.

Fan Motor And Display Assembly Access

To remove the Fan Motor and Display Assembly, use the following procedure:

1. Perform the front panel access procedure.

2. Disconnect the gray, flat cable from the Display board.

3. Remove the fan by removing the two bottom and the top right fan mounting screws. (The top left screw holds the filter housing to the fan housing, but does not hold the assembly to the front panel).

4. Remove the three remaining screws that hold the Display Assembly to the front panel.

5. Disconnect the two ribbon cables that connect the Display Assembly to the keyboard.

6. To reinstall the Display Assembly and Fan Motor, reverse the previous steps.

PERFORMANCE TESTING

The following paragraphs describe system diagnostic and performance verification tests. These tests can be used to compare the instrument's performance to specifications located in the appendix. The various diagnostic tests contained in the Data Logger software, which are selected and run through the system test menu, are summarized under the heading System Diagnostics. By selecting the appropriate test from menu prompted choices, a suspected fault can be investigated to isolate a problem quickly.

Under the heading Performance Test Procedures, a series of comprehensive verification tests, divided into specific circuit sections, are given. The performance tests incorporate some of the system diagnostic tests, but also require connecting test equipment and entering menu-driven programming steps. The performance tests can be used as a complete performance verification test for the Data Logger, or as thorough diagnostic tests for specific circuit sections.

System Diagnostics

A system test can be initiated after power-up when the keyswitch is in the PROGRAM position. The user can request system tests for any of seven system elements: the Controller, Advanced Math Processor, Keyboard/Display, Cartridge Tape, Port A, Port B, or Serial Link. The following five steps describe how to enter the System Test Menu, execute a desired test, and leave the System Test Menu. The function of each of the system diagnostic tests and the meaning of the prompts resulting from each test are described in the Summary of System Diagnostics subsection.

ENTERING AND RUNNING SYSTEM TESTS

1. Enter the System Test Menu from the Main Menu by pressing the "S" key. The Data Logger acknowledges with the prompt:

   ```
   <S> SYSTEM DIAGNOSTICS
   ```

2. Press the ENTER key. The prompt becomes:

   ```
   S: DEVICE TO TEST <1-7>? 1
   ```

   Now, the system is ready for you to choose a test from the System Test Menu. The seven system tests as they are shown on the Data Logger display are:

   ```
   S<1> CONTROLLER AND MEMORY
   S<2> KEYBOARD AND DISPLAY
   S<3> PORT A
   S<4> PORT B
   S<5> DC 100 CARTRIDGE TAPE DRIVE
   S<6> ADVANCED MATH PROCESSOR
   S<7> SERIAL LINK
   ```

3. Select the circuit section to be tested by pressing the appropriate

number followed by the ENTER key. Several test functions can be performed on each of the seven circuit sections, with the exception of the Serial Link section. For each device, where n is the number of tests for that device, the prompt becomes:

TEST <1-n>? 1

4. Select, by number, a particular test to be performed. When the selection has been made and ENTER is pressed, the prompt TEST IN PROGRESS is displayed. The test results are then displayed on the front panel, indicating that either the test was successful (TEST PASSED) or that it has failed (TEST FAILED). Some tests also provide other helpful prompts. To step through and acknowledge these results, press EXIT successively to view each test result response until there are no more. Press EXIT twice to return to the system test menu and obtain the following prompt:

S: DEVICE TO TEST <1-7>? _

5. When all desired tests are completed, press the EXIT key. The Data Logger will execute a power-on sequence and return to the Main Menu.

SUMMARY OF SYSTEM DIAGNOSTICS

In the following summary, the function of each test is described, and an explanation of the prompts resulting from each test is given. This summary can be used as a guide through the system diagnostic tests once the steps in the preceding paragraphs have been read and understood. The capitalized headings throughout this summary are identical to the actual Data Logger prompt. Under each heading is a phrase that describes what takes place when that test is invoked.

Caution

The RAM test for the controller, and the full RAM test for the Advanced Math Processor will erase the configuration program. Before starting this test, make sure your program can be conveniently reloaded when the test is complete.

S<1> CONTROLLER AND MEMORY

<1> ROM CHECKSUM TEST

This reads each ROM to see if the information stored in it is still correct. If any information has changed, the following error message is displayed:

XUnn ROM CHECKSUM TEST FAILED

(Where X = C for Controller Assembly or M for Memory assembly, and Unn = Reference designation of the faulty part, indicated by a one or two-digit number.

To acknowledge the error message, press EXIT. If there are errors in multiple ROMs, the additional reference designations can be displayed by sequentially pressing EXIT.

<2> RAM TEST (destroys the configuration program)

The RAM TEST Checks memory for proper read, write, and address decoding by performing a sequential write and read at every RAM location. If any RAM location fails, the following failure message is displayed:

xUnn RAM TEST FAILED

(Where X = C for Controller Assembly or M for Memory assembly, and Unn = Reference designation of the faulty RAM).

S<2> DISPLAY AND KEYBOARD

<1> DEVICE/CONTROLLER INTERFACE TEST

This tests the internal communication between the Display/Keyboard Assembly and the Controller board.

<2> PAINT CHARACTERS TEST

This lights up on all dots on the display.

<3> HORIZONTAL LINES TEST

This prints three horizontal lines across the full length of the display.

<4> VERTICAL LINES TEST

This prints a vertical line pattern across the display.

<5> KEYBOARD LED'S TEST

This sequentially lights all keyboard LEDs in the following order: Scan, Plot, Remote/Local, Alarm Ack. Single Scan, and Monitor.

<6> KEYBOARD TEST

This allows all keyboard buttons to be checked by echoing the depressed key to the display.

S<3> PORT A

<1> DEVICE CONTROLLER INTERFACE

This tests the internal communication between the interface board and the controller board.

If Option 2280A-341 RS-232-C Interface is installed, tests <2> through <4> can be performed:

<2> RAM TEST

This ensures that the RS-232-C board RAM is completely functional by performing a sequential read after write at every RAM location.

<3> UART TEST

This verifies Universal Asynchronous Receiver-Transmitter operation on the interface option PCA.

<4> RS-232 CONTROL LINE TEST

This tests the control lines accessible through J22. The lines are connected as follows:

From		To	
Pin Number	Mnemonic	Pin Number	Mnemonic
5	CTS	4	RTS
6	DSR	20	DTR
8	RLSD	20	NON

If Option 2280A-342 IEEE-488 Interface is installed, the following test can be performed:

<2> INTERNAL BUS TEST

This verifies operation of the IEEE-488 Interface assembly's CPU.

S<4> PORT B

(Same as Port A)

S<5> DC-100 CARTRIDGE TAPE DRIVE

<1> DEVICE/CONTROLLER I/F TEST

This tests the internal communications between the Cartridge Tape Drive board and the Controller board.

<2> ROM CHECKSUM

This checks the ROM to see if the information contained in it is still correct.

<3> RAM TEST

This ensures that the cartridge interface RAM is completely functional by performing a sequential read after write at every RAM location.

<4> ENCODE/DECODE TEST

This verifies the operation of the encoding and decoding circuitry by routing the output of one into the input of the other and checking the result.

<5> TAPE DRIVE READ/WRITE

This writes known blocks of data to the tape, reads the data from the tape, and compares the data read to the original data.

S<6> Advanced Math Processor

<1> ITEMS FAILED AT POWER UP

This displays the errors encountered during the math board power-up self tests. Possible errors are:

MATH BOARD INTERFACE FAILED
INCOMPATIBLE MATH BOARD SOFTWARE
MATH BOARD ROM CHECKSUM TEST FAILED
MATH BOARD RAM TEST FAILED
MATH BOARD APU TEST FAILED
MATH BOARD DOES NOT RESPOND

<2> ROM CHECKSUM TEST

This checks each ROM on the Math Board to see if the information stored in it is still correct. If the information has changed, the following error message is displayed:

Unn ROM CHECKSUM TEST FAILED

(Where Unn is the reference designation of the faulty part).

<3> MATH BOARD RAM TEST

This ensures that the Math Board RAM is completely functional by performing a sequential read after write at every RAM location.

<4> FULL RAM TEST (destroys the configuration programming)

This checks the RAM for proper internal and external read, write, and address decoding by performing sequential write and reads at every RAM location. If any RAM location fails, the following failure message is displayed:

AUnn RAM TEST FAILED

(Where A indicates the Advanced Math Assembly, and Unn indicates the reference designation of the failed RAM).

5> SIMPLE APU (Advanced Math Processor) TEST

This causes the math board CPU to run some simple mathematical tests on the math processor.

<6> COMPLEX APU (Advanced Math Processor) TEST

The Math Board CPU runs a full functional test on the math processor.

S<7> Serial Link

The serial link performance test verifies the ability of the Data Logger to communicate using the serial link. The serial link connects the Data Logger controller to serial link options (that must be installed in the mainframe to perform this test). Serial link options for the Data Logger include:

- Option 2280A-161 High Performance A/D Converter
- Option 2280A-168 Digital I/O Assembly
- Option 2280B-167 Counter/Totalizer
- Option 2280B-170 Analog Output

To run the test, a one-to-four-digit number equal to the first channel number associated with the serial link device must be entered (see Serial Link Performance Test in the Performance Test Procedures section following). The Data Logger then attempts to communicate through the serial link to the option.

Performance Test Procedures

The following five procedures provide a comprehensive test sequence for the Data Logger mainframe. Each procedure tests different features or functions of the Data Logger mainframe. The five test procedures are:

- Display and Keyboard
- Functional Capability
- Serial Link
- Printer
- Interface Communication*

Note that the remote interface capabilities test is followed by an asterisk. An asterisk indicates that the procedure is an optional test which may be required in some cases, but not all, since the Data Logger is often operated without using a remote interface.

The basic performance test procedures require only standard mainframe assemblies; no other equipment is required. However, some of the optional tests do require additional options. Data Logger options necessary to perform all tests are listed in Table 4-2.

Table 4-2. Options Necessary for Full Performance Testing

OPTION NUMBER	OPTION NAME
2280A-214	Advanced Math Processor
2280A-161	High Performance A/D Converter
2280A-162	Thermocouple/DC Volts Scanner
2280A-341	IEEE-488 Interface
2280A-342	RS-232-C Interface

DISPLAY AND KEYBOARD PERFORMANCE TEST

1. Disconnect the ac power line cord and all other high voltage inputs.

WARNING

HIGH VOLTAGE IS PRESENT INSIDE THE FRONT PANEL WHEN AC OR DC POWER IS CONNECTED. USE EXTREME CAUTION WHILE PERFORMING THE FOLLOWING STEPS.

2. Disconnect any external devices connected to the Data Logger mainframe (i.e. IEEE-488 or RS-232-C interfaces).

3. Verify line voltage selection and correct fuse ratings (checking the line voltage selection switches requires opening the front panel. Refer to the front panel access procedure, Figure 4-1 and Table 4-1).

4. Apply either line or battery power to the Data Logger.

5. While holding the ENTER key on the keyboard depressed, turn the keyswitch from the OFF position to the PROGRAM position. Holding the ENTER key for 5-10 seconds, watch for the following results:

   All dots in all display characters should light.

   After 8 seconds:

   The display should change to 3 horizontal lines that are continuous across all 40 display characters. Verify that no other dots are displayed.

   After 8 more seconds:

   The display should appear as follows:

```
 |  |  |    | |    |  |  |    | |    (continuing across the
 |dig 1|  |dig 2|  |dig 3|  |dig 4|  entire display)
```

   After 8 more seconds:

   The 6 LEDs on the keyboard associated with the SCAN, PLOT, REMOTE/LOCAL, ALARM ACK, SINGLE SCAN, and MONITOR keys, and should light, in the order listed, with only one being lit at a time. Verify that all six LEDs light, and then are extinguished.

   After 4 more seconds:

   The Data Logger should display:

   [KEYBOARD TEST: PRESS <EXIT> WHEN DONE]

6. Press the following keys and verify that the correct characters appear on the display in the order entered:

   ABCDEFGHIJKLMNOPQRSTUVWXYZ.0123456789+-*/

7. Press ENTER. The Data Logger should display:

   [KEYBOARD TEST: PRESS <EXIT> WHEN DONE]

8. Press the following keys:

   SCAN, SINGLE SCAN, PLOT, MONITOR, ACK, LOCAL, CLEAR, UP-ARROW, DOWN-ARROW, RIGHT-ARROW, LEFT-ARROW, SPACE, (,), =, DELETE CHAR

   Verify that the Data Logger displays:

   & # ; % @ " \ [ ] > < ( ) = []

9. Press EXIT. The Data Logger should display:

   [MAIN MENU CHOICE <M FOR MENU>? A]

10. Press the <ENTER> key. A tone should issue from the front panel. Ensure tone is of acceptable loudness. If it is not, refer to the calibration procedures in this section.

11. Press <EXIT> repeatedly until the Data Logger displays:

    [MAIN MENU CHOICE <M FOR MENU>? A]

12. The display and keyboard performance test is complete.

FUNCTIONAL CAPABILITY PERFORMANCE TEST

The following test verifies that the data logger mainframe is functional. Interface communication, the printer, the serial link, and the Advanced Math option are not tested here.

1. Turn the Data Logger keyswitch to OFF. Disconnect the ac line power cord and all other high voltage inputs.

   WARNING

   HIGH VOLTAGE IS PRESENT INSIDE THE DATA LOGGER WHEN AC OR DC POWER IS CONNECTED. DISCONNECT POWER FROM THE DATA LOGGER BEFORE PERFORMING THE FOLLOWING STEPS.

2. Pull out the Printer assembly and verify that the PRINTER switch is in the ON position (refer to Figure 4-4).

3. Push the printer back into the case, and reconnect the power input (ac line cord or battery).

4. Turn the keyswitch to PROGRAM. After a few seconds, the data logger should display:

   [MAIN MENU CHOICE <M FOR MENU>? A]

5. Repeatedly press the down-arrow key. The Data Logger should display in sequence:

   A PROGRAM A CHANNEL OR BLOCK
   F PROGRAM AN ALARM LIST
   K PROGRAM A SCAN GROUP

```
<P>  PROGRAM PLOT PARAMETERS
<U>  PROGRAM OUTPUT DEVICE PARAMETERS
<Z>  PROGRAM SYSTEM PARAMETERS
<D>  TRANSFER DATA
<T>  PERFORM A TAPE FUNCTION
<L>  LIST PROGRAM AND CONFIGURATION
<E>  ERASE ALL OF PROGRAM MEMORY
<S>  SYSTEM DIAGNOSTICS
<M>  PRINT THE MENU
```

6. Press EXIT. The Data Logger should display:

```
MAIN MENU CHOICE <M FOR MENU>? A
```

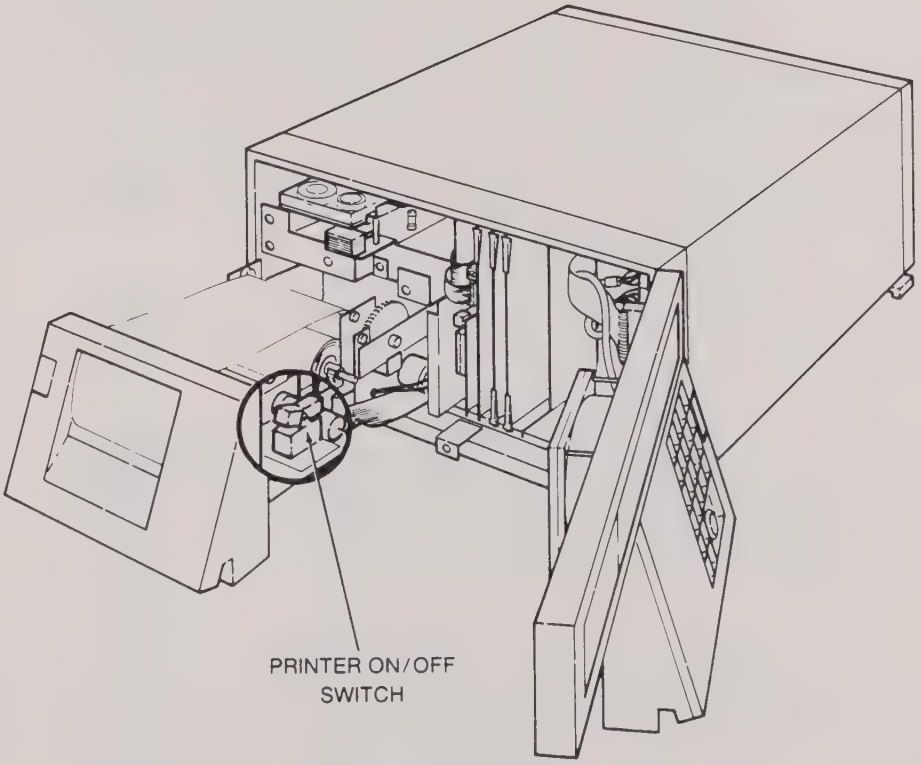

Figure 4-4. Printer On/Off Switch Location

7. Execute the Controller ROM self-test by performing the steps listed in Table 4-3.

Table 4-3. ROM Self-Test Programming Steps

STEP	KEYSTROKE	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>?
2	S	<S> SYSTEM DIAGNOSTICS
3	ENTER	S: DEVICE TO TEST <1-7>? 1
4	ENTER	S1: TEST <1,2>? 1
5	1	S1 <1> ROM CHECKSUM TEST
6	ENTER	

8. After a short delay, verify that the Data Logger displays:

   [TEST PASSED]

9. If the unit fails the test, the following error message is displayed:

   XUnn ROM CHECKSUM TEST FAILED

   (Where X = C for Controller Assembly or M for Memory Assembly, and Unn = the reference designation of the faulty part, indicated by a one-or-two-digit number).

10. Execute the RAM self-test by performing the steps in Table 4-4.

Table 4-4. RAM Self-Test Programming Steps

STEP	KEYSTROKE(S)	DATA LOGGER PROMPT
1	EXIT	S1: TEST <1,2>? 2
2	ENTER	REALLY (DESTROYS USER PROGRAM) <Y,N>? N
3	Y	REALLY (DESTROYS USER PROGRAM) <Y,N>? Y
4	ENTER	

11. After a maximum of 30 seconds, verify that the Data Logger displays:

    [TEST PASSED]

12. If the unit fails the test, the following error message is displayed:

    xUnn RAM TEST FAILED

    (Where X = C for Controller Assembly or M for Memory Assembly, and Unn = Reference designation symbol for the faulty RAM).

13. Depress the EXIT key three times to return to the main menu prompt.

14. Program a scan group and time interval using the steps given in Table 4-5.

Table 4-5. Scan Group and Time Interval Programming Steps

STEP	KEYSTROKE	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	K	<K> PROGRAM A SCAN GROUP
7	ENTER	SCAN GROUP NUMBER = 0
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	K: SCAN GROUP MENU CHOICE <1-5>? 1
10	ENTER	SCAN GROUP LABEL <40 CHRS MAX>=
11	SGL	SCAN GROUP LABEL <40 CHRS MAX>= SGL
12	ENTER	K: SCAN GROUP MENU CHOICE <1-5>? 2
13	ENTER	CL:
14	C0..9	CL: C0..0
15	ENTER	CL:
16	ENTER	K: SCAN GROUP MENU CHOICE <1-5>? 3
17	ENTER	K3: TRIGGER MODE <1-5>? 1
18	2	K3<2> TIME INTERVAL SCAN
19	ENTER	TIME INTERVAL =
20	00.00.15	TIME INTERVAL = 00:00:15
21	ENTER	K: SCAN GROUP MENU CHOICE <1-5>? 4
22	ENTER	K4: DEVICE <1-5>? 1
23	2	K4<2> PRINTER
24	ENTER	K42: TYPE OF DATA <1-4>? 1
25	2	K42<2> ALL DATA
26	ENTER	K4: DEVICE <1-5>? 3
27	EXIT	K: SCAN GROUP MENU CHOICE <1-5>? 5
28	EXIT	SCAN GROUP NUMBER = 0
29	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

15. Press the SCAN key. The SCAN indicator should light, and the Data Logger should print the following:

```
BEGIN SCAN GROUP 0        DD MMM YY  AA:AA:AA
SGL
C          0          .00000
C          1          .00000
C          2          .00000
C          3          .00000
C          4          .00000
C          5          .00000
C          6          .00000
C          7          .00000
C          8          .00000
C          9          .00000

END SCAN GROUP 0          DD MMM YY  BB:BB:BB

BEGIN SCAN GROUP 0        DD MMM YY  CC:CC:CC
SGL
C          0          .00000
C          1          .00000
C          2          .00000
C          3          .00000
C          4          .00000
C          5          .00000
C          6          .00000
C          7          .00000
C          8          .00000
C          9          .00000

END SCAN GROUP 0          DD MMM YY  BB:BB:BB
```

DD MM YY is the current date (day: month: year).
AA:AA:AA is the current time (hours : minutes : seconds). (Date and time will be correct only if they have been loaded.)
BB:BB:BB is between 2 and 4 seconds after time AA:AA:AA.
CC:CC:CC is exactly 15 seconds after time AA:AA:AA.

16. Press SCAN again. The Data Logger should stop printing and the SCAN indicator should extinguish.

17. Enter the steps in Table 4-6 to test the system clock:

Table 4-6. System Clock Self-Test Programming Steps

STEP	KEYSTROKE	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	Z	<Z> PROGRAM SYSTEM PARAMETERS
3	ENTER	Z:SYSTEM MENU CHOICE <1-7>? 1
4	2	Z<2> CALANDAR DATE AND TIME
5	ENTER	TIME =
6	23.59.45	TIME = 23:59:45
7	ENTER	DATE =
8	31 DEC 85	DATE = 31 DEC 85
9	ENTER	Z:SYSTEM MENU CHOICE <1-7>? 3
10	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

18. Press SCAN. The Data Logger should print:

```
BEGIN SCAN GROUP 0        1 JAN 86  AA:AA:AA
SGL
C          0          .00000
C          1          .00000
C          2          .00000
C          3          .00000
C          4          .00000
C          5          .00000
C          6          .00000
C          7          .00000
C          8          .00000
C          9          .00000
```

Where AA:AA:AA is 23:59:45 plus the time lapse between performing steps 14 and 15.

18. The functional capabilities performance test is complete.

SERIAL LINK PERFORMANCE TEST

The serial link performance test verifies the ability of the Data Logger to communicate using the serial link. The serial link connects the controller to serial link options. One option must be installed in the mainframe to perform this test. Serial link options for the Data Logger include:

- Option 2280A-161 High Performance A/D Converter
- Option 2280A-168 Digital I/O Assembly
- Option 2280B-167 Counter/Totalizer
- Option 2280B-170 Analog Output

To run the Serial Link Performance Test, perform the following steps:

1. Disconnect the Data Logger line power cord, the dc input, and all high-voltage inputs from the data logger.

WARNING

HIGH VOLTAGE IS PRESENT INSIDE THE DATA LOGGER WHEN AC OR DC POWER IS CONNECTED. DISCONNECT POWER FROM THE DATA LOGGER BEFORE PERFORMING THE FOLLOWING STEPS.

2. Remove all serial link options (listed above) from the mainframe.

3. Select one serial link option and set the address on that option to 0 (see Figure 4-5), then reinstall that option.

4. Apply input power to the Data Logger (ac line or battery).

5. Turn the keyswitch to PROGRAM. The Data Logger should display:

[MAIN MENU CHOICE <M FOR MENU>? A]

6. Execute the serial link self-test by entering the steps given in Table 4-7.

Table 4-7. Serial Link Self Test Programming Steps

STEP	KEYSTROKE	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	S	<S> SYSTEM DIAGNOSTICS
3	ENTER	S: DEVICE TO TEST <1-7>? 1
4	7	S<7> SERIAL LINK
5	ENTER	CHANNEL NUMBER = CO
6	0	CHANNEL NUMBER = 0
7	ENTER	

7. After a short delay, verify that the Data Logger displays:

[TEST PASSED]

8. The serial link performance test is complete.

The serial link self-test also provides a superficial operating test for any serial link options in the system. To test an individual suspected serial link option, run its performance test (located in that option's subsection in this manual.

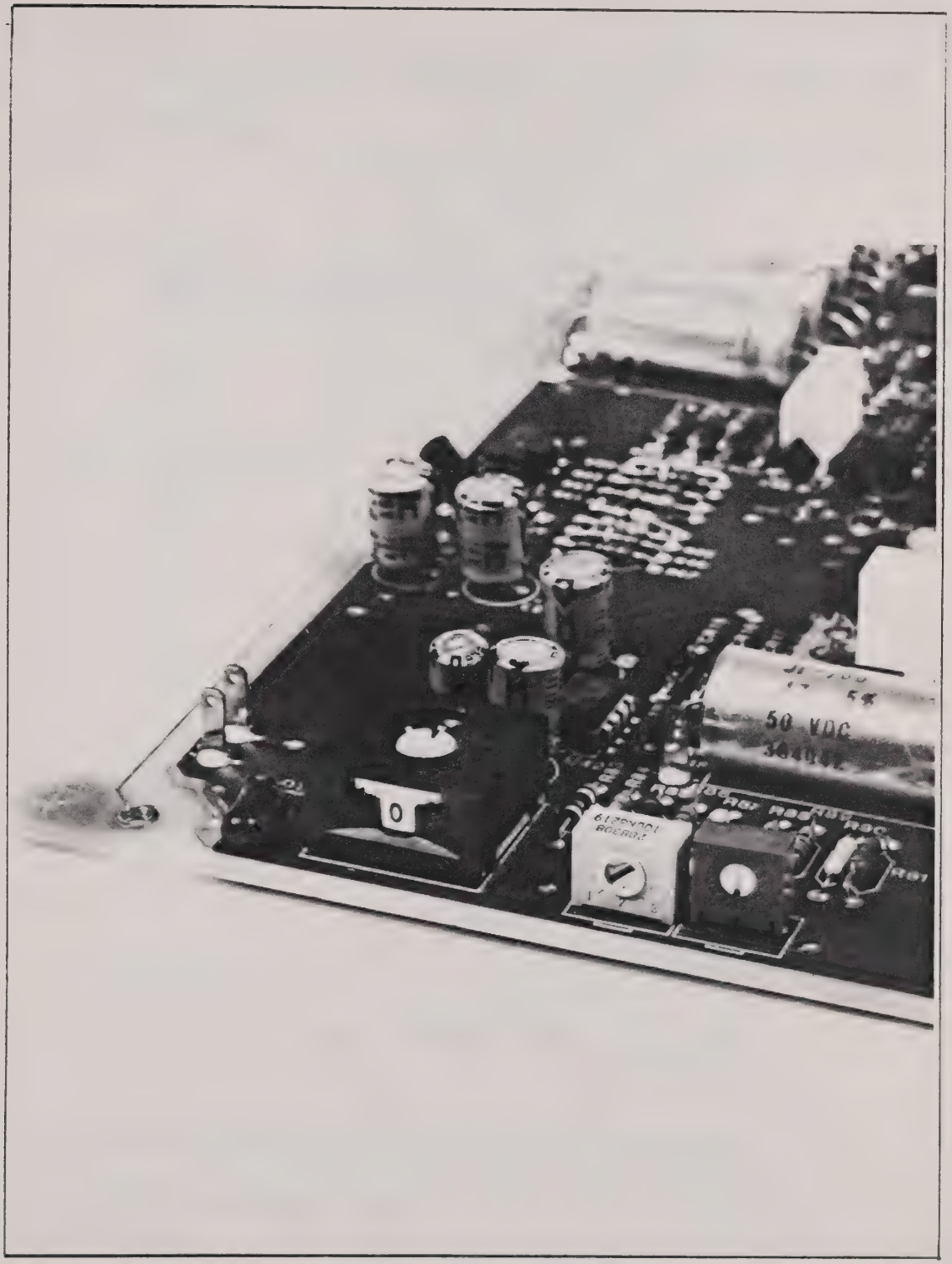

Figure 4-5. Serial Link Option Address Switch

PRINTER PERFORMANCE TEST

The printer performance test verifies that the printer is fully operational. Use the following procedure to test the printer.

1. Turn the keyswitch to OFF. Disconnect the Data Logger line power input and any other high-voltage inputs.

WARNING

HIGH VOLTAGE IS PRESENT INSIDE THE DATA LOGGER WHEN AC OR DC POWER IS CONNECTED. DISCONNECT POWER FROM THE DATA LOGGER BEFORE PERFORMING THE FOLLOWING STEPS.

2. Disconnect any external devices from the Data Logger mainframe (i.e. IEEE-488 or RS-232-C).

3. Verify correct line voltage settings and fuse ratings (refer to front panel access procedure and Figure 4-1 and Table 4-1 in this section), and verify that the printer on/off switch is in the ON position.

4. Reconnect the Data Logger power input.

5. Turn the front panel keyswitch to PROGRAM.

6. The Data Logger will display the following prompt:

```
[MAIN MENU CHOICE <M FOR MENU>? A       ]
```

7. Press M and observe the printer. The Data Logger should print the following information:

```
<A> PROGRAM A CHANNEL OR BLOCK
<F> PROGRAM AN ALARM LIST
<K> PROGRAM A SCAN GROUP
<P> PROGRAM PLOT PARAMETERS
<U> PROGRAM OUTPUT DEVICE PARAMETERS
<Z> PROGRAM SYSTEM PARAMETERS
<D> TRANSFER DATA
<T> PERFORM A TAPE FUNCTION
<L> LIST PROGRAM AND CONFIGURATION
<E> ERASE ALL OF PROGRAM MEMORY
<S> SYSTEM TEST
<M> PRINT THE MENU
```

9. If print alignment or intensity is not satisfactory, proceed to the printer calibration procedures in this section.

10. Turn the Data Logger keyswitch to PROGRAM and enter the steps given in Table 4-8.

Table 4-8. Programming Steps for Sample Plot Printout

STEP	KEYSTROKE	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) =
7	1	CHANNEL NUMBER (OR BLOCK) = 1
8	ENTER	PROGRAM COPY DELETE OR LIST? <P,C,D, OR L> P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
10	ENTER	AP: CHANNEL MENU CHOICE <1-5>? 1
11	3	AP<3> CHANNEL PROCEDURE
12	ENTER	CP:
13	C1=C1+1	CP: C1=C1+1
14	ENTER	CP:
15	ENTER	AP: CHANNEL MENU CHOICE <1-5>? 4
16	EXIT	A: CHANNEL FUNCTION <A-Z>? P
17	EXIT	CHANNEL NUMBER (OR BLOCK) = C1
18	EXIT	MAIN MENU CHOICE <M FOR MENU>? A
19	P	<P> PROGRAM PLOT PARAMETERS
20	ENTER	P: PLOT MENU CHOICE <1,2>? 1
21	ENTER	PLOT NUMBER <1-4>? 1
22	ENTER	CHANNEL TO PLOT =
23	1	CHANNEL TO PLOT = 1
24	ENTER	LEFT MOST VALUE = 0.0
25	ENTER	RIGHT MOST VALUE = 1.0
26	40	RIGHT MOST VALUE = 40
27	ENTER	PLOT NUMBER <1-4>? 2
28	EXIT	P: PLOT MENU CHOICE <1,2>? 2
29	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

11. Press the PLOT key. Verify that a printout similar to the one in Figure 4-6 is obtained.

12. Press PLOT again. Verify that the printer stops.

13. Verify that the PLOT key LED indicator extinguishes.

14. Cut the paper at the paper feed roll (not the take-up roll).

15. Press PLOT. Verify that the ALM ACK indicator lights before 40 values are plotted.

16. Press PLOT and verify that the plot mode LED goes off.

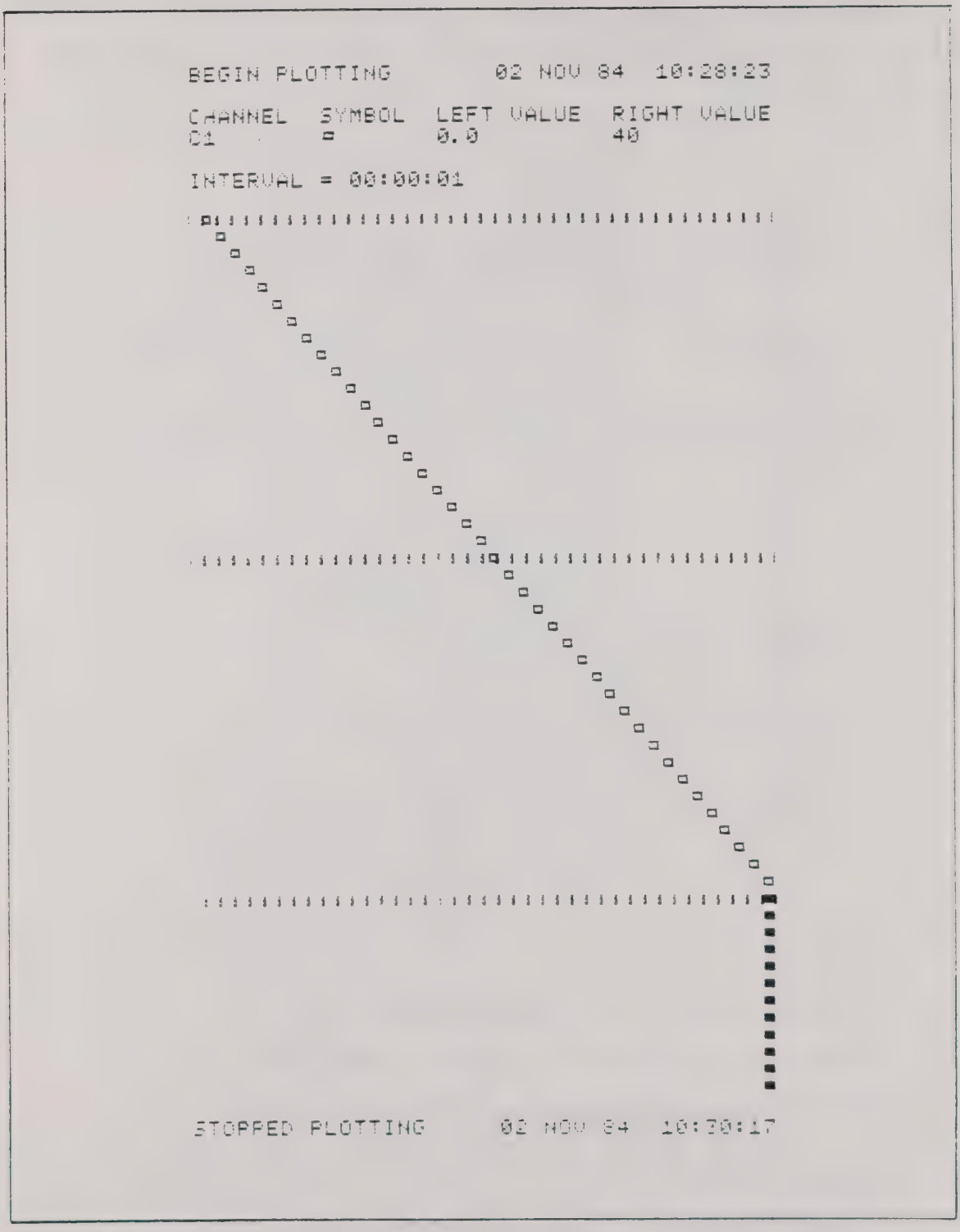
BEGIN PLOTTING 02 NOV 84 10:28:23
CHANNEL SYMBOL LEFT VALUE RIGHT VALUE
C1 = 0.0 40
INTERVAL = 00:00:01
STOPPED PLOTTING 02 NOV 84 10:30:17

Figure 4-6. Sample Plot Printout

17. Refeed the paper into the printer using the PAPER ADVANCE button on the front panel tape the ends of the paper together or attach the end to the take-up reel. (Figure 2-1 in Section 2 shows the location of the PAPER ADVANCE Button).

18. Press the ALM ACK key. Verify that the Data Logger displays:

    [PRINTER OUT OF PAPER]

19. Verify that the ALM ACK indicator turns off.

    NOTE
    It may be necessary to press ALM ACK key more than once to extinguish indicator.

20. The printer performance test is complete.

INTERFACE COMMUNICATION TEST

The following test procedure checks the ability of the Data Logger to communicate through the interface options (Option 2280A-341 RS-232-C Interface or Option 2280A-342 IEEE-488 Interface). Although one interface option or the other must be installed for this test, this procedure is not a comprehensive test of the interface; it tests the mainframe. Since many applications do not require an interface, and the Data Logger mainframe can operate without one, this procedure is optional.

1. Turn the keyswitch to OFF, then disconnect the Data Logger power input.

2. Install either interface option in Port A (refer to Figure 4-3).

3. Verify that the option test switch is in the OFF position.

4. Remove any interface option that may be present Port B.

5. Reconnect the Data Logger power input.

6. Turn the keyswitch to PROGRAM.

7. Initiate the Port A bus test by performing the steps in Table 4-9.

Table 4-9. Port A Bus Test Programming Steps

STEP	KEYSTROKE	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	S	<S> SYSTEM DIAGNOSTICS
3	ENTER	S: DEVICE TO TEST <1-7>? 1
4	3	S<3> PORT A
*5	ENTER	S3: TEST <1-n>? 1
6	1	S3<1> DEVICE/CONTROLLER INTERFACE TEST
7	ENTER	

* (n = the number of the last test for the device installed at Port A)

8. Verify that after a short delay the Data Logger displays:

   [TEST PASSED]

9. Turn the keyswitch to OFF.

10. Move the interface option from Port A to Port B.

11. Turn the keyswitch to the PROGRAM position.

12. Initiate the Port B bus test by performing the steps given in Table 4-10.

Table 4-10. Port B Bus Test Programming Steps

STEP	KEYSTROKE	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	S	<S> SYSTEM DIAGNOSTICS
3	ENTER	S: DEVICE TO TEST <1-7>? 1
4	4	S<4> PORT B
*5	ENTER	S4: TEST <1-n>? 1
6	1	S4<1> DEVICE/CONTROLLER INTERFACE TEST
7	ENTER	

* (n = the number of the last test for the device installed in Port B)

13. Verify that after a short delay the Data Logger displays:

    [TEST PASSED]

14. Turn the keyswitch to OFF.

15. Disconnect the data logger power input.

16. Return the data logger to its original configuration.

17. The remote interface communication performance test is complete.

SECTION 5

TROUBLESHOOTING

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INTRODUCTION

Troubleshooting information presented in this Section is intended to assist in isolating a malfunction to the printed circuit assembly level. Circuit board level troubleshooting can be easily accomplished using the system diagnostics contained in 2280 Series software.

Once the defective circuit board assembly is identified, we recommend that that repair be accomplished using the Fluke Module Exchange Program. Please refer to the Introduction in Section 1. However, a qualified user can troubleshoot 2280 Series circuit boards to the component level using the Theory of Operation section and schematics for required data. Before troubleshooting, however, contact a Fluke Service Representative.

PERFORMANCE TESTING

The following paragraphs describe system diagnostic and performance verification tests. These tests can be used to compare the instrument's performance to specifications located in the appendix. The various diagnostic tests contained in the Data Logger software, which are selected and run through the system test menu, are summarized under the heading System Diagnostics. By selecting the appropriate test from menu prompted choices, a suspected fault can be investigated to isolate a problem quickly.

Under the heading Performance Test Procedures, a series of comprehensive verification tests, divided into specific circuit sections, are given. The performance tests incorporate some of the system diagnostic tests, but also require connecting test equipment and entering menu-driven programming steps. The performance tests can be used as a complete performance verification test for the Data Logger, or as thorough diagnostic tests for specific circuit sections.

System Diagnostics

A system test can be initiated after power-up when the keyswitch is in the PROGRAM position. The user can request system tests for any of seven system elements: the Controller, Advanced Math Processor, Keyboard/Display, Cartridge Tape, Port A, Port B, or Serial Link. The following five steps describe how to enter the System Test Menu, execute a desired test, and leave the System Test Menu. The function of each of the system diagnostic tests and the meaning of the prompts resulting from each test are described in the Summary of System Diagnostics subsection.

Entering And Running System Tests

1. Enter the System Test Menu from the Main Menu by pressing the "S" key. The Data Logger acknowledges with the prompt:

   ```
   <S> SYSTEM DIAGNOSTICS
   ```

2. Press the ENTER key. The prompt becomes:

   ```
   S: DEVICE TO TEST <1-7>? 1
   ```

   Now, the system is ready for you to choose a test from the System Test Menu. The seven system tests as they are shown on the Data Logger display are:

   ```
   S<1> CONTROLLER AND MEMORY
   S<2> KEYBOARD AND DISPLAY
   S<3> PORT A
   S<4> PORT B
   S<5> DC 100 CARTRIDGE TAPE DRIVE
   S<6> ADVANCED MATH PROCESSOR
   S<7> SERIAL LINK
   ```

3. Select the circuit section to be tested by pressing the appropriate

number followed by the ENTER key. Several test functions can be performed on each of the seven circuit sections, with the exception of the Serial Link section. For each device, where n is the number of tests for that device, the prompt becomes:

TEST <1-n>? 1

4. Select, by number, a particular test to be performed. When the selection has been made and ENTER is pressed, the prompt TEST IN PROGRESS is displayed. The test results are then displayed on the front panel, indicating that either the test was successful (TEST PASSED) or that it has failed (TEST FAILED). Some tests also provide other helpful prompts. To step through and acknowledge these results, press EXIT successively to view each test result response until there are no more. Press EXIT twice to return to the system test menu and obtain the following prompt:

S: DEVICE TO TEST <1-7>? _

5. When all desired tests are completed, press the EXIT key. The Data Logger will execute a power-on sequence and return to the Main Menu.

Summary of System Diagnostics

In the following summary, the function of each test is described, and an explanation of the prompts resulting from each test is given. This summary can be used as a guide through the system diagnostic tests once the steps in the preceding paragraphs have been read and understood. The capitalized headings throughout this summary are identical to the actual Data Logger prompt. Under each heading is a phrase that describes what takes place when that test is invoked.

Caution

The RAM test for the controller, and the full RAM test for the Advanced Math Processor will erase the configuration program. Before starting this test, make sure your program can be conveniently reloaded when the test is complete.

S<1> CONTROLLER AND MEMORY

<1> ROM CHECKSUM TEST

This reads each ROM to see if the information stored in it is still correct. If any information has changed, the following error message is displayed:

XUnn ROM CHECKSUM TEST FAILED

(Where X = C for Controller Assembly or M for Memory assembly, and Unn = Reference designation of the faulty part, indicated by a one or two-digit number).

To acknowledge the error message, press EXIT. If there are errors in multiple ROMs, the additional reference designations can be displayed by sequentially pressing EXIT.

<2> RAM TEST (destroys the configuration program)

The RAM TEST Checks memory for proper read, write, and address decoding by performing a sequential write and read at every RAM location. If any RAM location fails, the following failure message is displayed:

xUnn RAM TEST FAILED

(Where X = C for Controller Assembly or M for Memory assembly, and Unn = Reference designation of the faulty RAM).

S<2> DISPLAY AND KEYBOARD

<1> DEVICE/CONTROLLER INTERFACE TEST

This tests the internal communication between the Display/Keyboard Assembly and the Controller board.

<2> PAINT CHARACTERS TEST

This lights up on all dots on the display.

<3> HORIZONTAL LINES TEST

This prints three horizontal lines across the full length of the display.

<4> VERTICAL LINES TEST

This prints a vertical line pattern across the display.

<5> KEYBOARD LED'S TEST

This sequentially lights all keyboard LEDs in the following order: Scan, Plot, Remote/Local, Alarm Ack, Single Scan, and Monitor.

<6> KEYBOARD TEST

This allows all keyboard buttons to be checked by echoing the depressed key to the display.

S<3> PORT A

<1> DEVICE CONTROLLER INTERFACE

This tests the internal communication between the interface board and the controller board.

If Option 2280A-341 RS-232-C Interface is installed, tests <2> through <4> can be performed:

<2> RAM TEST

This ensures that the RS-232-C board RAM is completely functional by performing a sequential read after write at every RAM location.

<3> UART TEST

This verifies Universal Asynchronous Receiver-Transmitter operation on the interface option PCA.

<4> RS-232 CONTROL LINE TEST

This tests the control lines accessible through J22. The lines are connected as follows:

From		To	
Pin Number	Mnemonic	Pin Number	Mnemonic
5	CTS	4	RTS
6	DSR	20	DTR
8	RLSD	20	DTR

If Option 2280A-342 IEEE-488 Interface is installed, the following test can be performed:

<2> INTERNAL BUS TEST

This verifies operation of the IEEE-488 Interface assembly's CPU.

S<4> PORT B

(Same as Port A)

S<5> DC-100 CARTRIDGE TAPE DRIVE

<1> DEVICE/CONTROLLER I/F TEST

This tests the internal communications between the Cartridge Tape Drive board and the Controller board.

<2> ROM CHECKSUM

This checks the ROM to see if the information contained in it is still correct.

<3> RAM TEST

This ensures that the cartridge interface RAM is completely functional by performing a sequential read after write at every RAM location.

<4> ENCODE/DECODE TEST

This verifies the operation of the encoding and decoding circuitry by routing the output of one into the input of the other and checking the result.

<5> TAPE DRIVE READ/WRITE

This writes known blocks of data to the tape, reads the data from the tape, and compares the data read to the original data.

S<6> Advanced Math Processor

<1> ITEMS FAILED AT POWER UP

This displays the errors encountered during the math board power-up self tests. Possible errors are:

MATH BOARD INTERFACE FAILED
INCOMPATIBLE MATH BOARD SOFTWARE
MATH BOARD ROM CHECKSUM TEST FAILED
MATH BOARD RAM TEST FAILED
MATH BOARD APU TEST FAILED
MATH BOARD DOES NOT RESPOND

<2> ROM CHECKSUM TEST

This checks each ROM on the Math Board to see if the information stored in it is still correct. If the information has changed, the following error message is displayed:

Unn ROM CHECKSUM TEST FAILED

(Where Unn is the reference designation of the faulty part).

<3> MATH BOARD RAM TEST

This ensures that the Math Board RAM is completely functional by performing a sequential read after write at every RAM location.

<4> FULL RAM TEST (destroys the configuration programming)

This checks the RAM for proper internal and external read, write, and address decoding by performing sequential write and reads at every RAM location. If any RAM location fails, the following failure message is displayed:

AUnn RAM TEST FAILED

(Where A indicates the Advanced Math Assembly, and Unn indicates the reference designation of the failed RAM).

5> SIMPLE APU (Advanced Math Processor) TEST

This causes the math board CPU to run some simple mathematical tests on the math processor.

<6> COMPLEX APU (Advanced Math Processor) TEST

The Math Board CPU runs a full functional test on the math processor.

S<7> Serial Link

The serial link performance test verifies the ability of the Data Logger to communicate using the serial link. The serial link connects the Data Logger controller to serial link options (that must be installed in the mainframe to perform this test). Serial link options for the Data Logger include:

- Option 2280A-161 High Performance A/D Converter
- Option 2280A-168 Digital I/O Assembly
- Option 2280B-167 Counter/Totalizer
- Option 2280B-170 Analog Output

To run the test, a one-to-four-digit number equal to the first channel number associated with the serial link device must be entered (see Serial Link Performance Test in the Performance Test Procedures section following). The Data Logger then attempts to communicate through the serial link to the option.

PERFORMANCE TEST PROCEDURES

The following five procedures provide a comprehensive test sequence for the Data Logger mainframe. Each procedure tests different features or functions of the Data Logger mainframe. The five test procedures are:

- o Display and Keyboard
- o Functional Capability
- o Serial Link
- o Printer
- o Interface Communication*

Note that the remote interface capabilities test is followed by an asterisk. An asterisk indicates that the procedure is an optional test which may be required in some cases, but not all, since the Data Logger is often operated without using a remote interface.

The basic performance test procedures require only standard mainframe assemblies; no other equipment is required. However, some of the optional tests do require additional options. Data Logger options necessary to perform all tests are listed in Table 5-2.

Table 5-2. Options Necessary for Full Performance Testing

OPTION NUMBER	OPTION NAME
2280A-214	Advanced Math Processor
2280A-161	High Performance A/D Converter
2280A-162	Thermocouple/DC Volts Scanner
2280A-341	IEEE-488 Interface
2280A-342	RS-232-C Interface

Display And Keyboard Performance Test

1. Disconnect the ac power line cord and all other high voltage inputs.

WARNING

HIGH VOLTAGE IS PRESENT INSIDE THE FRONT PANEL WHEN AC OR DC POWER IS CONNECTED. USE EXTREME CAUTION WHILE PERFORMING THE FOLLOWING STEPS.

2. Disconnect any external devices connected to the Data Logger mainframe (i.e. IEEE-488 or RS-232-C interfaces).

3. Verify line voltage selection and correct fuse ratings (checking the line voltage selection switches requires opening the front panel. Refer to the front panel access procedure, Figure 4-1 and Table 4-1).

4. Apply either line or battery power to the Data Logger.

5. While holding the ENTER key on the keyboard depressed, turn the keyswitch from the OFF position to the PROGRAM position. Holding the ENTER key for 5-10 seconds, watch for the following results:

   All dots in all display characters should light.

   After 8 seconds:

   The display should change to 3 horizontal lines that are continuous across all 40 display characters. Verify that no other dots are displayed.

   After 8 more seconds:

   The display should appear as follows:

```
 |  |  |    | |    |  |  |    | |    (continuing across the
 |dig 1|  |dig 2|  |dig 3|  |dig 4|  entire display)
```

   After 8 more seconds:

   The 6 LEDs on the keyboard associated with the SCAN, PLOT, REMOTE/LOCAL, ALARM ACK, SINGLE SCAN, and MONITOR keys, and should light, in the order listed, with only one being lit at a time. Verify that all six LEDs light, and then are extinguished.

   After 4 more seconds:

   The Data Logger should display:

   [KEYBOARD TEST: PRESS <EXIT> WHEN DONE]

6. Press the following keys and verify that the correct characters appear on the display in the order entered:

   ABCDEFGHIJKLMNOPQRSTUVWXYZ.0123456789+-*

7. Press ENTER. The Data Logger should display:

   [KEYBOARD TEST: PRESS <EXIT> WHEN DONE]

8. Press the following keys:

   SCAN, SINGLE SCAN, PLOT, MONITOR, ACK, LOCAL, CLEAR, UP-ARROW, DOWN-ARROW, RIGHT-ARROW, LEFT-ARROW, SPACE, (,), =, DELETE CHAR

   Verify that the Data Logger displays:

   & # ; % @ " \ [ ] > < ( ) = []

9. Press EXIT. The Data Logger should display:

   [MAIN MENU CHOICE <M FOR MENU>? A]

10. Press the <ENTER> key. A tone should issue from the front panel. Ensure tone is of acceptable loudness. If it is not, refer to the calibration procedures in this section.

11. Press <EXIT> repeatedly until the Data Logger displays:

    [MAIN MENU CHOICE <M FOR MENU>? A]

12. The display and keyboard performance test is complete.

Functional Capability Performance Test

The following test verifies that the data logger mainframe is functional. Interface communication, the serial link, the Cartridge Tape option, and the Advanced Math option are not tested here.

1. Turn the Data Logger keyswitch to OFF. Disconnect the ac line power cord and all other high voltage inputs.

   WARNING

   HIGH VOLTAGE IS PRESENT INSIDE THE DATA LOGGER WHEN AC OR DC POWER IS CONNECTED. DISCONNECT POWER FROM THE DATA LOGGER BEFORE PERFORMING THE FOLLOWING STEPS.

2. Pull out the Printer assembly and verify that the PRINTER switch is in the ON position (refer to Figure 5-1).

3. Push the printer back into the case, and reconnect the power input (ac line cord or battery).

4. Turn the keyswitch to PROGRAM. After a few seconds, the data logger should display:

   [MAIN MENU CHOICE <M FOR MENU>? A]

5. Repeatedly press the down-arrow key. The Data Logger should display in sequence:

   A> PROGRAM A CHANNEL OR BLOCK
   F> PROGRAM AN ALARM LIST
   K> PROGRAM A SCAN GROUP

```
<P>  PROGRAM PLOT PARAMETERS
<U>  PROGRAM OUTPUT DEVICE PARAMETERS
 Z>  PROGRAM SYSTEM PARAMETERS
<D>  TRANSFER DATA
<T>  PERFORM A TAPE FUNCTION
.L>  LIST PROGRAM AND CONFIGURATION
<E>  ERASE ALL OF PROGRAM MEMORY
<S>  SYSTEM DIAGNOSTICS
<M>  PRINT THE MENU
```

6. Press EXIT. The Data Logger should display:

```
MAIN MENU CHOICE <M FOR MENU>? A
```

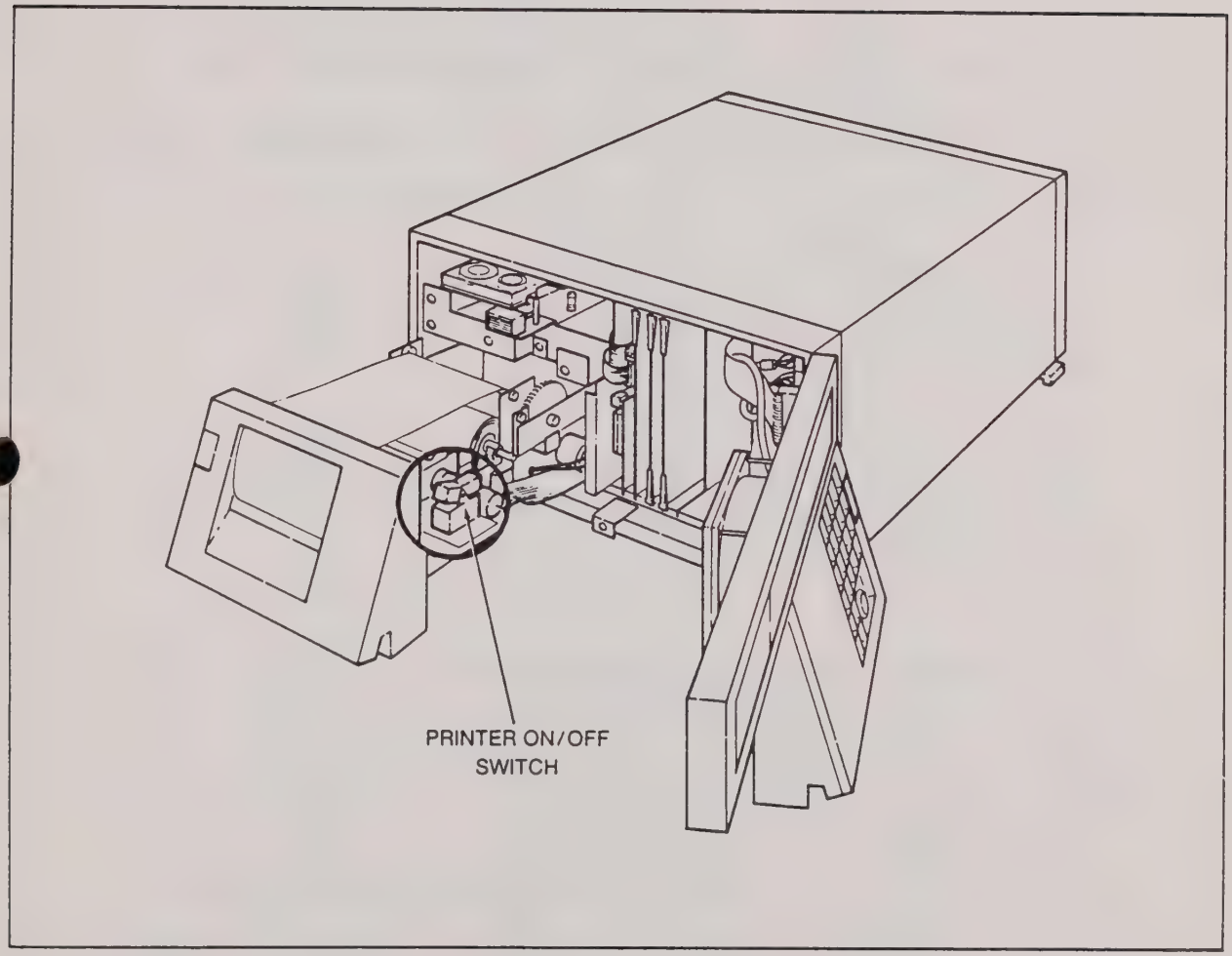


Figure 5-1. Printer On/Off Switch Location

7. Execute the Controller ROM self-test by performing the steps listed in Table 5-3.

Table 5-3. ROM Self-Test Programming Steps

STEP	KEYSTROKE	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>?
2	S	<S> SYSTEM DIAGNOSTICS
3	ENTER	S: DEVICE TO TEST <1-7>? 1
4	ENTER	S1: TEST <1,2>? 1
5	1	S1 <1> ROM CHECKSUM TEST
6	ENTER	

8. After a short delay, verify that the Data Logger displays:

[TEST PASSED]

9. If the unit fails the test, the following error message is displayed:

XUnn ROM CHECKSUM TEST FAILED

(Where X = C for Controller Assembly or M for Memory Assembly, and Unn = the reference designation of the faulty part, indicated by a one-or-two-digit number).

10. Execute the RAM self-test by performing the steps in Table 5-4.

Table 5-4. RAM Self-Test Programming Steps

STEP	KEYSTROKE(S)	DATA LOGGER PROMPT
1	EXIT	S1: TEST <1,2>? 2
2	ENTER	REALLY (DESTROYS USER PROGRAM) <Y,N>? N
3	Y	REALLY (DESTROYS USER PROGRAM) <Y,N>? Y
4	ENTER	

11. After a maximum of 30 seconds, verify that the Data Logger displays:

[TEST PASSED]

12. If the unit fails the test, the following error message is displayed:

    xUnn RAM TEST FAILED

    (Where X = C for Controller Assembly or M for Memory Assembly, and Unn = Reference designation symbol for the faulty RAM).

13. Depress the EXIT key three times to return to the main menu prompt.

14. Program a scan group and time interval using the steps given in Table 5-5.

Table 5-5. Scan Group and Time Interval Programming Steps

STEP	KEYSTROKE	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	K	<K> PROGRAM A SCAN GROUP
7	ENTER	SCAN GROUP NUMBER = 0
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	K: SCAN GROUP MENU CHOICE <1-5>? 1
10	ENTER	SCAN GROUP LABEL <40 CHRS MAX>=
11	SGL	SCAN GROUP LABEL <40 CHRS MAX>= SGL
12	ENTER	K: SCAN GROUP MENU CHOICE <1-5>? 2
13	ENTER	CL:
14	CO..9	CL: CO..0
15	ENTER	CL:
16	ENTER	K: SCAN GROUP MENU CHOICE <1-5>? 3
17	ENTER	K3: TRIGGER MODE <1-5>? 1
18	2	K3<2> TIME INTERVAL SCAN
19	ENTER	TIME INTERVAL =
20	00.00.15	TIME INTERVAL = 00:00:15
21	ENTER	K: SCAN GROUP MENU CHOICE <1-5>? 4
22	ENTER	K4: DEVICE <1-5>? 1
23	2	K4<2> PRINTER
24	ENTER	K42: TYPE OF DATA <1-4>? 1
25	2	K42<2> ALL DATA
26	ENTER	K4: DEVICE <1-5>? 3
27	EXIT	K: SCAN GROUP MENU CHOICE <1-5>? 5
28	EXIT	SCAN GROUP NUMBER = 0
29	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

15. Press the SCAN key. The SCAN indicator should light, and the Data Logger should print the following:

```
BEGIN SCAN GROUP 0        DD MMM YY  AA:AA:AA
SGL
C          0          .00000
C          1          .00000
C          2          .00000
C          3          .00000
C          4          .00000
C          5          .00000
C          6          .00000
C          7          .00000
C          8          .00000
C          9          .00000

END SCAN GROUP 0          DD MMM YY  BB:BB:BB

BEGIN SCAN GROUP 0        DD MMM YY  CC:CC:CC
SGL
C          0          .00000
C          1          .00000
C          2          .00000
C          3          .00000
C          4          .00000
C          5          .00000
C          6          .00000
C          7          .00000
C          8          .00000
C          9          .00000

END SCAN GROUP 0          DD MMM YY  BB:BB:BB
```

DD MM YY is the current date (day: month: year).
AA:AA:AA is the current time (hours : minutes : seconds). (Date and time will be correct only if they have been loaded.)
BB:BB:BB is between 2 and 4 seconds after time AA:AA:AA.
CC:CC:CC is exactly 15 seconds after time AA:AA:AA.

16. Press SCAN again. The Data Logger should stop printing and the SCAN indicator should extinguish.

17. Enter the steps in Table 5-6 to test the system clock:

Table 5-6. System Clock Self-Test Programming Steps

STEP	KEYSTROKE	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	Z	<Z> PROGRAM SYSTEM PARAMETERS
3	ENTER	Z:SYSTEM MENU CHOICE <1-7>? 1
4	2	Z<2> CALANDAR DATE AND TIME
5	ENTER	TIME =
6	23.59.45	TIME = 23:59:45
7	ENTER	DATE =
8	31 DEC 85	DATE = 31 DEC 85
9	ENTER	Z:SYSTEM MENU CHOICE <1-7>? 3
10	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

18. Press SCAN. The Data Logger should print:

```
BEGIN SCAN GROUP 0        1 JAN 86  AA:AA:AA
SGL
C          0          .00000
C          1          .00000
C          2          .00000
C          3          .00000
C          4          .00000
C          5          .00000
C          6          .00000
C          7          .00000
C          8          .00000
C          9          .00000
```

Where AA:AA:AA is 23:59:45 plus the time lapse between performing steps 14 and 15.

19. The functional capabilities performance test is complete.

Serial Link Performance Test

The serial link performance test verifies the ability of the Data Logger to communicate using the serial link. The serial link connects the controller to serial link options. One option must be installed in the mainframe to perform this test. Serial link options for the Data Logger include:

- Option 2280A-161 High Performance A/D Converter
- Option 2280A-168 Digital I/O Assembly
- Option 2280B-167 Counter/Totalizer
- Option 2280B-170 Analog Output

To run the Serial Link Performance Test, perform the following steps:

1. Disconnect the Data Logger line power cord, the dc input, and all high-voltage inputs from the data logger.

WARNING

HIGH VOLTAGE IS PRESENT INSIDE THE DATA LOGGER WHEN AC OR DC POWER IS CONNECTED. DISCONNECT POWER FROM THE DATA LOGGER BEFORE PERFORMING THE FOLLOWING STEPS.

2. Remove all serial link options (listed above) from the mainframe.

3. Select one serial link option and set the address on that option to 0 (see Figure 5-2), then reinstall that option.

4. Apply input power to the Data Logger (ac line or battery).

5. Turn the keyswitch to PROGRAM. The Data Logger should display:

```
[MAIN MENU CHOICE <M FOR MENU>? A        ]
```

6. Execute the serial link self-test by entering the steps given in Table 5-7.

Table 5-7. Serial Link Self Test Programming Steps

STEP	KEYSTROKE	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	S	<S> SYSTEM DIAGNOSTICS
3	ENTER	S: DEVICE TO TEST <1-7>?
4	7	S<7> SERIAL LINK
5	ENTER	CHANNEL NUMBER = CO
6	0	CHANNEL NUMBER = 0
7	ENTER	

7. After a short delay, verify that the Data Logger displays:

```
[TEST PASSED                    ]
```

8. The serial link performance test is complete.

The serial link self-test also provides a superficial operating test for any serial link options in the system. To test an individual suspected serial link option, run its performance test (located in that option's subsection in this manual.

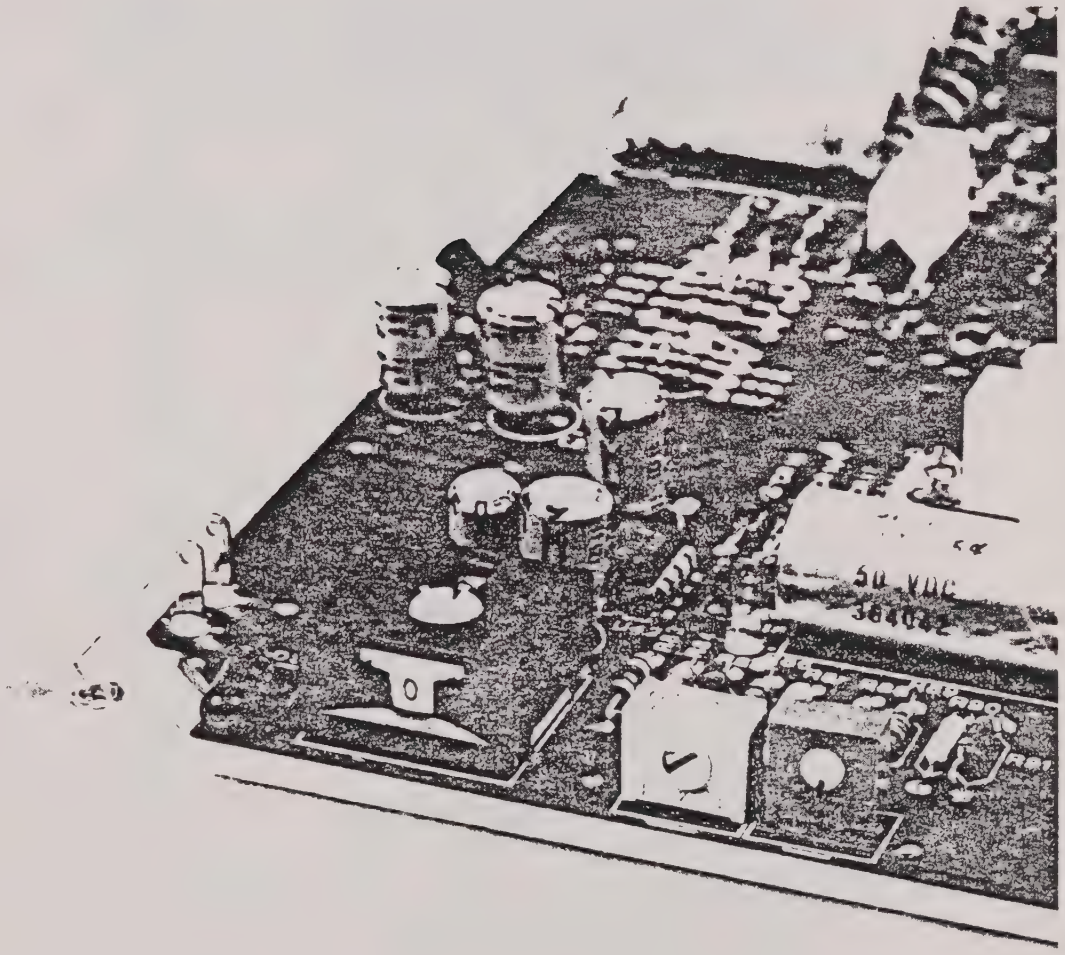


Figure 5-2. Serial Link Option Address Switch

Printer Performance Test

The printer performance test verifies that the printer is fully operational. Use the following procedure to test the printer.

1. Turn the keyswitch to OFF. Disconnect the Data Logger line power input and any other high-voltage inputs.

WARNING

HIGH VOLTAGE IS PRESENT INSIDE THE DATA LOGGER WHEN AC OR DC POWER IS CONNECTED. DISCONNECT POWER FROM THE DATA LOGGER BEFORE PERFORMING THE FOLLOWING STEPS.

2. Disconnect any external devices from the Data Logger mainframe (i.e. IEEE-488 or RS-232-C).

3. Verify correct line voltage settings and fuse ratings (refer to front panel access procedure and Figure 4-1 and Table 4-1 in Section 4), and verify that the printer on/off switch is in the ON position.

4. Reconnect the Data Logger power input.

5. Turn the front panel keyswitch to PROGRAM.

6. The Data Logger will display the following prompt:

```
[MAIN MENU CHOICE <M FOR MENU>? A       ]
```

7. Press M and observe the printer. The Data Logger should print the following information:

```
<A> PROGRAM A CHANNEL OR BLOCK
<F> PROGRAM AN ALARM LIST
<K> PROGRAM A SCAN GROUP
<P> PROGRAM PLOT PARAMETERS
<U> PROGRAM OUTPUT DEVICE PARAMETERS
<Z> PROGRAM SYSTEM PARAMETERS
<D> TRANSFER DATA
<T> PERFORM A TAPE FUNCTION
<L> LIST PROGRAM AND CONFIGURATION
<E> ERASE ALL OF PROGRAM MEMORY
<S> SYSTEM TEST
<M> PRINT THE MENU
```

9. If print alignment or intensity is not satisfactory, proceed to the printer calibration procedures in this section.

10. Turn the Data Logger keyswitch to PROGRAM and enter the steps given in Table 5-8.

Table 5-8. Programming Steps for Sample Plot Printout

STEP	KEYSTROKE	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) =
7	1	CHANNEL NUMBER (OR BLOCK) = 1
8	ENTER	PROGRAM COPY DELETE OR LIST? <P,C,D, OR L> P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
10	ENTER	AP: CHANNEL MENU CHOICE <1-5>? 1
11	3	AP<3> CHANNEL PROCEDURE
12	ENTER	CP:
13	C1=C1+1	CP: C1=C1+1
14	ENTER	CP:
15	ENTER	AP: CHANNEL MENU CHOICE <1-5>? 4
16	EXIT	A: CHANNEL FUNCTION <A-Z>? P
17	EXIT	CHANNEL NUMBER (OR BLOCK) = C1
18	EXIT	MAIN MENU CHOICE <M FOR MENU>? A
19	P	<P> PROGRAM PLOT PARAMETERS
20	ENTER	P: PLOT MENU CHOICE <1,2>? 1
21	ENTER	PLOT NUMBER <1-4>? 1
22	ENTER	CHANNEL TO PLOT =
23	1	CHANNEL TO PLOT = 1
24	ENTER	LEFT MOST VALUE = 0.0
25	ENTER	RIGHT MOST VALUE = 1.0
26	40	RIGHT MOST VALUE = 40
27	ENTER	PLOT NUMBER <1-4>? 2
28	EXIT	P: PLOT MENU CHOICE <1,2>? 2
29	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

11. Press the PLOT key. Verify that a printout similar to the one in Figure 5-3 is obtained.

12. Press PLOT again. Verify that the printer stops.

13. Verify that the PLOT key LED indicator extinguishes.

14. Cut the paper at the paper feed roll (not the take-up roll).

15. Press PLOT. Verify that the ALM ACK indicator lights before 40 values are plotted.

16. Press PLOT and verify that the plot mode LED goes off.

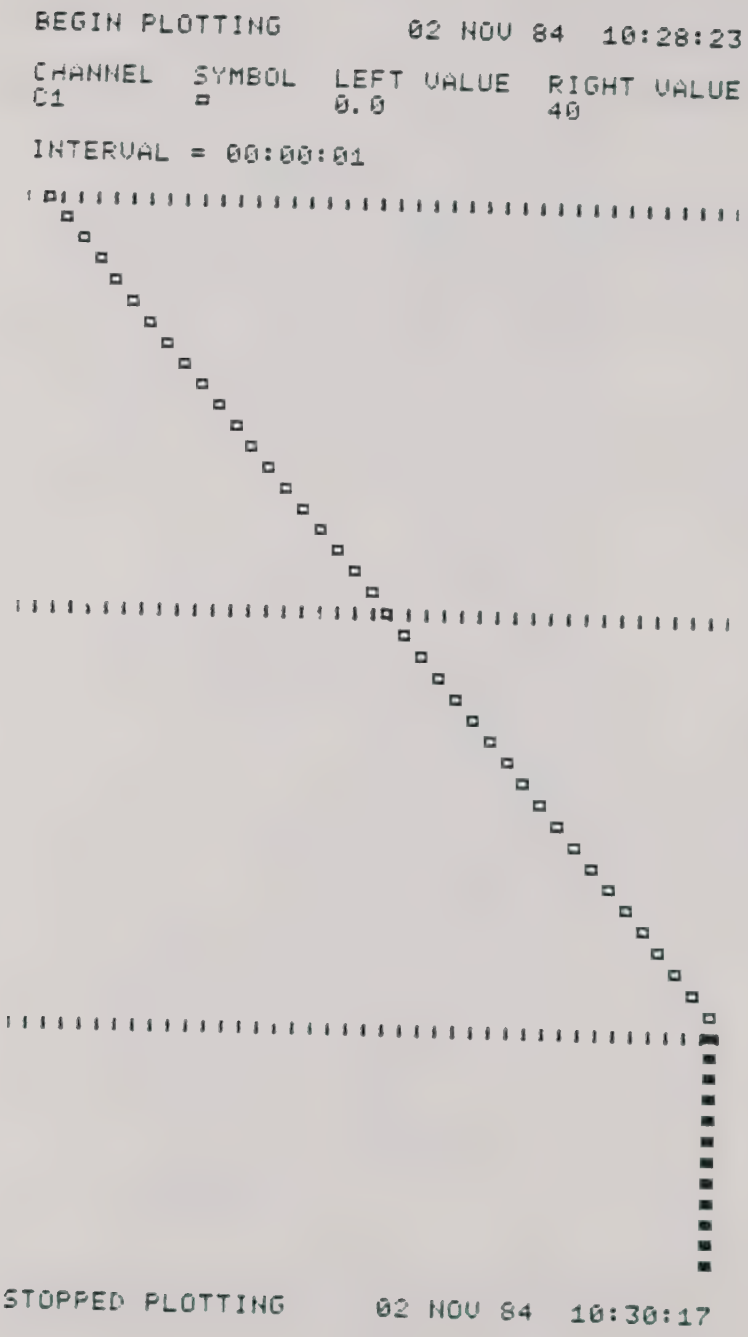

BEGIN PLOTTING 02 NOV 84 10:28:23
CHANNEL SYMBOL LEFT VALUE RIGHT VALUE
C1 0.0 40
INTERVAL = 00:00:01
STOPPED PLOTTING 02 NOV 84 10:30:17

Figure 5-3. Sample Plot Printout

17. Refeed the paper into the printer using the PAPER ADVANCE button on the front panel tape the ends of the paper together or attach the end to the take-up reel. (Figure 2-1 in Section 2 shows the location of the PAPER ADVANCE Button).

18. Press the ALM ACK key. Verify that the Data Logger displays:

    [PRINTER OUT OF PAPER]

19. Verify that the ALM ACK indicator turns off.

    NOTE
    It may be necessary to press ALM ACK key more than once to extinguish indicator.

20. The printer performance test is complete.

Interface Communication Test

The following test procedure checks the ability of the Data Logger to communicate through the interface options (Option 2280A-341 RS-232-C Interface or Option 2280A-342 IEEE-488 Interface). Although one interface option or the other must be installed for this test, this procedure is not a comprehensive test of the interface; it tests the mainframe. Since many applications do not require an interface, and the Data Logger mainframe can operate without one, this procedure is optional.

1. Turn the keyswitch to OFF, then disconnect the Data Logger power input.

2. Install either interface option in Port A (refer to Figure 4-3).

3. Verify that the option test switch is in the OFF position.

4. Remove any interface option that may be present Port B.

5. Reconnect the Data Logger power input.

6. Turn the keyswitch to PROGRAM.

7. Initiate the Port A bus test by performing the steps in Table 5-9.

Table 5-9. Port A Bus Test Programming Steps

STEP	KEYSTROKE	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	S	<S> SYSTEM DIAGNOSTICS
3	ENTER	S: DEVICE TO TEST <1-7>? 1
4	3	S<3> PORT A
*5	ENTER	S3: TEST <1-n>? 1
6	1	S3<1> DEVICE/CONTROLLER INTERFACE TEST
7	ENTER	

* (n = the number of the last test for the device installed at Port A)

8. Verify that after a short delay the Data Logger displays:

   [TEST PASSED]

9. Turn the keyswitch to OFF.

10. Move the interface option from Port A to Port B.

11. Turn the keyswitch to the PROGRAM position.

12. Initiate the Port B bus test by performing the steps given in Table 4-10.

Table 5-10. Port B Bus Test Programming Steps

STEP	KEYSTROKE	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	S	<S> SYSTEM DIAGNOSTICS
3	ENTER	S: DEVICE TO TEST <1-7>?
4	4	S<4> PORT B
*5	ENTER	S4: TEST <1-n>? 1
6	1	S4<1> DEVICE/CONTROLLER INTERFACE TEST
7	ENTER	

* (n = the number of the last test for the device installed in Port B)

13. Verify that after a short delay the Data Logger displays:

    [TEST PASSED

14. Turn the keyswitch to OFF.

15. Disconnect the Data Logger power input.

16. Return the data logger to its original configuration.

17. The remote interface communication performance test is complete.

CALIBRATION AND ADJUSTMENTS

Calibration and adjustment procedures for the Data Logger mainframe are divided into three separate sections: power supply calibration, audio tone volume adjustment, and printer calibration. Each section may be performed independently, but all three sections are required to ensure that the Data Logger conforms to its specifications. There is no established time interval requirement for calibration of the Data Logger.

Power Supply Calibration

The power supply voltage levels do not require calibration. Power Supply Assembly current-limit calibration is not required unless R56, R57, or U9 has been replaced. Periodic calibration is neither required nor recommended. Current-limit calibration must be performed at a Fluke Factory Service Center because of specialized calibration equipment necessary for this procedure.

Audio Tone Adjustment

Use the following procedure to adjust the audio tone volume emitted from the keyboard.

1. Disconnect the Data Logger power input.

WARNING
HIGH VOLTAGE IS PRESENT INSIDE THE FRONT PANEL WHEN AC OR DC POWER IS CONNECTED. USE EXTREME CAUTION WHILE PERFORMING THE FOLLOWING STEPS.

2. Loosen the three screws that secure the front panel to the case, and swing the front panel open (refer to the front panel access procedure).

3. Reconnect the Data Logger power input.

4. Turn the keyswitch to RUN.

5. Press the space key, and note the volume of the tone.

6. While pressing the space key, adjust R2 on the display circuit board (see Figure 5-4) until the tone is acceptable.

7. Turn the keyswitch to the OFF position, disconnect the power input, and close the front access panel.

8. Audio tone volume adjustment is complete.

Printer Calibration

Printer calibration is necessary only if the print quality is unacceptable. Use the following procedure to adjust print alignment and print density. An oscilloscope is required to perform this procedure.

1. Disconnect the Data Logger power input.

WARNING
HIGH VOLTAGE IS PRESENT INSIDE THE FRONT PANEL WHEN AC OR DC POWER IS CONNECTED. USE EXTREME CAUTION WHILE PERFORMING THE FOLLOWING STEPS.

2. Loosen the three captive screws that secure the Data Logger front panel, and swing the front panel open on the hinges (refer to the front panel access procedure).

3. Locate the printer self-test switch, the print-speed adjustment (R11), and the print-strobe adjustment (R13) on the printer interface board, and locate the contrast adjustment (R5) on the printer driver board (refer to Figure 5-5).

4. Reconnect the Data Logger power (ac line or battery).

5. Turn the keyswitch to RUN.

6. Press the printer self-test switch.

7. While observing the printout, set the print strobe adjustment (R13) so that the characters being printed are properly aligned.

8. If adjusting R13 does not align the characters properly, perform steps 9 and 10, then repeat step 7.

9. Set the oscilloscope timebase to 20 ms/div, and set the vertical gain to 2V/div. Connect the positive scope lead to printer test point TP74 and connect the negative scope lead to test point TP1.

10. Adjust the print speed (R11) until the time interval shown in the waveform diagram in Figure 5-6 is 55.5 ms +/- 1 ms.

11. Set contrast adjustment R5 fully clockwise, then adjust R5 to produce the desired print density.

12. Press the printer self-test switch. Printing should cease.

13. Turn the keyswitch OFF.

14. Disconnect the data logger power.

15. Secure the front panel.

16. Printer calibration is complete.

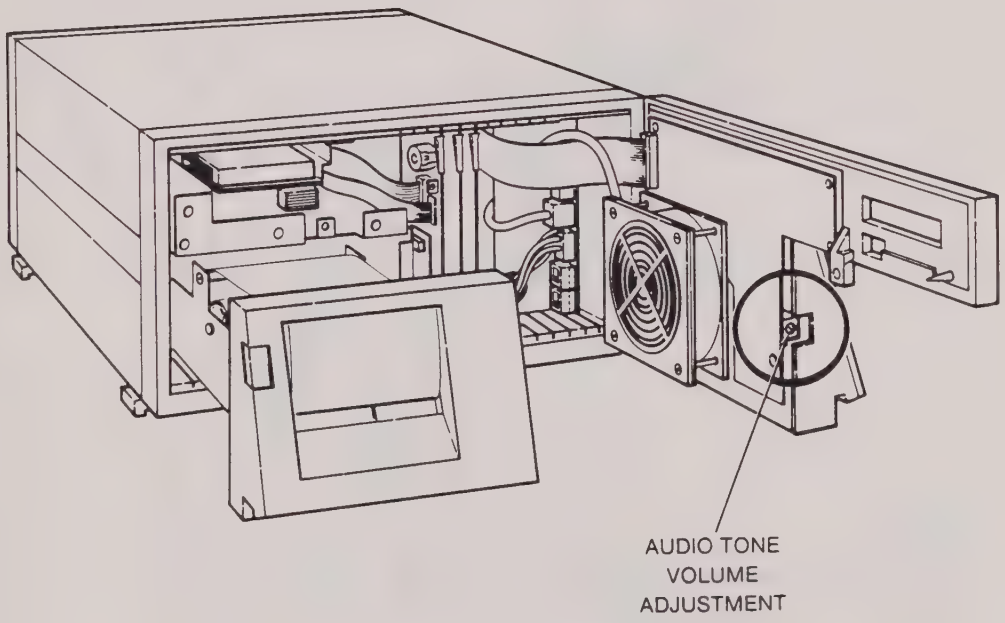


Figure 5-4. Audio Tone Volume Adjustment

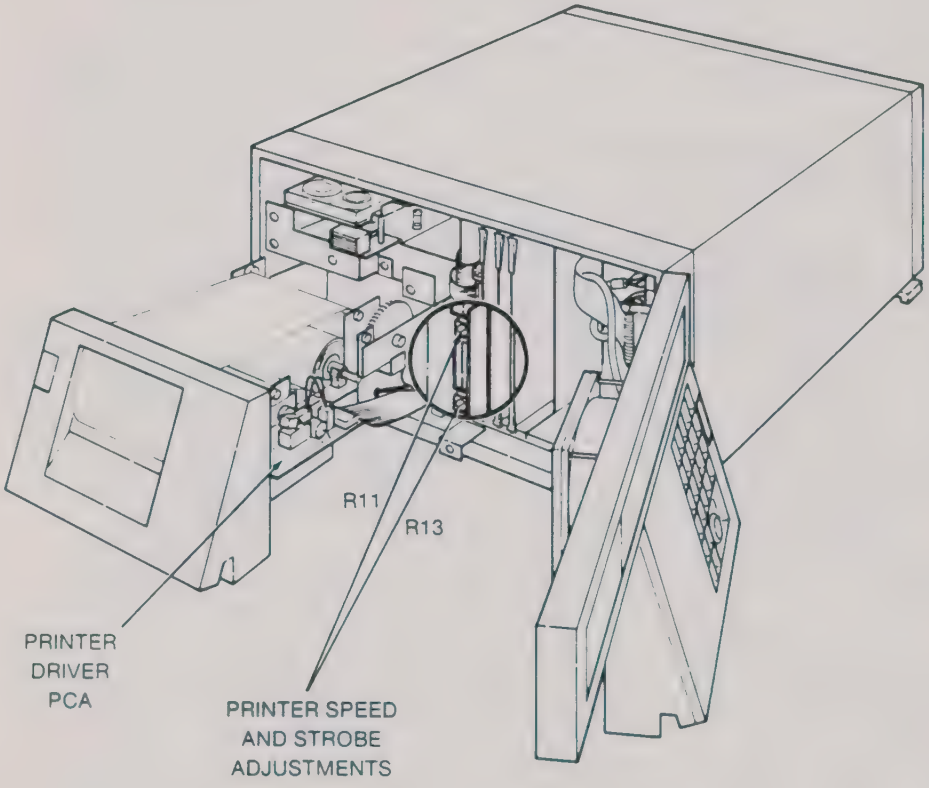


Figure 5-5. Printer Speed and Strobe Adjustments

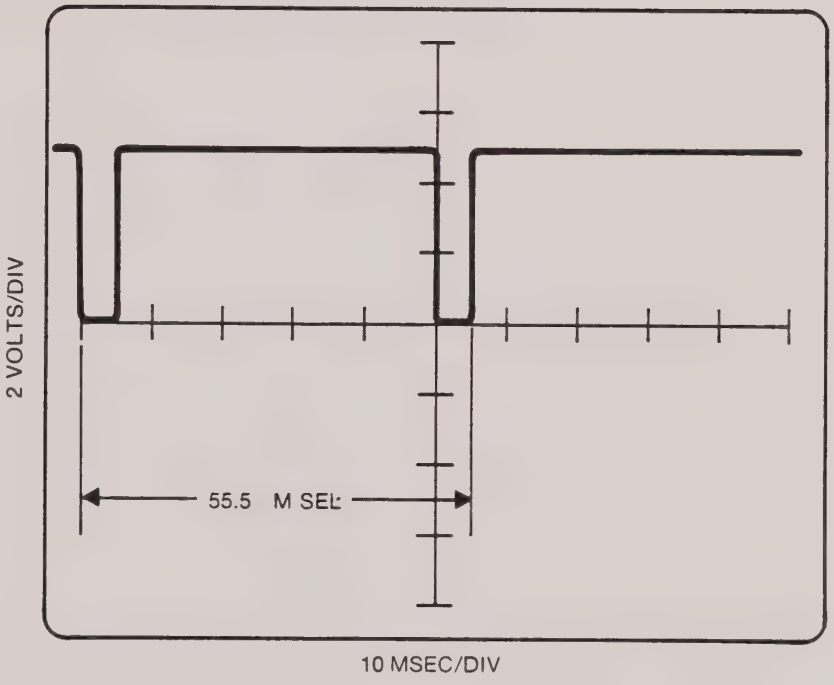


Figure 5-6. Print Speed Adjustment Waveform

SECTION 6

LIST OF REPLACEABLE PARTS

CONTENTS

Introduction 6-2
How to Obtain Parts 6-3

INTRODUCTION

An illustrated parts breakdown of the 2280 Series Data Loggers is provided in this section. A similar parts list is included in each option subsection of Sections 9, 10, and 11 for Data Logger options. Components are listed alphanumerically by assembly. Both electrical and mechanical components are listed by reference designation. Each listed part is shown in an accompanying illustration.

Parts lists include the following information:

- Reference designation
- Description
- Fluke stock number
- Federal supply code for manufacturers
- Manufacturer's part number
- Total quantity of components per assembly
- Recommended quantity: This entry indicates the number of spare parts necessary to support one to five instruments for a period of 2 years. This list presumes that common electronic parts are available of at the maintenance site. For maintenance for 1 year or more at an isolated site, it is recommended that at least one of each assembly in the instrument be stocked. In the case of optional subassemblies, plug-ins, etc., that are not always part of the instrument or are deviations from the basic instrument model, the REC QTY column lists the recommended spares quantity for the items in that particular assembly.

HOW TO OBTAIN PARTS

Components may be ordered directly from the manufacturer's part number, or from the John Fluke Manufacturing. Co., Inc. or an authorized representative by using the Fluke Stock Number. In the event the part ordered has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions if necessary.

To ensure prompt and efficient handling of your order, include the following information:

- Quantity
- Fluke Stock Number
- Description
- Reference designation
- Printed circuit board number and revision letter
- Instrument Model Number and Serial Number

A Recommended Spare Parts Kit for your basic instrument is available from the factory. This kit contains those items listed in the REC QTY column for the parts lists in the quantities recommended.

Parts price information is available from the John Fluke Manufacturing Co., Inc. or its representative. Prices are also found in the Fluke Replacement Parts Catalog, which is available on request.

CAUTION

Indicated devices are subject to damage by static discharge.

TABLE 6-1. 2280B FINAL ASSEMBLY
(SEE FIGURE 6-1.)

REFERENCE DESIGNATOR A-)NUMERICS---)		S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
A	1	*	DISPLAY PCA	718502	89536	718502	1		
A	2	*	PRINTER ASSEMBLY	646596	89536	646596	1		
A	3	*	PRINTER INTERFACE PCA	639344	89536	639344	1		
A	4	*	CONTROLLER PCA	752956	89536	752956	1		1
A	5	*	MEMORY PCA	752949	89536	752949	1		2
A	6	*	TRANSFORMER PCA	639245	89536	639245	1		
A	7	*	MOTHERBOARD PCA	639237	89536	639237	1		
A	8	*	POWER SUPPLY PCA	716084	89536	716084	1		
B	2		17 VDC, LOW TORQUE	615765	89536	615765	1		
E	1		STRAP,GROUNDING	578989	89536	578989	1		
E	2		TERMINAL,RING,22/16,CRIMP,INSULATED	649574	89536	649574	1		
F	1		FUSE,1/4 X 1-1/4,SLOW,1.5A,250V	109231	71400	MDX1R5			5
F	1		FUSE,1/4 X 1-1/4,SLOW,0.75A,250V	109256	71400	MDX3-4		5	6
F	2		FUSE,1/4 X 1-1/4,SLOW,10A,250V	109298	71400	MDX10	1	5	
H	1		SCREW,THD FORM,PHP,STL,7-19X3/4	447953	89536	447953	4		
H	2		SCREW,MACH,FHP,STL,6-32X3/8	114363	73734	182444	2		
H	3		SCREW,MACH,PHP,STL,6-32X3/4	114223	73734	19048	21		
H	4		SCREW,MACH,PHP SEMS,STL,6-32X5/8	272591	89536	272591	1		
H	5		SCREW,MACH,FHP,STL,6-32X5/8	114876	89536	114876	2		
H	6		SCREW,MACH,PHP SEMS,STL,6-32X3/8	177022	89536	177022	8		
H	7		SCREW,MACH,PHP SEMS,STL,6-32X1/2	177030	89536	177030	7		
H	8		SCREW,MACH,PHP,STL,4-40X3/8	152124	73734	19024	1		
H	9		SCREW,MACH,FHP,S STL,8-32X3/4	682880	89536	682880	13		
H	10		SCREW,MACH,FHP,STL,8-32X7/8	650119	89536	650119	4		
H	11		NUT,WELD TAB,SELF-LOCATE,STL,6-32	641654	89536	641654	20		
H	12		NUT,HEX,MINI,S.STL,6-32	110569	89536	110569	2		
H	13		WASHER,LOCK,INTRNL,STEEL,#6	110338	89536	110338	3		
H	14		SCREW,MACH,PHP,STL,8-32X5/8	114983	89536	114983	3		
H	15		WASHER,LOCK,INTRNL,STEEL,#8	110320	89536	110320	3		
H	16		PRESS INSERTED IN THERMOPLASTICS	631705	89536	631705	12		
H	17		INTERNAL THREAD, 8-32, NO SLOT	641696	89536	641696	24		
H	18		WASHER,LOCK,SPLIT,STEEL,#4	110395	89536	110395	1		
H	19		WASHER,FLAT,STEEL,#6,0.010 THK	111005	89536	111005	1		
H	20		WASHER,LOCK,INTRNL,STEEL,0.512 ID	641381	89536	641381	4		
H	21		SCREW,MACH,FHP,STL,8-32X5/8	184994	89536	184994	10		
H	22		SCREW,MACH,FHP,STL,8-32X1/4	276774	89536	276774	1		
H	23		SCREW,SET,HH,STL,M3X0.5X6	696401	89536	696401	1		
H	24		SCREW,MACH,PHP SEMS,STL,6-32X3/8	177022	89536	177022	16		
H	25		WASHER,FLAT,STEEL,#6,0.031 THK	110270	89536	110270	1		
H	26		SCREW,MACH,PHP SEMS,STL,4-40X3/8	281196	89536	281196	4		
H	27		SCREW,MACH,FHUP,STL,6-32X3/8	271817	89536	271817	4		
H	28		SCREW,MACH,FHP,STL,4-40X1/2	149047	89536	149047	2		
H	29		SCREW,THD FORM,THP,STL,6-20X3/8	156489	89536	156489	1		
H	30		SCREW,MACH,PHP SEMS,STL,8-32X3/8	436030	89536	436030	4		
H	31		NUT,MACH,HEX,BR,4-40	152074	89536	152074	2		
H	32		WASHER,LOCK,SPLIT,STEEL,#4	110395	89536	110395	2		
H	33		SCREW,MACH,PHP,STL,3-56X1/4	114298	89536	114298	2		
H	34		WASHER,LOCK,INTRNL,STEEL,#3	110783	89536	110783	2		
H	35		SCREW,MACH,PHP SEMS,STL,6-32X1/4	178533	89536	178533	4		
H	36		WASHER,FLAT,STEEL,#6,0.010 THK	111005	89536	111005	4		
H	37		SCREW,MACH,PHP,STL,6-32X1/2	152173	89536	152173	2		
H	38		WASHER,LOCK,SPLIT,STEEL,#6	110692	89536	110692	2		
H	39		WASHER,LOCK,INTRNL,STEEL,#6	110338	89536	110338	2		
H	40		WASHER,FLAT,BRASS,#6,0.028 THK	111310	89536	111310	4		
H	41		POUROUS,(OPEN CELL)FOAM, POLYESTER	543942	89536	543942	1		
H	42		SCREW,THD FORM,PHP,STL,6-20X3/8	288266	89536	288266	1		
H	43		SCREW,MACH,PHP SEMS,STL,6-32X3/8	177022	89536	177022	5		
H	44		SCREW,MACH,FHS,STL,6-32X2	615815	89536	615815	2		
H	45		SCREW,MACH,FHS,ST,6-32X2-3/4	650028	89536	650028	1		
H	46		SCREW,MACH,FHS,STL,6-32X2-1/4	649871	89536	649871	1		
H	47		PANEL, S/S, SLOTTED DRIVE, 6-32,BLACK	682617	89536	682617	3		
H	48		WASHER,LOCK,SPLIT,STEEL,#6	110692	89536	110692	4		
H	49		WASHER,LOCK,INTRNL,STEEL,0.387 ID	129957	78189	1220-05	1		
H	50		WASHER,LOCK,INTRNL,STEEL,#6	110338	89536	110338	2		
H	51		NUT,MACH,HEX,STL,3/8-32	110510	73734	8009NP	1		
H	52		NUT,HEX,MINI,S.STL,6-32	110569	89536	110569	5		
H	53		WASHER,FLAT,STEEL,#6,0.010 THK	111005	89536	111005	5		
H	54		CONN,D-SUB,JACK SCREW,4-40	448092	89536	448092	4		
H	55		WASHER,LOCK,INTRNL,STEEL,#4	110403	89536	110403	4		
H	56		SCREW,MACH,PHP SEMS,STL,6-32X3/4	309963	89536	309963	8		
H	57		SCREW,MACH,PHP SEMS,STL,6-32X3/8	177022	89536	177022	11		
H	58		NUT,HEX,MINI,S.STL,6-32	110569	89536	110569			
H	59		WASHER,LOCK,SPLIT,STEEL,#6	110692	89536	110692			
MP	1		FRONT BEZEL, MACHINED & PAINTED	660829	89536	660829	1		

TABLE 6-1. 2280B FINAL ASSEMBLY
(SEE FIGURE 6-1.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
MP 2		GASKET,SHIELDING,STEEL MESH W/CORE	714071	89536	714071	3		
MP 3		GASKET, REAR	712067	89536	712067	1		
MP 4		FRONT PANEL	578872	89536	578872	1		
MP 5		BRACKET,OPTION SUPPORT	578898	89536	578898	1		
MP 6		COVER, TOP	712216	89536	712216	1		
MP 7		COVER, BOTTOM	712224	89536	712224	1		
MP 8		BRACKET,CARD GUIDE	578948	89536	578948	1		
MP 9		BRACKET,ACCESS PANEL ALIGNMENT	583534	89536	583534	1		
MP 10		COVER, LINE CONNECTOR	716092	89536	716092	1		
MP 11		HANDLE RETAINER	579052	89536	579052	4		
MP 12		HANDLE,STRAP	630178	89536	630178	2		
MP 13		BRACKET,ACCESS PANEL MOUNT	618454	89536	618454	1		
MP 14		BRACKET,HANDLE SUPPORT	632414	89536	632414	4		
MP 15		PCB RETAINER	728188	89536	728188	1		
MP 16		HANDLE,MODIFIED	633362	89536	633362	2		
MP 17		CHASSIS SIDE	536888	89536	536888	2		
MP 18		CHASSIS BASE	536896	89536	536896	2		
MP 19		SHIELD,CARD GUIDE	648832	89536	648832	1		
MP 20		FUSE HLDR,CAP,1/4 X 1-1/4 FUSE	460238	61935	031.1666	2	5	
MP 21		FUSE HLDR,BODY W/NUT,HIGH	375188	61935	031.1653	2		
MP 22		FOOT, SINGLE BAIL TYPE (DARK UMBER)	653923	89536	653923	4		
MP 23		CLAMP,CABLE,SELF ADHESIVE,1.00X.88	513606	89536	513606	3		
MP 24		ADHESIVE BACK., ACCEPT CABLE .17"X2"	658831	89536	658831	1		
MP 25		SLEEV,POLYOL,SHRINK,.750-.375ID,CLEAR	423830	89536	423830			
MP 26		SLEEV,POLYOL,SHRINK,.187-.093ID,BLACK	113852	89536	113852			
MP 27		TAPE,FOIL,ALUM,CONDUCT,1/2"WIDE	696583	89536	696583	3		
MP 28		CHASSIS,PRINTER	610501	89536	610501	1		
MP 29		BRACKET,PAPER GUIDE	610626	89536	610626	1		
MP 30		BUTTON,PRINTER	604660	89536	604660	1		
MP 31		MANDREL,40COLUMN SUPPLY	586529	89536	586529	1		
MP 32		SPACER,PRINTER SUPPORT	604645	89536	604645	4		
MP 33		SPRING,PRINTER	610527	89536	610527	1		
MP 34		SPACER,PRINTER CHASSIS	604652	89536	604652	1		
MP 35		MANDREL,REWIND 40 COL.	610485	89536	610485	2		
MP 36		PRINTER FRONT PAINTED	647743	89536	647743	1		
MP 37		BRKT,PAPER HOLD DOWN	610519	89536	610519	1		
MP 38		LATCH,PRINTER	610873	89536	610873	1		
MP 39		BRKT,MOTOR MOUNT	610535	89536	610535	1		
MP 40		PRINTER SLIDE,MODIFIED	610691	89536	610691	1		
MP 41		SPACER,PRINTER PAPER	604637	89536	604637	2		
MP 42		DECAL, ROCKER SWITCH	605857	89536	605857	1		
MP 43		BRACKET, MANDREL ALIGNMENT	579094	89536	579094	1		
MP 44		PIN, PRINTER FRONT	650853	89536	650853	2		
MP 45		SPRING,COIL,COMP,SQUARED END,M WIRE	615484	89536	615484	1	1	
MP 46		HEAT SENSITIVE PAPER FOR OLIVETT#1840	631853	89536	631853			
MP 47		GROMMET RUBBER, FOR 3/16 DIA HOLE	102772	89536	102772	1		
MP 48		SPACER,RND,ALUM,0.156IDX0.250	153155	89536	153155	2		
MP 49		RING,RET,EXT,FLAT,STEEL,0.385 ID	658815	89536	658815	1		
MP 50		SPACER,RND,NYLON,6-32X1.063	104174	89536	104174	2		
MP 51		ACCESS PANEL,FINISHED	749820	89536	749820	1		
MP 52		SHIELD, ANTI STATIC	660753	89536	660753	1		
MP 53		HINGE,ACCESS PANEL	578880	89536	578880	1		
MP 54		BRKT,TORSION SPRING	610618	89536	610618	1		
MP 55		CARTRIDGE DOOR	749770	89536	749770	1		3
MP 56		BRACKET,SWITCH MOUNTING	613067	89536	613067	1		
MP 57		SPRING,CASSETTE DOOR	686287	89536	686287	1		
MP 58		LOCK,MODIFIED	655670	89536	655670	1		
MP 59		SLEEV,POLYOL,SHRINK,1.00-.500ID,CLEAR	423848	89536	423848			
MP 60		SLEEV,POLYOL,SHRINK,.187-.093ID,BLACK	113852	89536	113852			
MP 61		REAR BEZEL,FINISHED	749812	89536	749812	1		
MP 62		DECAL,CORNER	605691	89536	605691	2		
MP 63		DECAL, FUSE RATING	585075	89536	585075	1		
MP 64		NAMEPLATE, SERIAL -REAR PANEL-	472795	89536	472795	1		
MP 65		DECAL, PAPER LOAD	605881	89536	605881	1		
MP 66		DECAL,LENS	585091	89536	585091	1		4
MP 67		DUST COVER,PRINTER	579144	89536	579144	1		
MP 68		LATCH,PRINTER DOOR	616151	89536	616151	1		
MP 69		LATCH,PROGRAMMER DOOR	616144	89536	616144	1		
MP 70		DOOR,PROGRAMMER	578963	89536	578963	1		
MP 71		SPRING,COIL,COMP,SQUARED END,M WIRE	615484	89536	615484	2		
MP 72		OPTION COVER MODIFIED	633255	89536	633255	3		
MP 73		COVER,SMALL OPTION	578955	89536	578955	1		
MP 74		LABEL,2280A OPTION BOX	707885	89536	707885	1		
MP 75		DECAL,OPTION NUMBERS	698399	89536	698399			

TABLE 6-1. 2280B FINAL ASSEMBLY
(SEE FIGURE 6-1.)

REFERENCE DESIGNATOR A-)NUMERICS---)	S	DESCRIPTION	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOTE
MP 76		DECAL, OPTION NUMBERS SET 2	707711	89536	707711			
MP 77		HEAT SENSITIVE PAPER FOR OLIVETT#1840	631853	89536	631853	2		
MP 78		FILLER PANEL,FRONT	578997	89536	578997			
MP 79		FILLER PANEL,REAR	610212	89536	610212			
MP 80		LABEL,2280A SHIPPING IDENTIFIER	707893	89536	707893	1		
MP 81		LABEL,I.P.INSTRUMENTATION	707901	89536	707901	1		
MP 82		OPERATOR PROGRAMMER KEYBOARD	585067	89536	585067	1		
MP 83		280-6Y-N-DOT MATRIX PU-1840-4-P	603233	89536	603233	1		
MP 84		DUST COVER,LENS	610790	89536	610790	1		
MP 85		NON METALLIC,.8MOD,3MM FACE WIDTH	615492	89536	615492	1		
MP 86		.8 MODULE, 4MM FACE WIDTH, 6TEETH	615518	89536	615518	1		
MP 87		CUTTER PAPER	632406	89536	632406	1		
MP 88		SHIPPING BOX 2280A,2281A	686097	89536	686097	1		
MP 89		ACCESSORY BOX, 2280A	686105	89536	686105	1		
MP 90		CAP,REAR END	686212	89536	686212	1		
MP 91		CAP,FRONT END	686220	89536	686220	1		
MP 92		BAG, LARGE ACCESSORY	698027	89536	698027	1		
MP 93		BAIL, INSTRUMENT	707877	89536	707877	2		
P 25		CONN,D-SUB,SOLDER CUP,9 PIN	347617	89536	347617	1		
S 1		ROTARY SWITCH	604488	89536	604488	1		
S 2		SWITCH,ROCKER,SPDT	615773	89536	615773	1		
TB 1		SINGLE ROW, .375 CENTERS, 2 TERMINALS	615641	89536	615641	1		
TM 1		2280A-PROGRAMMING FORMS	656769	89536	656769	1		
TM 2		2280 SERIES MANUAL SET	753236	89536	753236	1		
TM 4		2280A-START UP GUIDE	737320	89536	737320	1		
W 1		CABLE ASSY,DISPLAY	605733	89536	605733	1		
W 2		CABLE ASSY, CHASSIS GROUND	729665	89536	729665	1		
W 3		CABLE ASSY,12 VOLT POWER	610782	89536	610782	1		
W 4		CABLE ASSY ACCESS PANEL GROUND	648816	89536	648816	1		
W 5		CABLE ASSY, PRINTER GROUND	648808	89536	648808	1		
W 6		CABLE ASSY, FUSE	610857	89536	610857	1		
W 7		CABLE ASSY,AC POWER	580795	89536	580795	1		
W 8		CABLE ASSY, POWER GROUND	581678	89536	581678	1		
W 9		CABLE ASSY,ROCKER SWITCH	610915	89536	610915	1		
W 10		CABLE ASSY MOTOR	610907	89536	610907	1		
W 11		CABLE ASSY,HINGE	648790	89536	648790	1		
W 12		CABLE ASSY PROGRAMMER KEY	610865	89536	610865	1		
W 13		CABLE,POWER SWITCH	580787	89536	580787	1		
W 14		CORD,LINE,5-15/IEC,3-18AWG,SVT	343723	89536	343723	1		
W 15		WIRE,PVC,UL1015,18AWG,BTIN,RED	135517	89536	135517			
W 16		CABLE ASSY,FAN	610899	89536	610899	1		
WT 1		PVC,ADHESIVE BACKED, 5/16,5/16,3/4SQ	682237	89536	682237	2		

NOTE 1 = ORDER P/N 639260 FOR 2280A
ORDER P/N 753020 FOR 2285B

NOTE 2 = ORDER P/N 731745 FOR 2280A
ORDER P/N 753012 FOR 2285B

NOTE 3 = ORDER P/N 610840 FOR 2280A

NOTE 4 = ORDER P/N 749788 FOR 2285B

NOTE 5 = USE FOR LINE VOLTAGES BETWEEN 90-132V AC.

NOTE 6 = USE FOR LINE VOLTAGES BETWEEN 198-250V AC.

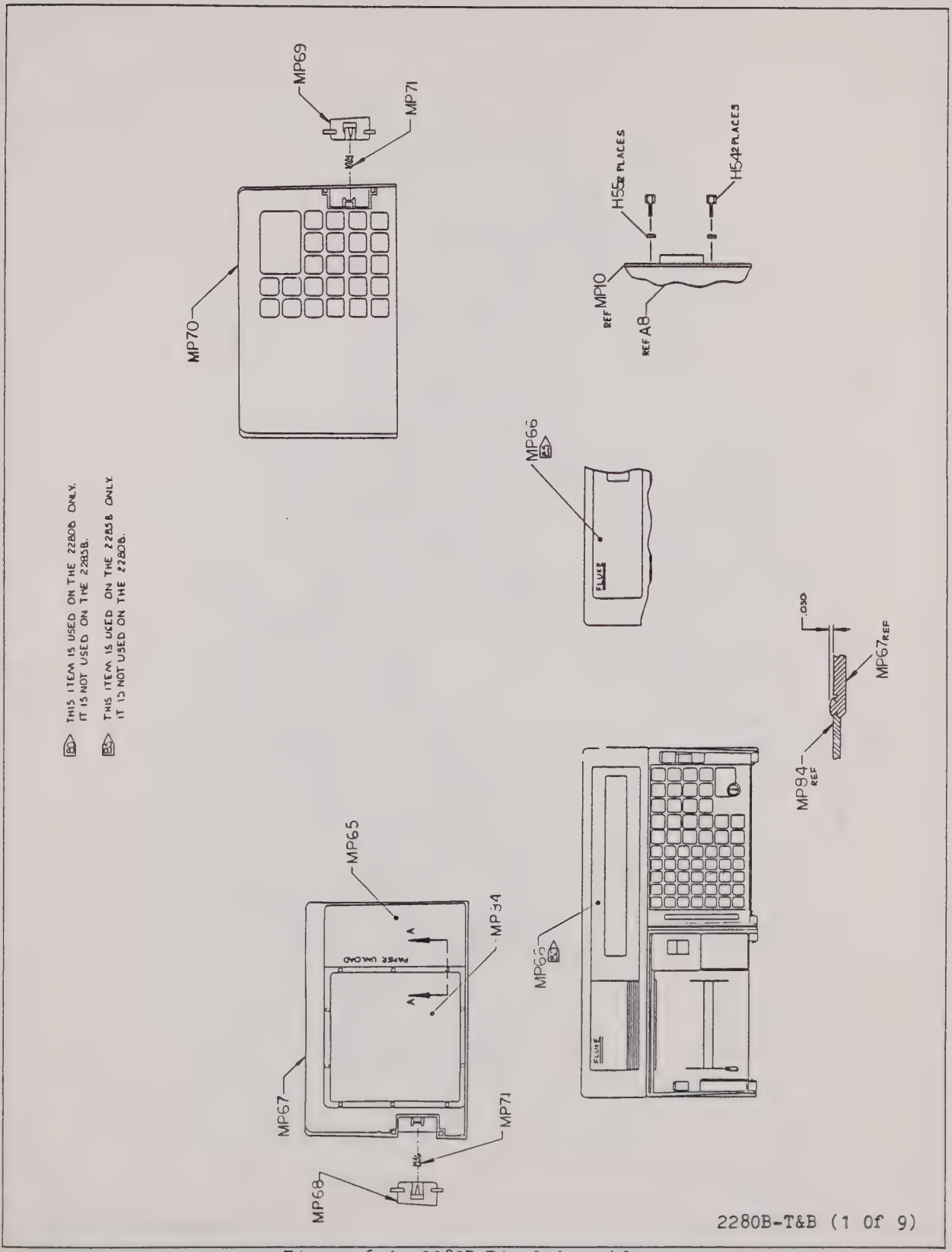


Figure 6-1. 2280B Final Assembly

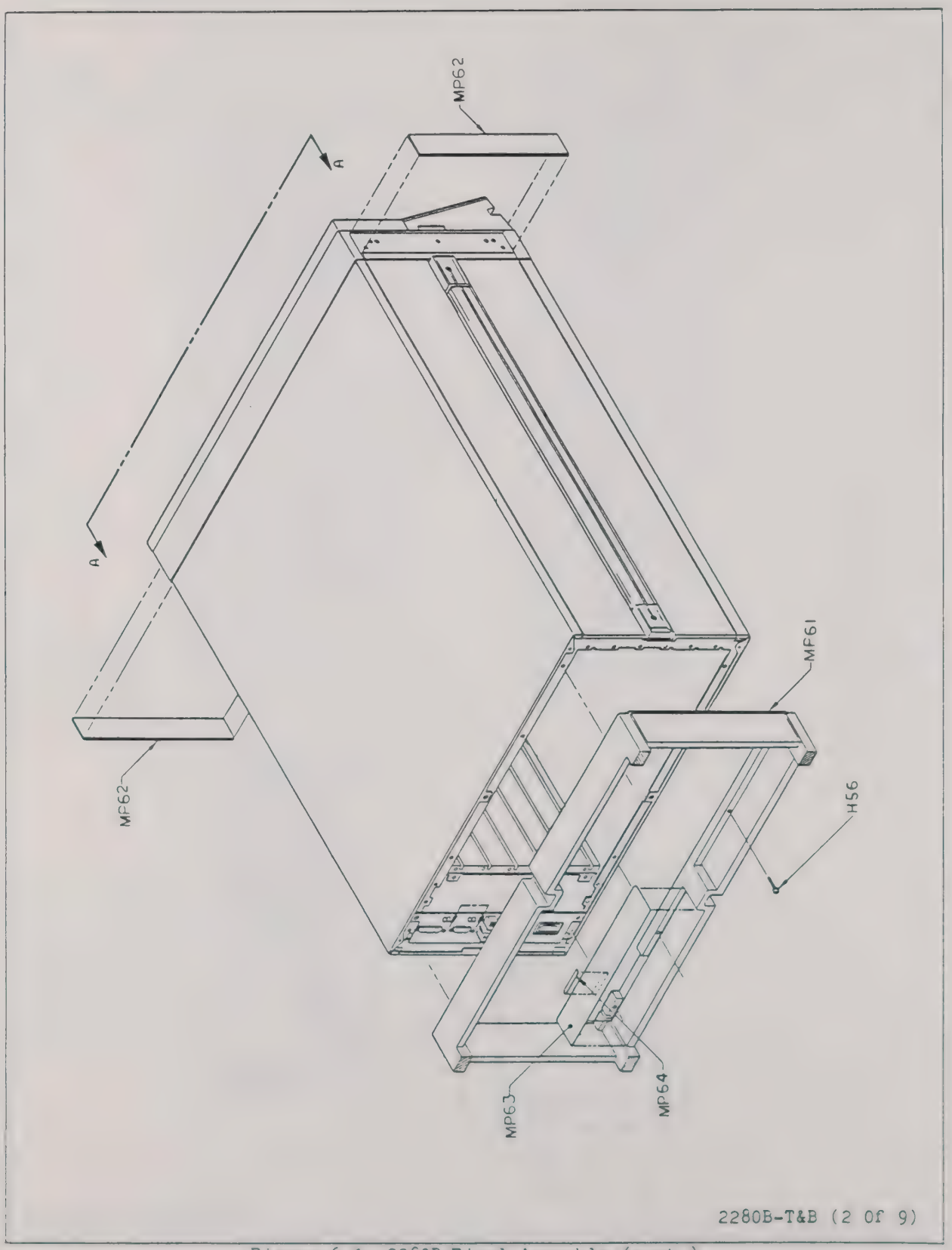
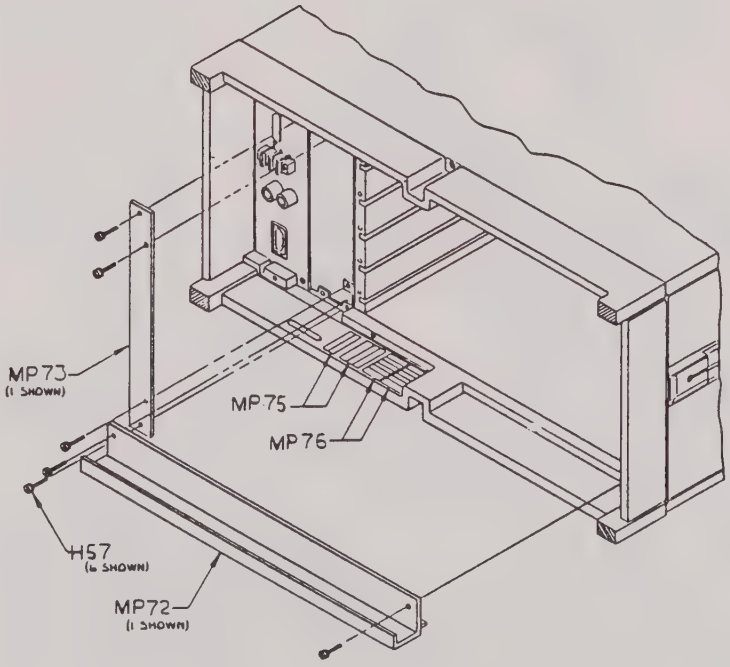


Figure 6-1. 2280B Final Assembly (cont.)



2280B-T&B (3 Of 9)

Figure 6-1. 2280B Final Assembly (cont.)

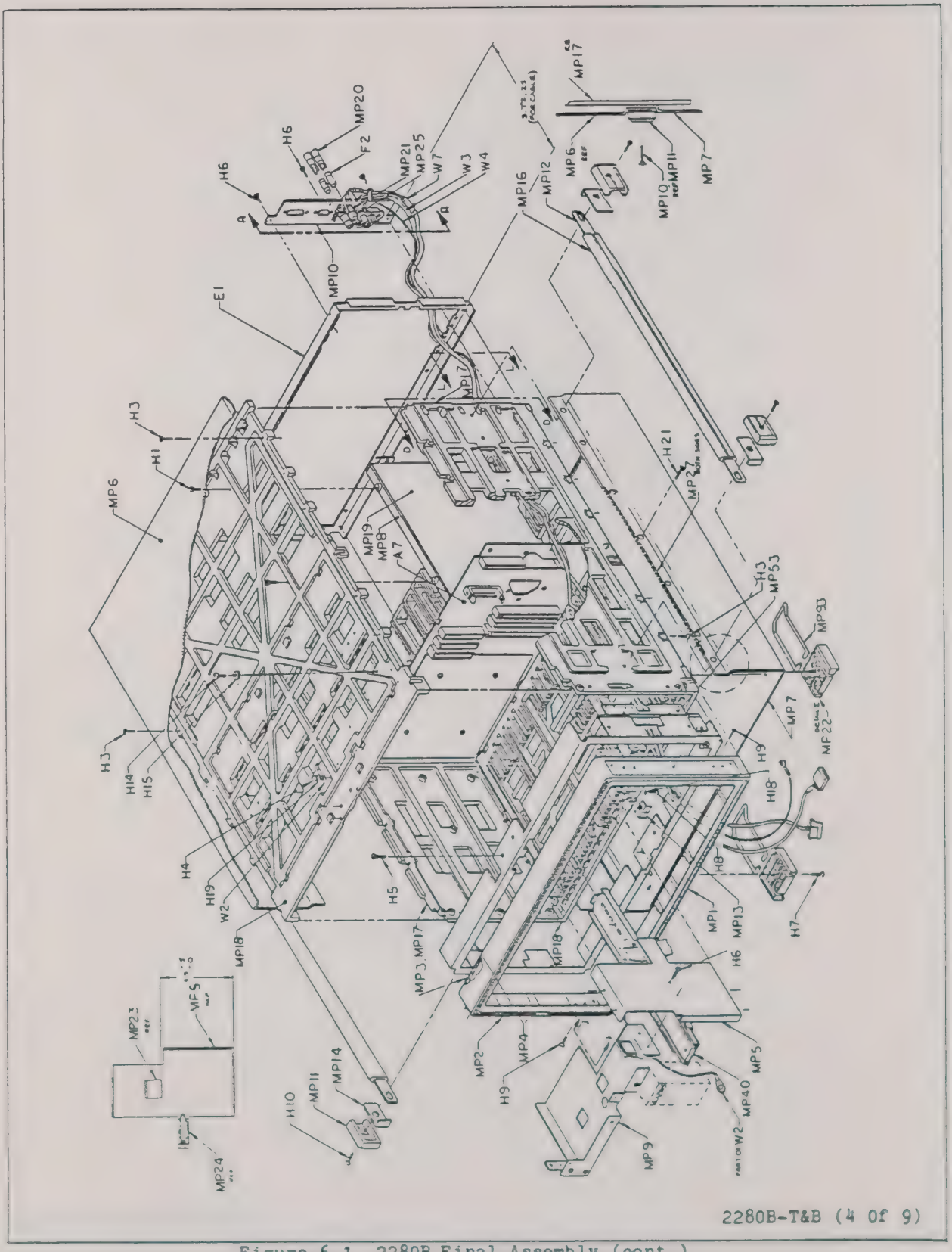


Figure 6-1. 2280B Final Assembly (cont.)

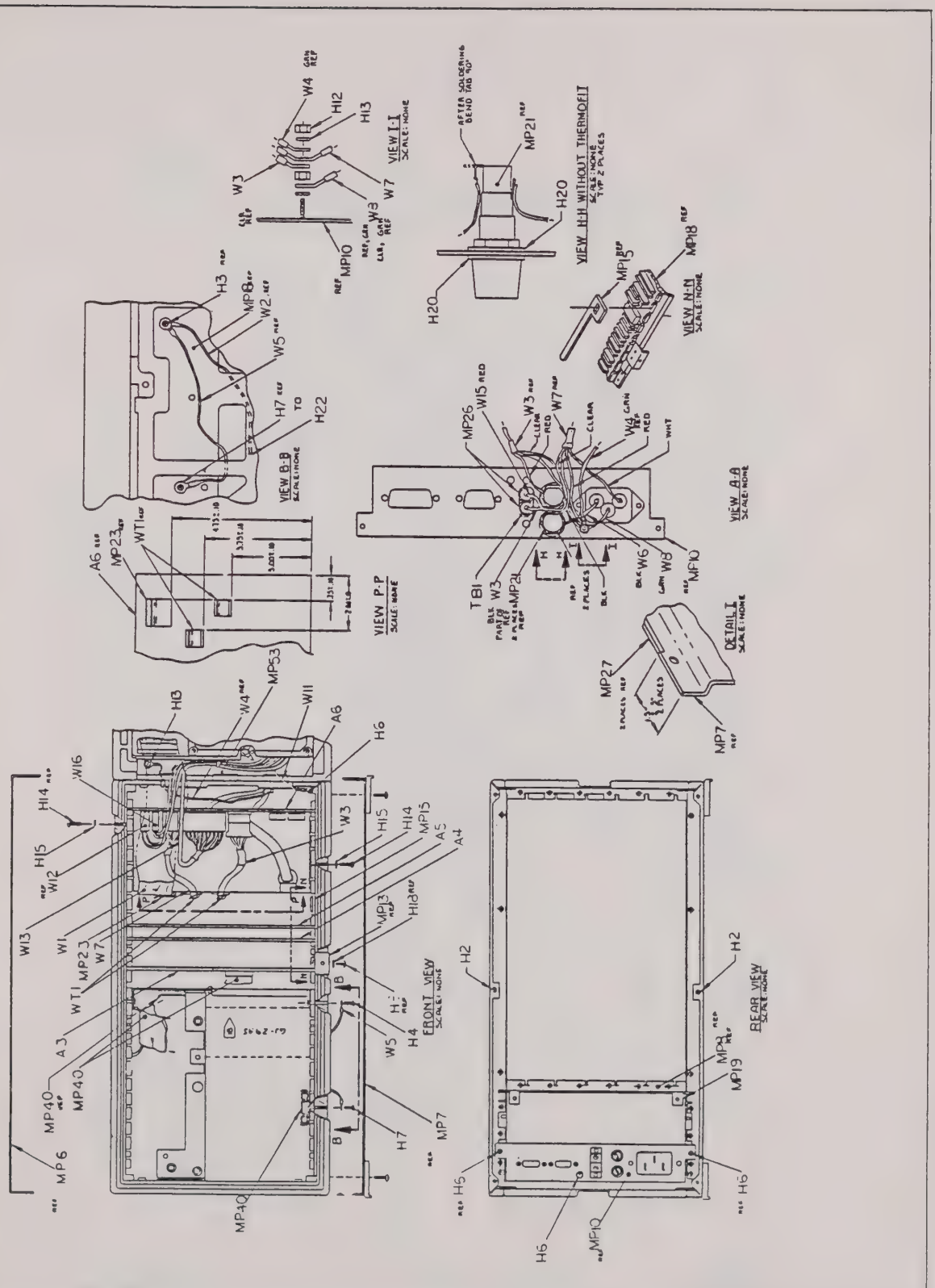


Figure 6-1. 2280B Final Assembly (cont.)

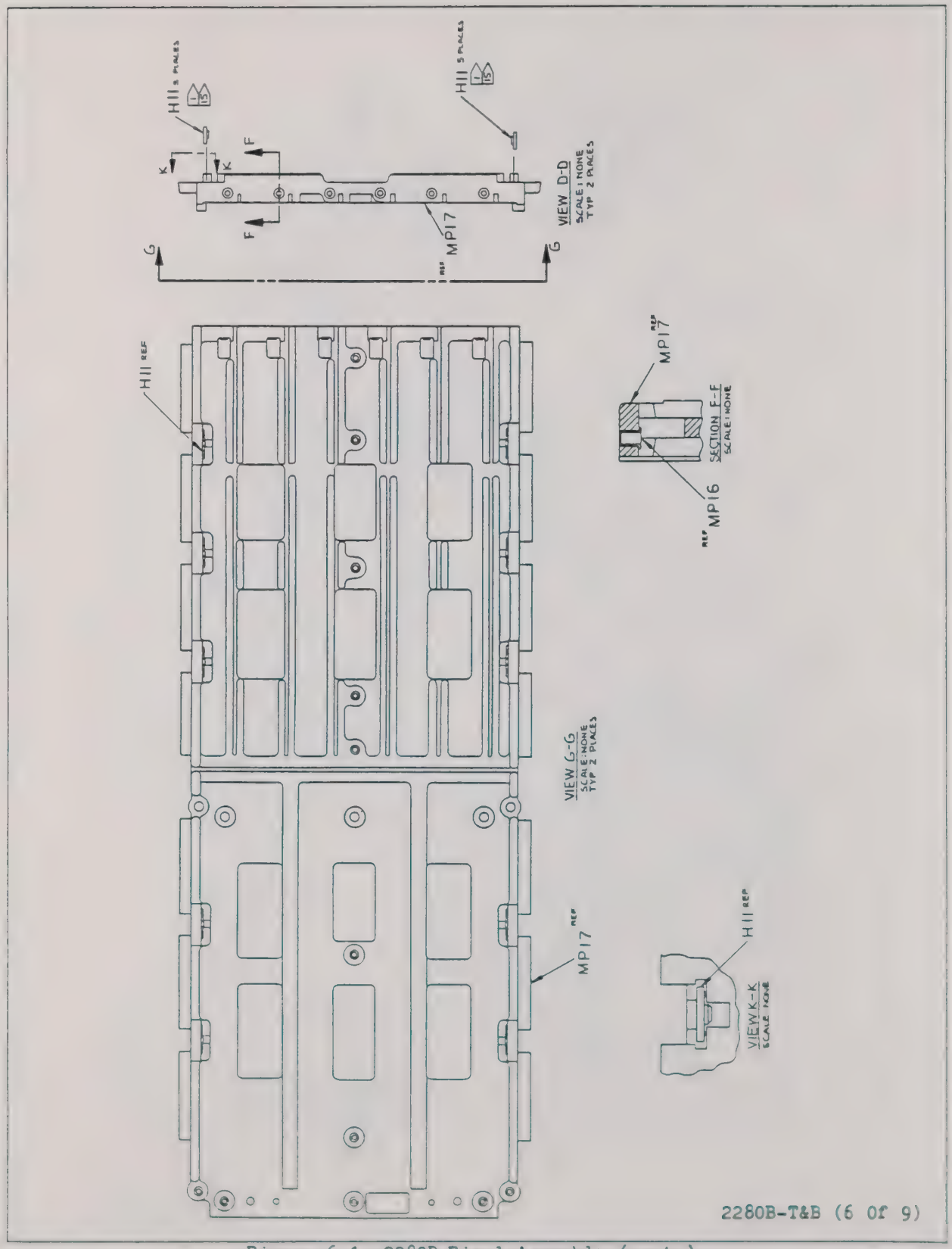
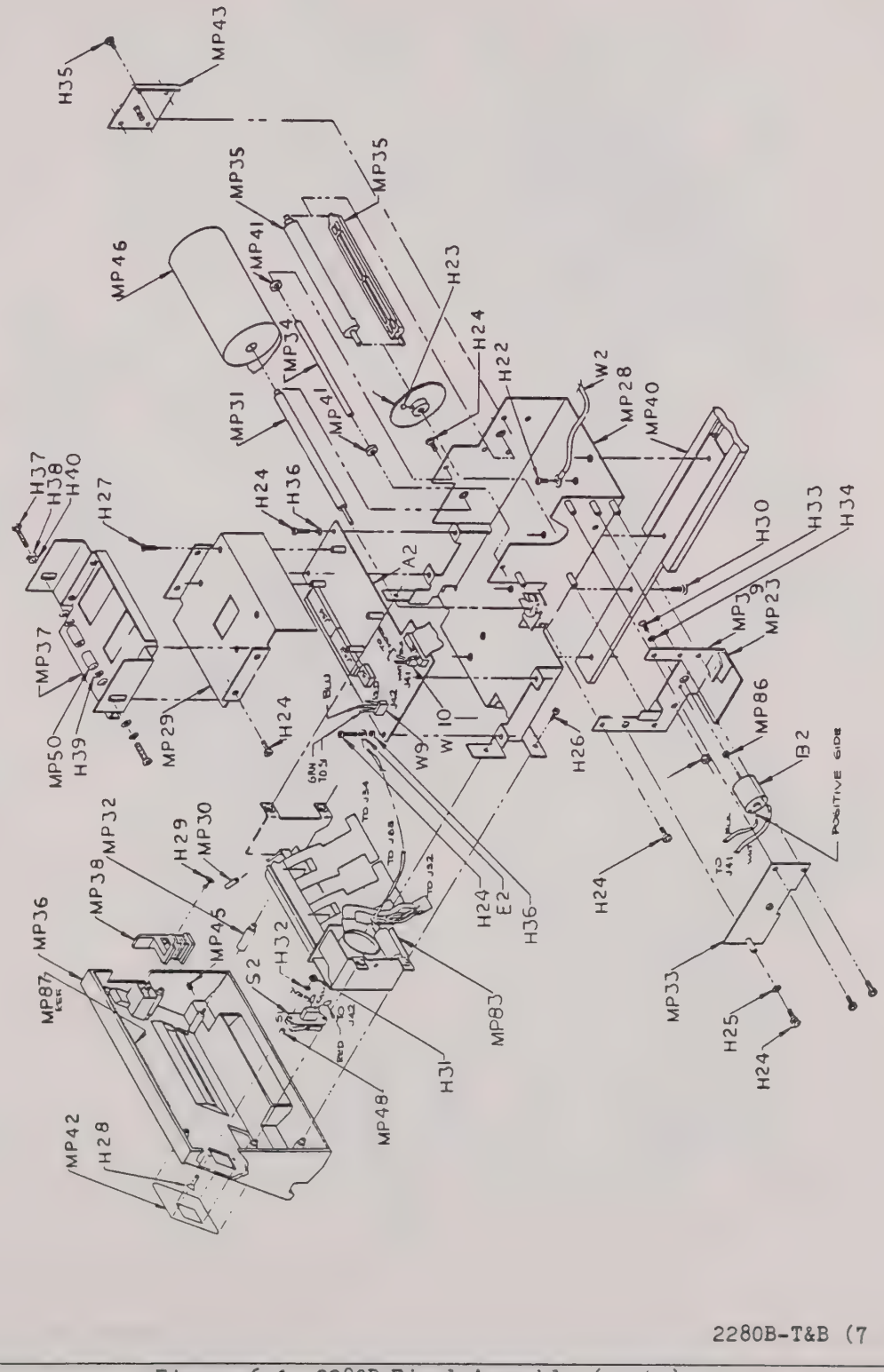
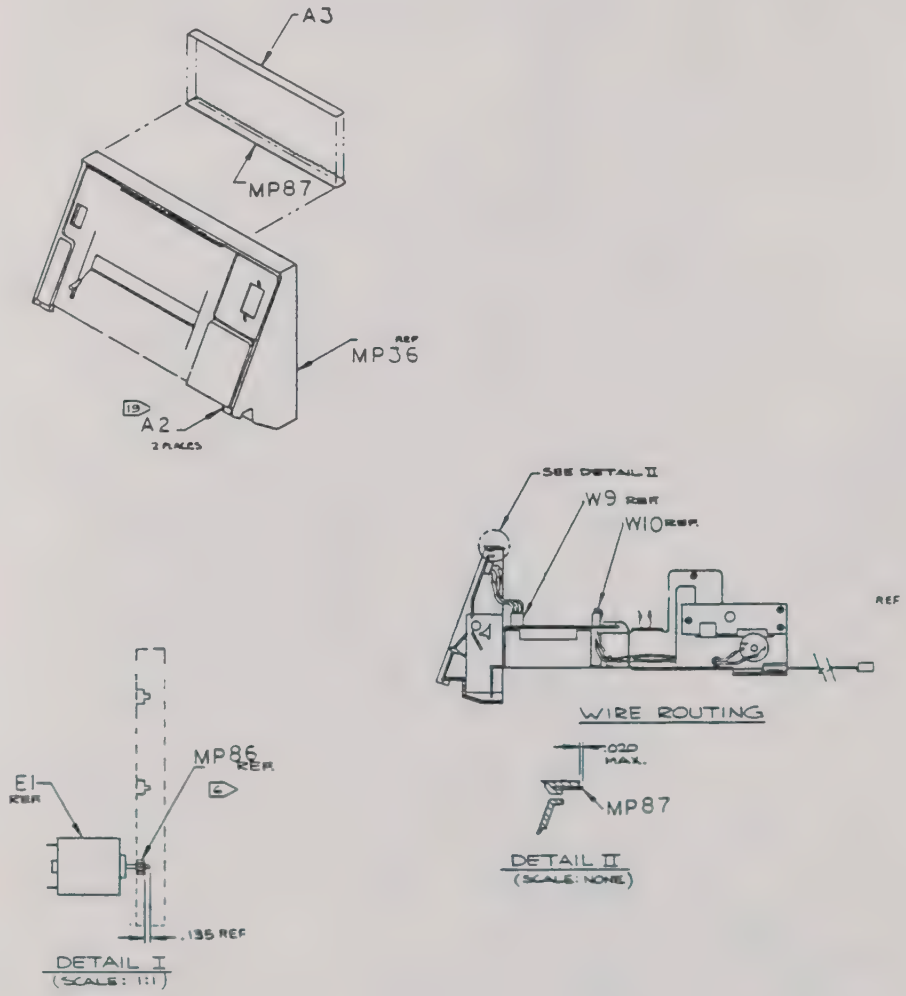


Figure 6-1. 2280B Final Assembly (cont.)



2280B-T&B (7 Of 9)

Figure 6-1. 2280B Final Assembly (cont.)



2280B-T&B (8 Of 9)

Figure 6-1. 2280B Final Assembly (cont.)

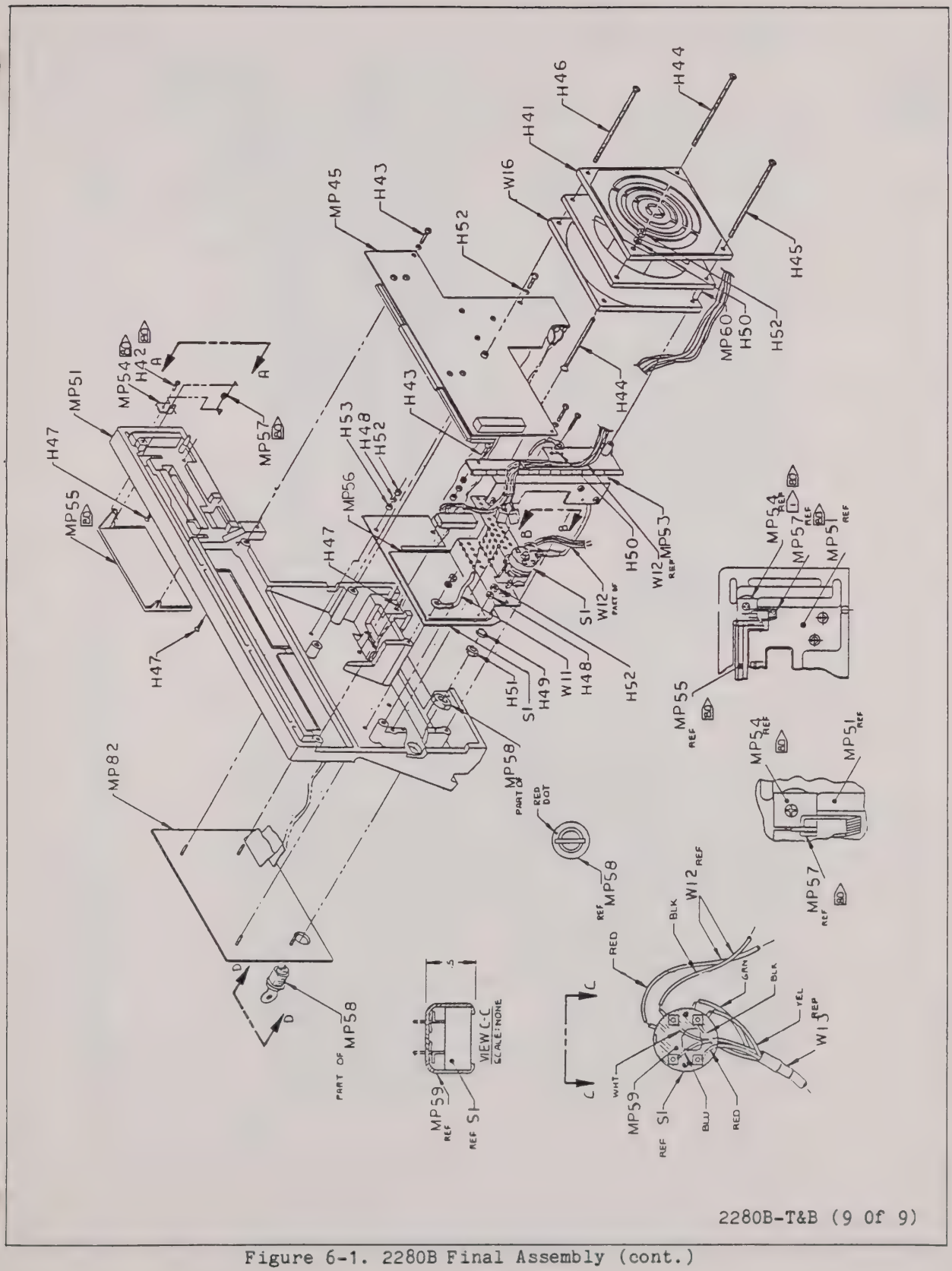


Figure 6-1. 2280B Final Assembly (cont.)

TABLE 6-2. A1 DISPLAY PCA
(SEE FIGURE 6-2.)

REFERENCE DESIGNATOR A->NUMERICS---)	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q
C 1		CAP,AL,47UF,+-20%,16V	643304	89536	643304	1	
C 2		CAP,POLYES,0.22UF,+-10%,100V	436113	73445	C280MAH1A220K	1	
C 3		CAP,TA,10UF,+-20%,35V	417683	56289	196D106X0035KA1	1	
C 4, 15		CAP,CER,0.001UF,+-20%,100V,X7R	402966	72982	8121-A100-W5R-102M	2	
C 5- 12, 26-		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	12	
C 29			519157				
C 13		CAP,CER,18PF,+-2%,100V,COG	512335	51406	RD870-100V	1	
C 14		CAP,CER,4.7PF,+-0.25PF,100V,COH	362772	89536	362772	1	
C 16		CAP,TA,10UF,+-20%,15V	193623	56289	196D106X0015A1	1	
C 17		CAP,CER,560PF,+-5%,50V,COG	528505	89536	528505	1	
CR 1, 2	*	DIODE,SI, 200 PIV, 1.0 AMP	586644	04713	1N4935	2	
CR 3	*	ZENER,UNCOMP, 10.0V, 5%, 25.0MA, 1.0W	340695	12969	UZ8710	1	1
CR 4	*	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	1	1
DS 1		DISPLAY,MODIFIED	580324	89536	580324	1	
F 1		FUSE,PICO,FAST,0.5A,125V	603274	71400	GFA	1	
H 1		SCREW,MACH,PHP,STL,4-40X1/4	129890	73734	19022	4	
H 2		WASHER,LOCK,SPLIT,S STEEL,#4	147603	89536	147603	4	
J 21, 29		SOCKET,SIP,0.100 CTR,16 PIN	493817	89536	493817	2	
LS 1		AF TRANSD,SPEAKER,0.63" DIA,50 MW	513093	89536	513093	1	1
MP 1		BRACKET,DISPLAY MOUNTING	581660	89536	581660	1	
MP 2		SPACER,SWAGED,RND,BRASS,0.150IDX0.187	357269	89536	357269	1	
MP 3		BAG,SHIELDING,TRANSPARENT,10"X12"	680959	89536	680959	1	
Q 1, 2, 3	*	TRANSISTOR,SI,VMOS,PWR,TO-237,VN10KM	640516	32293	VN10KM	3	1
R 1		RES,CF,30,+-5%,0.25W	442228	80031	CR251-4-5P30E	1	
R 2		RES,VAR,CERM,1K,+-10%,0.5W	285155	71450	360S102A	1	
R 3		RES,CF,2K,+-5%,0.25W	441469	80031	CR251-4-5P2K	1	
R 4		RES,CF,1,+-5%,0.25W	357665	80031	CR251-4-5P1E	1	
R 5, 6		RES,CF,5.1K,+-5%,0.25W	368712	80031	CR251-4-5P5K1	2	
R 7, 8, 10		RES,CF,100,+-5%,0.25W	348771	80031	CR251-4-5P100E	3	
R 9, 13		RES,CF,22K,+-5%,0.25W	348870	80031	CR251-4-5P22K	2	
R 14- 19		RES,CF,240,+-5%,0.25W	376624	80031	CR251-4-5P240E	6	
T 1		INVERTER TRANSFORMER	612267	89536	612267	1	
TP 1, 3, 10,		CONN,TAB,FASTON,PRESS-IN,0.110 WIDE	512889	02660	62395	12	
TP 12, 16- 18,			512889				
TP 60, 70, 75-			512889				
TP 77			512889				
U 1, 2, 3,	*	IC,BIPLR,8CHNL FLOURESCNT DISPLY DRVR	535799	56289	UDN6118A	10	1
U 6, 7, 15,	*		535799				
U 16, 17, 20,	*		535799				
U 21	*		535799				
U 4, 8- 10,	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,W/CLEAR	454892	01295	SN74LS273N	6	2
U 13, 14	*		454892				
U 5	*	IC,LSTTL,3-8 LINE DCDR W/ENABLE	407585	01295	SN74LS138N	1	2
U 11	*	IC,LSTTL,OCTL LINE DRVR W/3-STATE OUT	429035	01295	SN74LS244N	1	1
U 12, 18, 19,	*	IC,LSTTL,8BIT ADDRSABLE LATCH,W/CLR	419242	01295	SN74LS259N	6	1
U 27, 32, 37	*		419242				
U 22		IC,NMOS,8-BIT UCOMP W/PROG. EPROM	731778	89536	731778	1	
U 23	*	IC,LSTTL,QUAD 2 INPUT OR GATE	393108	01295	SN74LS32N	1	2
U 24	*	IC,CMOS,HEX BUFFER W/3-STATE OUTPUT	407759	12040	MM80C97N	1	1
U 25	*	IC,CMOS,HEX BUFFER	381830	02735	CD4050AE	1	1
U 26	*	IC,LSTTL,DUAL JK F/F,W/SEP CLKS&CLRS	393157	01295	SN74LS107N	1	1
U 28	*	IC,LSTTL,HEX INVERTER	393058	01295	SN74LS04N	1	1
U 29	*	IC,LSTTL,OCTL BUFFER W/3-ST&NOR ENABL	429902	12040	DM81LS95N	1	1
U 30	*	IC,TTL,OCTAL D F/F,+EDG TRG	473223	01295	SN74LS374N	1	1
U 31	*	IC,CMOS,TRIPLE 3 INPUT AND GATE	408807	02735	CD4073BE	1	1
U 33	*	IC,DUAL DIV BY 16 BINARY COUNTER	483578	01295	SN74LS393N	1	1
U 34	*	IC,TTL,MOS-LED 6SEGMENT DRIVER	429506	12040	DS75492N	1	1
U 35	*	IC,CMOS,4-1 LINE LTCH 4-16 LINE DCDR	355156	04713	MC14515BCP	1	1
U 36	*	IC,NMOS,INPUT/OUTPUT EXPANDER	507293	34649	P8243	1	1
XDS 1		SOCKET,SIP,0.100 CTR,20 PIN	485045	89536	485045	4	5
XU 22		SOCKET,DIP,0.100 CTR,40 PIN	429282	09922	DILB40P-108	1	
Y 1	*	CRYSTAL,11MHZ,+-0.01%,HC-18/U	586628	89536	586628	1	
Z 1, 3, 4		RES,NET,SIP,8 PIN,4 RES,10K,+-2%	513309	89536	513309	3	
Z 2, 5		RES,NET,SIP,8 PIN,7 RES,22K,+-2%	500041	89536	500041	2	
Z 6, 7		RES,NET,SIP,10 PIN,5 RES,1K,+-2%	655209	89536	655209	2	

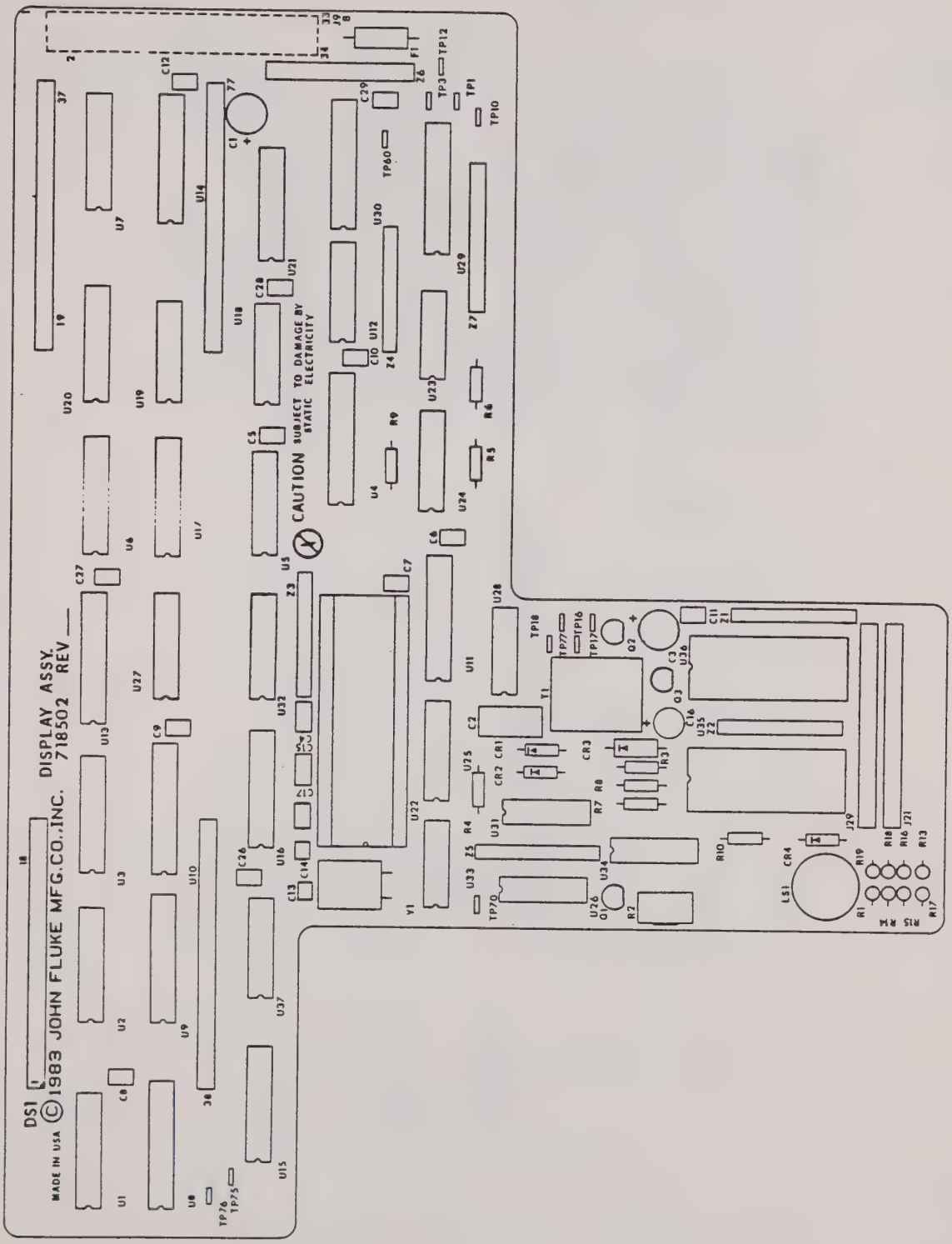
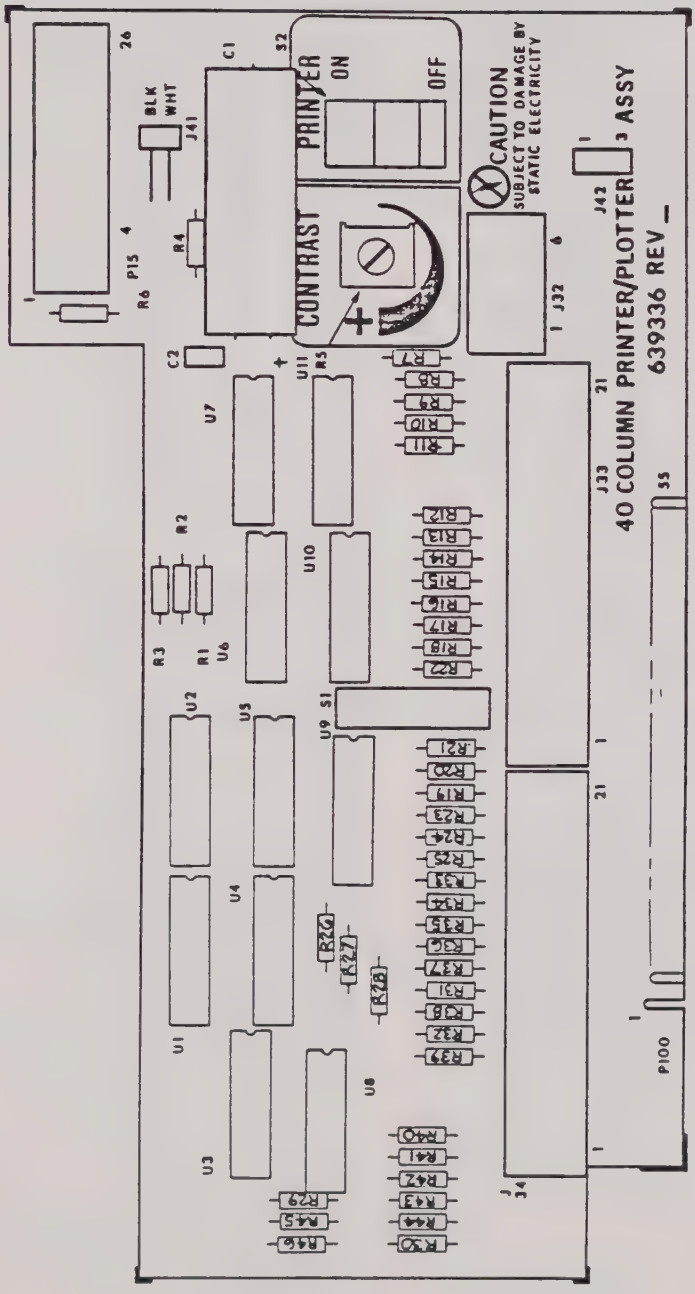


Figure 6-2. A1 Display PCA

TABLE 6-3. A2 PRINTER DRIVER PCA
(SEE FIGURE 6-3.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOT -E
C 1		CAP,AL,330UF,+100-10%,25V	614404	89536	614404	1		
C 2		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	1		
J 32		CONN,FLAT CABLE,REC,90,6 POS	603647	89536	603647	1		
J 33, 34		CONN,FLAT CABLE,REC,90,21 POS	603654	89536	603654	2		
J 41, 42		CONN,POST,PWB,.025SQ,NON-INSUL,TIN	484428	00779	9-87022-1	5		
MP 1		SPACER,SWAGED,RND,BRASS,6-32X0.500	284380	89536	284380	4	1	
MP 2		BAG,SHIELDING,TRANSPARENT,5"X8"	680892	89536	680892	1		
P 15		CONN,FLAT CABLE,PWB PLUG,26 PIN	530147	89536	530147	1	2	
R 1		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	1		
R 2, 3, 6		RES,CF,2K,+-5%,0.25W	441469	80031	CR251-4-5P2K	3		
R 4		RES,CF,22K,+-5%,0.25W	348870	80031	CR251-4-5P22K	1		
R 5		RES,VAR,CERM,100K,+-10%,0.5W	369520	11236	360T-104A	1		
R 7- 46		RES,CF,68,+-5%,0.25W	414532	80031	CR251-4-5P68E	40		
S 1		SWITCH,PUSHBUTTON,SPDT MOMENTARY	631143	89536	631143	1		
S 2		SWITCH,ROCKER,DPDT	641407	89536	641407	1	1	
U 1, 4, 8-	*	IC,ARRAY,7 TRANS,NPN,DARLINGTON PAIRS	454116	01295	ULN2003	6	1	
U 11	*		454116					
U 2, 3, 5-	*	IC,CMOS,8BIT SHFT RGS W/3-ST&I/O LTCH	524520	04713	MC14094BCP	5		
U 7	*		524520					
W 1		CABLE ASSY,PRINTER	605444	89536	605444	1		



2280A-1615

Figure 6-3. A2 Printer Driver PCA

TABLE 6-4. A3 PRINTER INTERFACE PCA
(SEE FIGURE 6-4.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOT -E
C 1- 6, 11,		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	11		
C 13- 16			519157					
C 7		CAP,POLYES,0.01UF,+-10%,250V	325548	73445	C280MAE/A10K	1		
C 8		CAP,CER,18PF,+-2%,100V,COG	512335	51406	RD870-100V	1		
C 9		CAP,CER,4.7PF,+-0.25PF,100V,COH	362772	89536	362772	1		
C 10		CAP,AL,47UF,+-20%,16V	643304	89536	643304	1		
C 12		CAP,CER,5600PF,+-5%,50V,COG	528596	89536	528596	1		
C 17- 21		CAP,CER,0.001UF,+-20%,100V,X7R	402966	72982	8121-A100-W5R-102M	5		
CR 1	*	ZENER,UNCOMP, 5.6V, 5%, 20.0MA, 0.4W	277236	07910	1N752A	1		
CR 2	*	DIODE,SI, 100 PIV, 1.0 AMP	343491	01295	1N4002	1	1	
E 1		COPPER TEFLON INSUL .300 IN LENGTH	528257	89536	528257	1		
H 1		NUT,HEX,MINI,S.STL,6-32	110569	89536	110569	2		
H 2		SCREW,MACH,PHP,STL,6-32X3/8	152165	89536	152165	2		
H 3		WASHER,FLAT,BRASS,#6,0.012 THK	111054	89536	111054	2		
H 4		WASHER,LOCK,SPLIT,STEEL,#6	110692	89536	110692	2		
J 15		HEADER,DUAL ROW,.100 CTRS,26 POS	603662	89536	603662	1	1	
MP 1		CABLE TIE,4"L,0.100"W,0.75 DIA	172080	89536	172080	2		
MP 2		PUSHBUTTON, PG SMALL RECT. C.L. REPL.	412163	89536	412163	1		
MP 3		BAG,SHIELDING,TRANSPARENT,12"X16"	680983	89536	680983	1		
MP 4		HEATSINK, INNER, U1	473660	13103	6070B	1	1	
Q 1	*	TRANSISTOR,SI,BV= 60V, 65W,TO-220	386128	01295	T1P120	1	1	
Q 2	*	TRANSISTOR,SI,BV= 45V, 30W,TO-220	325761	09214	D44C5	1	1	
Q 3	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	1	1	
R 1		RES,MF,150K,+-1%,0.125W,100PPM	241083	91637	CMF551503F	1		
R 2, 14		RES,CC,200,+-5%,1W	190603	89536	190603	2		
R 3		RES,CC,360,+-5%,1W	266361	89536	266361	1		
R 4		RES,CC,10,+-5%,0.25W	147868	01121	CB1005	1		
R 5		RES,CF,6.8K,+-5%,0.25W	368761	80031	CR251-4-5P6K8	1		
R 6- 8, 15,		RES,CF,22K,+-5%,0.25W	348870	80031	CR251-4-5P22K	7		
R 17, 20, 21			348870					
R 9, 18		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	2		
R 10		RES,MF,1.4K,+-1%,0.125W,100PPM	344333	91637	CMF551401F	1		
R 11		RES,VAR,CERM,1K,+-10%,0.5W	285155	71450	360S102A	1		
R 12		RES,MF,1.1K,+-1%,0.125W,100PPM	241497	91637	CMF551101F	1		
R 13		RES,VAR,CERM,150K,+-10%,0.5W	414102	11236	360T151A	1		
R 16		RES,CF,1,+-5%,0.25W	357665	80031	CR251-4-5P1E	1		
R 19		RES,MF,45.3K,+-1%,0.125W,100PPM	234971	91637	CMF554532F	1		
S 1		SWITCH,PUSHBUTTON,DPDT PUSH-PUSH	520437	89536	520437	1		
TP 1, 3, 10,		CONN,TAB,FASTON,PRESS-IN,0.110 WIDE	512889	02660	62395	9		
TP 12, 71- 75			512889					
U 1	*	IC,CMOS,HEX BUFFER	381830	02735	CD4050AE	1	1	
U 2	*	IC,CMOS,QUAD 2 INPUT NOR GATE	355172	02735	CD4001AE	1	1	
U 3	*	IC,CMOS,HEX INVERTER	404681	02735	CD4069BE	1	1	
U 4	*	IC,CMOS,DUAL D F/F,+EDG TRG W/SET&RST	536433	04713	MC4013BCP	1	1	
U 5, 12	*	IC,CMOS,HEX BUFFER W/3-STATE OUTPUT	407759	12040	MM80C97N	2	1	
U 6	*	IC,NMOS,8-BIT MICROPROCESSOR	504563	89536	504563	1		
U 7	*	IC,LSTTL,OCTAL D TRANSPARENT LATCHES	504514	01295	SN74LS373N	1	1	
U 8	*	IC, 2K X 8 EPROM (PROGRAMMED)	655589	89536	655589	1		
U 9	*	IC,LSTTL,8BIT ADDRSABLE LATCH,W/CLR	419242	01295	SN74LS259N	1	1	
U 10	*	IC,CMOS,DUAL JK F/F,+EDG TRIG	355230	02735	CD4027AE	1	1	
U 11	*	IC,CMOS,DUAL MONOSTABLE MULTIBRATOR	454017	04713	MC14538BCP	1	1	
XU 6		SOCKET,DIP,0.100 CTR,40 PIN	429282	09922	DILB40P-108	1		
XU 8		SOCKET,DIP,0.100 CTR,24 PIN	376236	91506	324-AG39D	1		
Y 1	*	CRYSTAL,6MHZ,+-0.01%,HC-18/U	461665	89536	461665	1	1	
Z 1, 2		RES,NET,SIP,8 PIN,7 RES,4.7K,+-2%	412916	80031	95081002CL	2		
Z 3, 4, 5		RES,NET,DIP,14 PIN,7 RES,10K,+-5%	364000	01121	314	3		

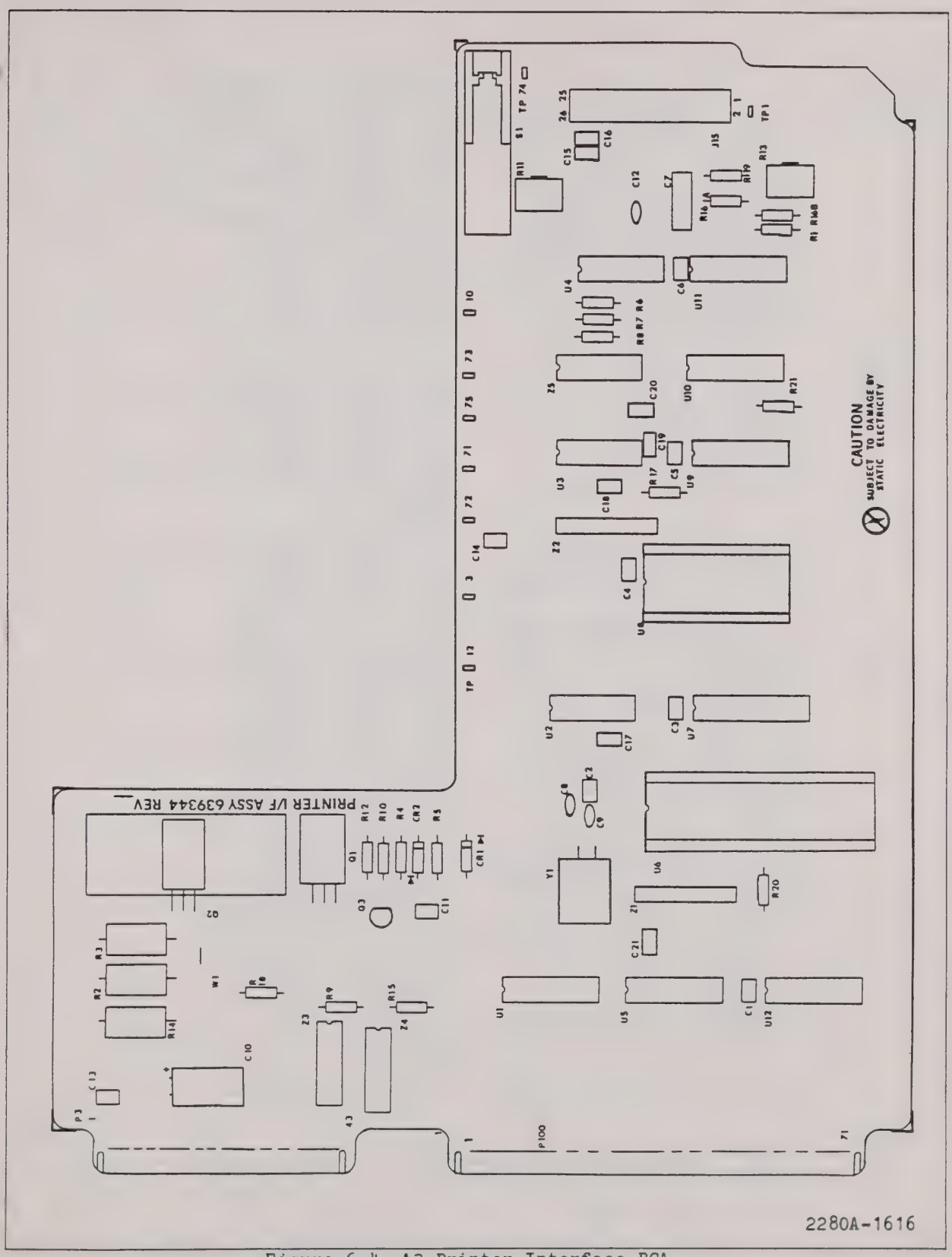


Figure 6-4. A3 Printer Interface PCA

TABLE 6-5. A4 CONTROLLER PCA
(SEE FIGURE 6-5.)

REFERENCE DESIGNATOR A->NUMERICS---)	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOT -E
C 1- 26, 29		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	27		
C 23		CAP,AL,47UF,+-20%,16V	643304	89536	643304	1		
C 27		CAP,MICA,39PF,+-5%,500V	148544	72136	DM15E390J	1		
C 28		CAP,MICA,4PF,+-0.5PF,500V	190397	72136	DM15C040E	1		
C 30		CAP,CER,220PF,+-2%,100V,COG	512111	51406	RPE121	1		
C 31, 32		CAP,CER,560PF,+-5%,50V,COG	528505	89536	528505	2		
C 34		CAP,CER,0.01UF,+-20%,50V,Z5U	614214	72982	8121-050-651-10NFM	1		
CR 1	*	DIODE,GER,BV=100.0V,IO= 80MA,80 MW	149187	93332	1N270	1		
CR 2, 3	*	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	2	1	
DS 1	*	DIODE,LED,RED 7 SEGMENT,ALPHA NUMERIC	472944	28480	QDSP3016	1	1	
MP 1		BAG,SHIELDING,TRANSPARENT,12"X16"	680983	89536	680983	1		
MP 2		EJECTOR,PCB .062,	706879	89536	706879	1		
MP 3		COMPONENT HOLDER	422865	98159	2829-75-2	1		
Q 1	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	1	1	
R 1, 9, 11,		RES,CF,22K,+-5%,0.25W	348870	80031	CR251-4-5P22K	5		
R 12, 13			348870					
R 2, 7		RES,CF,1,+-5%,0.25W	357665	80031	CR251-4-5P1E	2		
R 3, 6		RES,CF,100K,+-5%,0.25W	348920	80031	CR251-4-5P100K	2		
R 4		RES,CF,1K,+-5%,0.25W	343426	80031	CR251-4-5P1K	1		
R 5		RES,CC,22M,+-5%,0.25W	221986	01121	CB2265	1		
R 8		RES,CF,3.3K,+-5%,0.25W	348813	80031	CR251-4-5P3K3	1		
R 10		RES,CF,20,+-5%,0.25W	442202	80031	CR251-4-5P20E	1		
R 14, 15		RES,CF,5.1K,+-5%,0.25W	368712	80031	CR251-4-5P5K1	2		
R 16		RES,CF,220,+-5%,0.25W	342626	80031	CR251-4-5P220E	1		
TP 1, 10, 11,		TURRET,MINI HOLLOW LUG #2010B-1	179283	88245	2010B-5	11	1	
TP 50, 51, 70,			179283					
TP 71, 72, 73,			179283					
TP 74, 75			179283					
U 1	*	IC,NMOS, PARALLEL I/O CONTROLLER	536920	89536	536920	1		
U 2	*	IC,CMOS,8 INPUT NAND GATE	504860	04713	MC14068BCP	1	1	
U 3, 8, 9	*	IC,CMOS,HEX BUFFER W/3-STATE OUTPUT	407759	12040	MM80C97N	3	1	
U 4	*	IC,CMOS,UNIV.ASYNC RECVR/TRANSMITTER	453464	89536	453464	1		
U 5, 14, 23,	*	IC,LSTTL,OCTL BUFFER W/3-ST&NOR ENABL	429902	12040	DM81LS95N	4	1	
U 24	*		429902					
U 6	*	IC,LSTTL,8-3 LINE PRIORITY ENCDR,3-ST	483669	01295	SN74LS348N	1	1	
U 7	*	IC,LSTTL,HEX D F/F,+EDG TRG,W/CLEAR	393207	01295	SN74LS174N	1	1	
U 10, 17, 18	*	IC,LSTTL,DUAL D F/F,+EDG TRG,W/CLR	393124	01295	SN74LS74N	3	1	
U 11, 40	*	IC,CMOS,HEX D F/F,+EDG TRG,W/RESET	404509	12040	MM74C174N	2	1	
U 12	*	IC,CMOS,QUAD 2 INPUT NAND GATE	453241	02735	CD4011BE	1	1	
U 13	*	IC,CMOS,DUAL D F/F,+EDG TRG W/SET&RST	536433	04713	MC4013BCP	1	1	
U 15	*	IC,FTTL,HEX INVERTER	634444	07235	74F04PC	1	1	
U 16	*	IC,LSTTL,DIV BY 2,DIV BY 5 COUNTER	402545	01295	SN74LS90N	1	1	
U 19	*	IC,LSTTL,DUAL 4 INPUT NAND GATE	393280	01295	SN74LS20N	1	1	
U 20	*	IC,TTL,QUAD 2 INPUT AND GATE	393066	01295	SN74LS08N	1	1	
U 21	*	IC,LSTTL,TRIPLE 3 INPUT AND GATE	393082	04713	SN74LS11N	1	1	
U 22	*	IC,CMOS,DUAL 1 OF 4 DECODER	584987	04713	MC14555BP	1	1	
U 25	*	IC,NMOS,8 BIT MICROCOMPUTER	478073	50088	MK3880-4CPU	1	1	
U 26		IC, 8K X 8 EPROM (PROGRAMMED)	752964	89536	752964	1		1
U 27, 28	*	IC, 2K X 8 STAT RAM	584144	33297	uPD4016C-2	2	1	
U 29, 30, 38	*	IC,LSTTL,3-8 LINE DCDR W/ENABLE	407585	01295	SN74LS138N	3	1	
U 31	*	IC,CMOS,14STAGE RIPPLE CARRY BIN CNTR	507640	89536	507640	1	1	
U 32	*	IC,LSTTL,OCTL BUS TRNSCVR W/3-ST OUT	477406	01295	SN74LS245N	1	1	
U 33	*	IC,LSTTL,8BIT ADDRSABLE LATCH,W/CLR	419242	01295	SN74LS259N	1	1	
U 34, 37	*	IC,LSTTL,QUAD 2 INPUT OR GATE	393108	01295	SN74LS32N	2	1	
U 35	*	IC,LSTTL,HEX INVERTER W/SCHMT TRIG	483180	01295	SN74LS14N	1	1	
U 36	*	IC,LSTTL,TRIPLE 3 INPUT NOR GATE	393090	01295	SN74LS27N	1	1	
U 41	*	IC,CMOS,SERIAL,I/O CALENDER & CLOCK	586412	89536	586412	1		
XU 1, 4, 25		SOCKET,DIP,0.100 CTR,40 PIN	429282	09922	DILB40P-108	3		
XU 26		SOCKET,DIP,0.100 CTR,28 PIN	448217	91506	328-AG39D	1		
XU 27, 28, 39		SOCKET,DIP,0.100 CTR,24 PIN	376236	91506	324-AG39D	3		
XU 41		SOCKET,DIP,0.100 CTR,14 PIN	276527	09922	DILB8P-108	1		
Y 1		OSCILLATOR,4MHZ/8MHZ,TTL CLOCK	642710	89536	642710	1	1	
Y 2	*	CRYSTAL,32.768KHZ,+-0.003%,DIP	501817	89536	501817	1		
Z 1, 2, 4,		RES,NET,SIP,10 PIN,9 RES,22K,+-2%	574442	89536	574442	7		
Z 5, 6, 7,			574442					
Z 8			574442					
Z 3		RES,NET,SIP,10 PIN,9 RES,4.7K,+-2%	484063	80031	9508100ZCL	1		
Z 9		RES,NET,DIP,16 PIN,8 RES,240,+-5%	424457	01121	314	1		

NOTE 1 = PART NUMBER IS FOR MAINFRAME EPROM SET. EACH SET INCLUDES 16 PROGRAMMED EPROMS. ONE EPROM ON THE CONTROLLER PCA AND 15 ON THE MEMORY PCA.

ORDER P/N 655530 FOR 2280A
ORDER P/N 753038 FOR 2285B

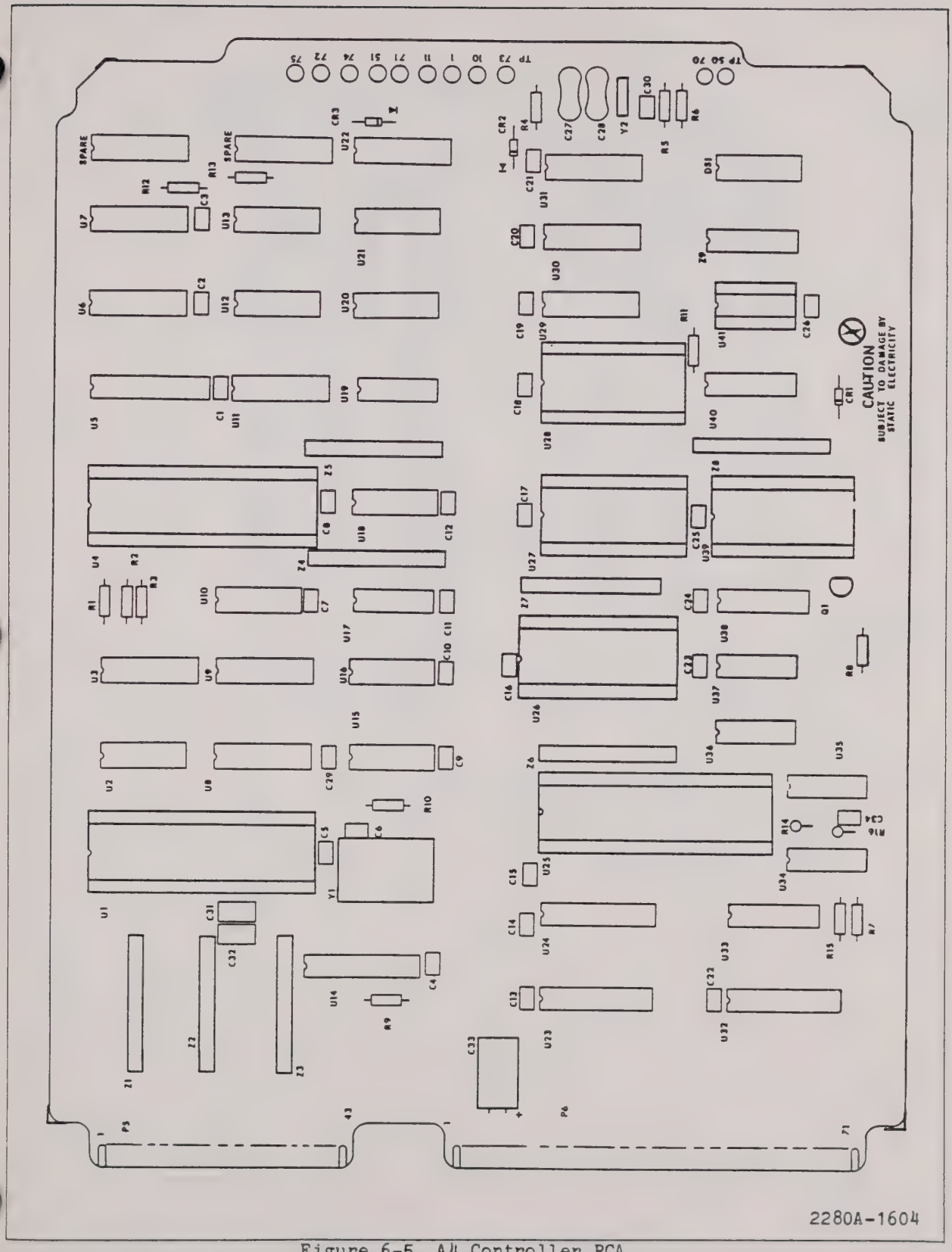


Figure 6-5. A4 Controller PCA

TABLE 6-6. A5 MEMORY PCA
(SEE FIGURE 6-6.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	RS -Q	NOT -E
C 1- 17, 20-		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	36		
C 38			519157					
C 18		CAP,AL,47UF,+-20%,16V	643304	89536	643304	1		
CR 1- 5	*	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	5		
MP 1		EJECTOR,PCB .062,	706879	89536	706879	1	1	
MP 2		BAG,SHIELDING,TRANSPARENT,12"X16"	680983	89536	680983	1		
Q 1- 15	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	159855	07910	CS23030	15	1	
Q 16	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	352369	12040	2N4403	1	1	
R 1		RES,CF,68,+-5%,0.25W	414532	80031	CR251-4-5P68E	1		
R 2, 5, 6,		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	4		
R 7			348839					
R 3		RES,CF,270,+-5%,0.25W	348789	80031	CR251-4-5P270E	1		
R 4		RES,CF,470,+-5%,0.25W	343434	80031	CR251-4-5P470E	1		
R 8, 9		RES,CF,22K,+-5%,0.25W	348870	80031	CR251-4-5P22K	2		
TP 1, 10, 11,		TURRET,MINI HOLLOW LUG #2010B-1	179283	88245	2010B-5	8		
TP 80- 84			179283					
U 1, 12, 19	*	IC,LSTTL,HEX BUFFER W/NOR ENABLE	483800	01295	SN74LS367N	3	3	
U 2- 11, 13-	*	IC,8K X 8 EPROM(PROGRAMMED FOR 2280B)	752964	89536	752964	1		1
U 17	*		752964					1
U 18	*	IC,LSTTL,OCTAL BUFFER/LINE DRIVER	634105	04713	SN74LS541N	1	1	
U 20	*	IC,LSTTL,QUAD 2 INPUT OR GATE	393108	01295	SN74LS32N	1	1	
U 21, 22, 29,	*	IC,LSTTL,3-8 LINE DCDR W/ENABLE	407585	01295	SN74LS138N	5	1	
U 42, 49	*		407585					
U 25, 26, 30,	*	IC,2K X 8 STAT RAM	585786	89536	585786	4		
U 31	*		585786					
U 27, 33	*	IC,LSTTL,OCTL BUS TRNSCVR W/3-ST OUT	477406	01295	SN74LS245N	2	1	
U 28, 34, 44	*	IC,LSTTL,QUAD 2 INPUT NAND GATE	393033	01295	SN74LS00N	3	1	
U 35	*	IC,LSTTL,HEX D F/F,+EDG TRG,W/CLEAR	393207	01295	SN74LS174N	1	1	
U 36, 41, 43,	*	IC,LSTTL,QUAD 2-1 LINE MUX W/STROBE	407833	01295	SN74LS157N	4	1	
U 48	*		407833					
U 37	*	IC,LSTTL,QUAD BUS BFR W/3-STATE OUT	472746	01295	SN74LS125N	1	1	
XU 2- 11, 13-		SOCKET,DIP,0.100 CTR,28 PIN	448217	91506	328-AG39D	15		
XU 17			448217					
XU 25, 26, 30-		SOCKET,DIP,0.100 CTR,24 PIN	376236	91506	324-AG39D	14		
XU 32, 38- 40,			376236					
XU 45- 47, 50-			376236					
XU 52			376236					
Z 1- 4		RES,NET,SIP,8 PIN,7 RES,560,+-2%	484451	89536	484451	4		
Z 5- 7, 9		RES,NET,SIP,10 PIN,9 RES,22K,+-2%	574442	89536	574442	4		
Z 8		RES,NET,SIP,6 PIN,5 RES,22K,+-2%	520122	89536	520122	1		

NOTE 1 = PART NUMBER IS FOR MAINFRAME EPROM SET. EACH SET INCLUDES 16 PROGRAMMED EPROMS. ONE EPROM ON THE CONTROLLER PCA AND 15 ON THE MEMORY PCA.

ORDER P/N 655530 FOR 2280A
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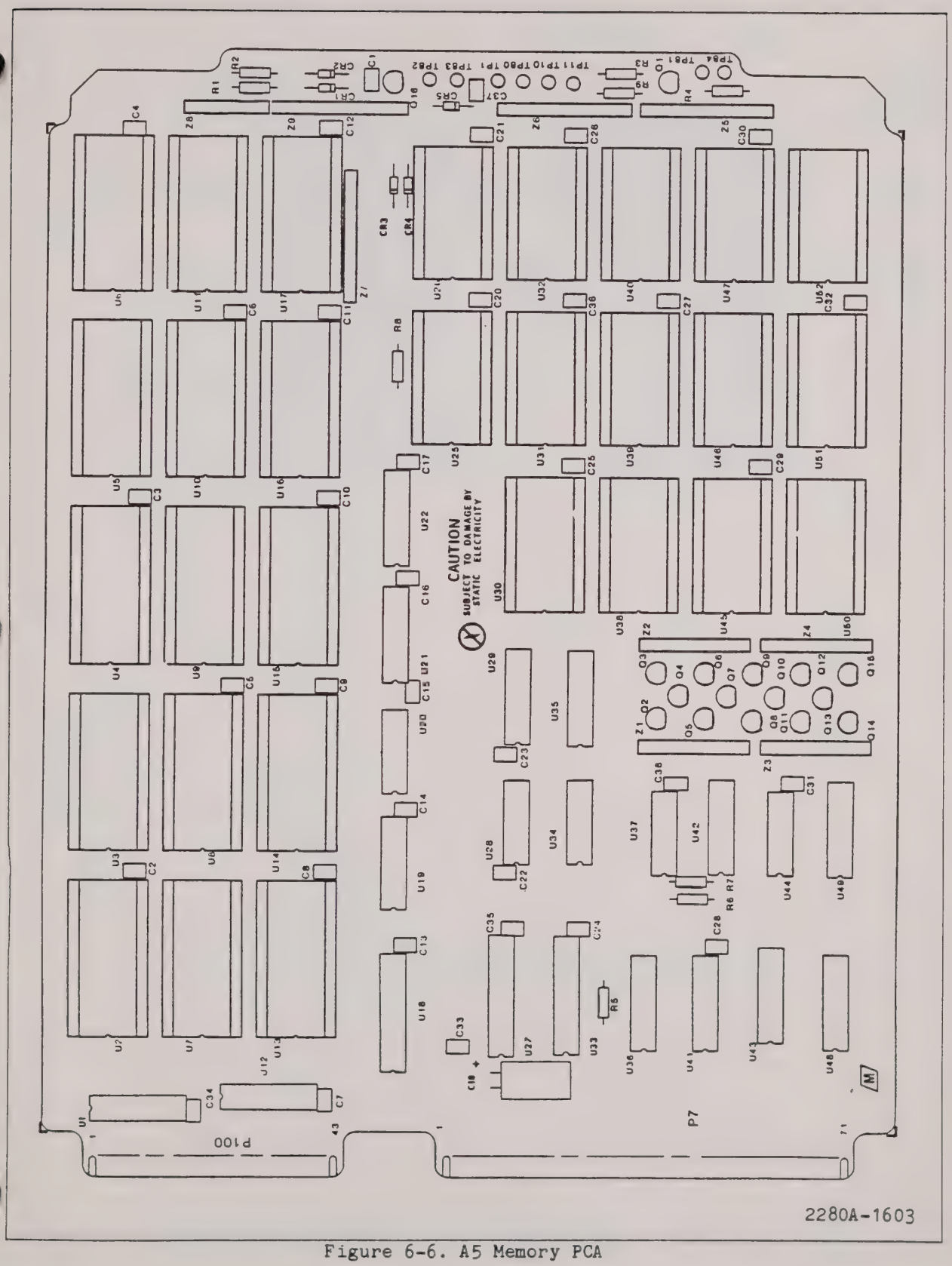


Figure 6-6. A5 Memory PCA

TABLE 6-7. A6 TRANSFORMER PCA
(SEE FIGURE 6-7.)

REFERENCE DESIGNATOR A->NUMERICS---)	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOT -E
C 1- 3		CAP,AL,4500UF,+100-10%,25V	493684	89536	493684	3		
C 4- 7	*	DIODE,SI, 100 PIV, 1.0 AMP	343491	01295	1N4002	4		
C 4, 5		CAP,CER,5000PF,+-20%,250V,X7R	485839	89536	485839	2		
C 6		CAP,POLYES,0.1UF,+-20%,250V AC	542233	55112	158.00-0.10uF-250V	1		
C 7		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	1		
CR 1- 3	*	DIODE,SI, 200 PIV, 12.0 AMP	188854	04713	MR1122	3	1	
H 1		NUT,MACH,HEX,STL,10-32	110536	89536	110536	3		
H 2		WASHER,LOCK,SPLIT,STEEL,#10	111484	89536	111484	3		
H 3		WASHER,FLAT,STEEL,#10,0.031 THK	110262	89536	110262	3		
J 13		HEADER,SIP,.156,FRICT. LOK,10,1.536	446724	27264	09-65-1101	1	1	
J 16		HEADER,SIP,.156,FRICT. LOK,4,.600	385443	89536	385443	1		
J 20		HEADER,SIP,.156,FRICT. LOK,3,.444	380022	89536	380022	1		
J 31		CONN,PWB,MATE-N-LOK,4 PIN	512269	00779	350211-1	1		
J 35		HEADER,SIP,.156,FRICT. LOK,2,.288	641647	89536	641647	1		
K 1		RELAY,ARMATURE,1 FORM C,12VDC	512194	28478	20693-83	1	1	
MP 1		HEATSINK,DIODE	583849	89536	583849	1		
MP 2		HEATSINK	428805	13103	6046P8	1	1	
Q 1	*	TRANSISTOR,SI,BV= 45V, 30W,TO-220	325761	09214	D44C5	1	1	
R 1		RES,CC,820,+-5%,1W	266379	01121	GB8215	1		
R 2		RES,CC,2K,+-5%,0.5W	169854	01121	EB2025	1		
R 4, 5		RES,CC,10,+-10%,0.5W	108092	01121	EB1001	2		
R 6		RES,CC,100,+-5%,0.5W	188508	01121	EB1015	1		
R 7		RES,CC,1K,+-5%,0.5W	108597	01121	EB1025	1		
R 8		RES,CF,5.1,+-5%,0.25W	441287	80031	CR251-4-5P5R1	1		
S 1, 2		SWITCH,SLIDE,DPDT,POWER	234278	89536	234278	2		

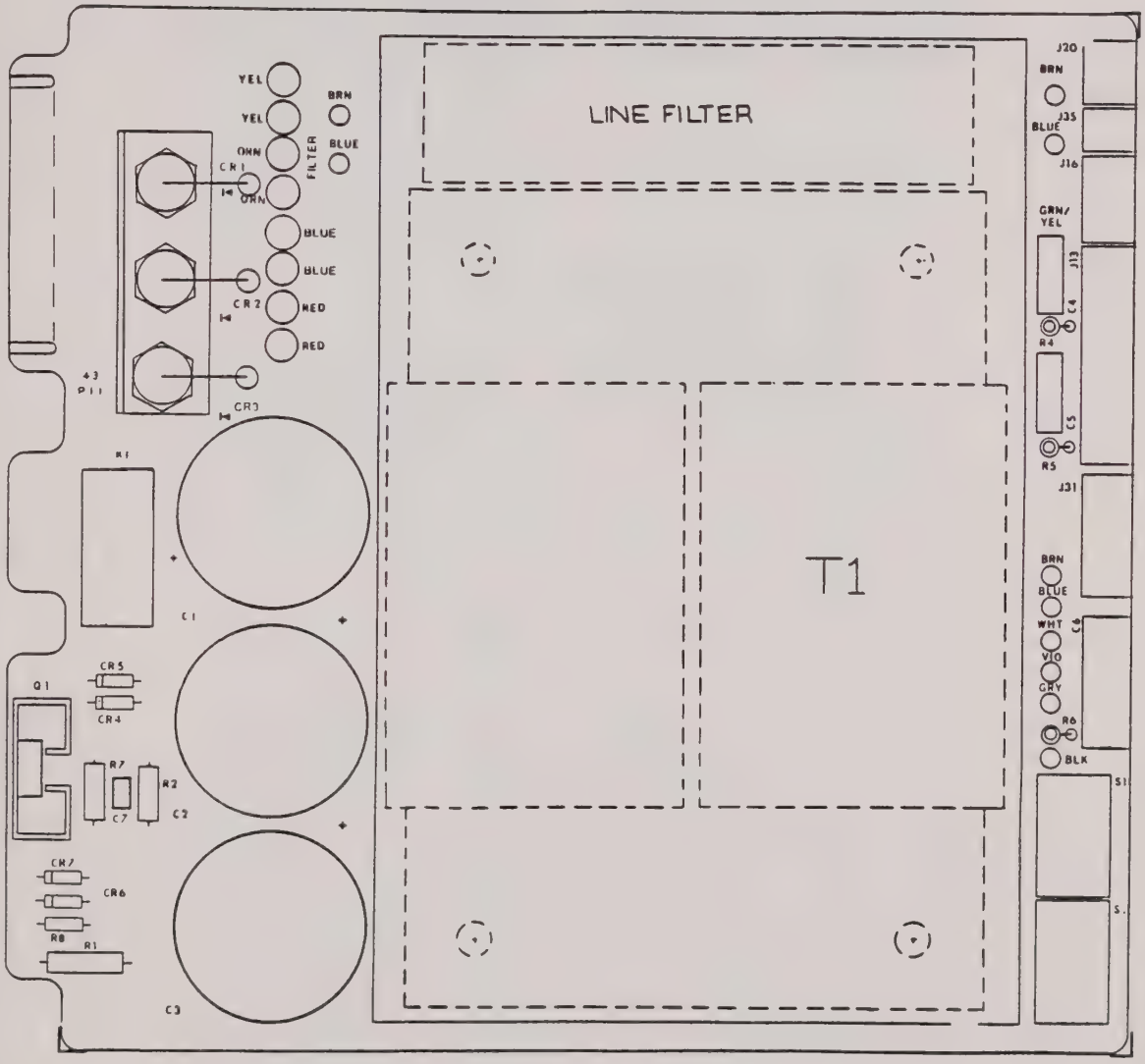
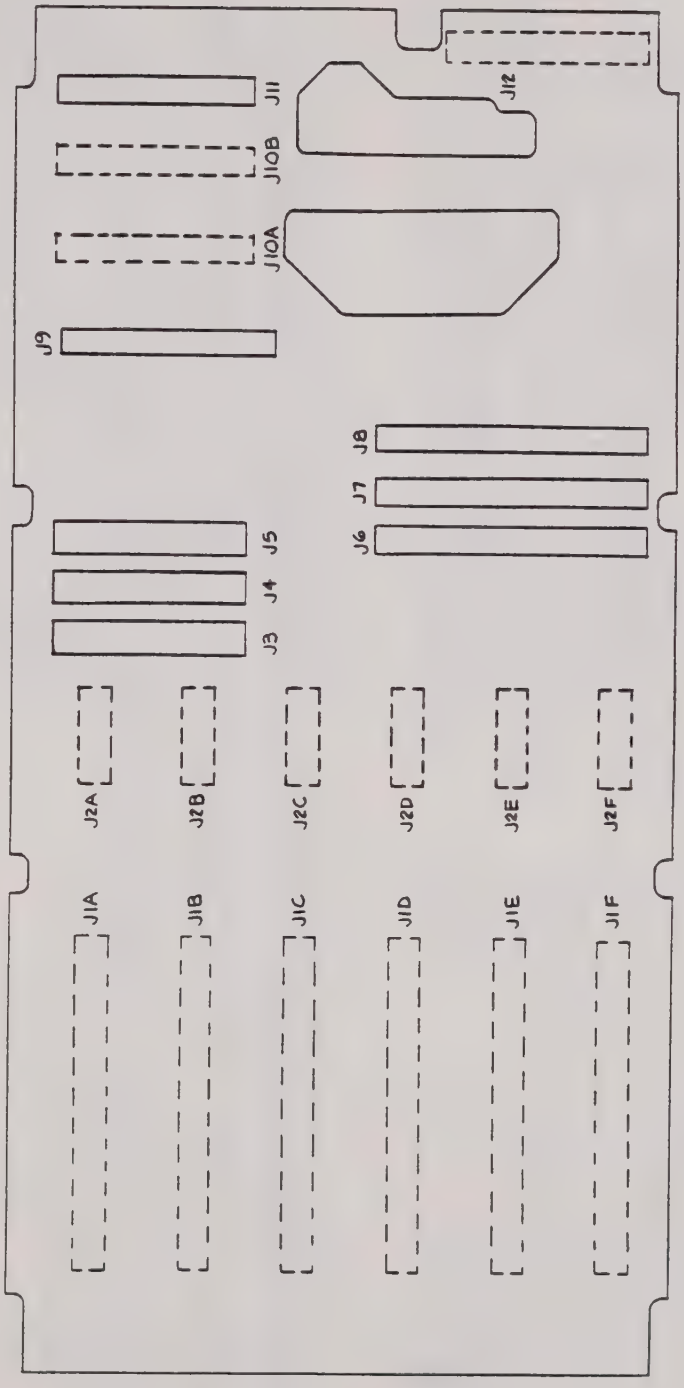


Figure 6-7. A6 Transformer PCA

TABLE 6-8. A7 MOTHERBOARD PCA
(SEE FIGURE 6-8.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
H 1		SCREW,MACH,FIHS,NYL,6-32X5/8	330019	95987	N-632-5/8	4		
H 2		NUT,NYLON 6-32 HEX, BLACK NYLON	111013	89536	111013	4		
J 3- 5, 11		CONN,PWB EDGE,REC,0.100 CTR,44 POS	520148	00779	1-5308843-5	4		
J 6- 8		CONN,PWB EDGE,REC,0.100 CTR,72 POS	520155	00779	1-530843-9	3		
J 9		CONN,FLAT CABLE,HDR,.100X.100,34 POS	643239	89536	643239	1		
MP 1		SPACER,RND,ALUM,0.156IDX0.250	153155	89536	153155	4		



2280A-1601

Figure 6-8. A7 Motherboard PCA

TABLE 6-9. A8 POWER SUPPLY PCA
(SEE FIGURE 6-9.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOT -E
BT 1		BATTERY,NI-CAD,3.6V,0.49AH	615476	89536	615476	1		
C 1, 3, 4,		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	11		
C 13, 14, 16,			519157					
C 17, 22, 26,			519157					
C 34, 35			519157					
C 2, 9		CAP,AL,1000UF,+100-10%,25V	601971	89536	601971	2		
C 5, 10, 23,		CAP,TA,1UF,+-10%,35V	161919	56289	196D010X0035G	4		
C 32			161919					
C 6, 7, 27,		CAP,POLYES,0.1UF,+-10%,100V	393439	80031	719A1	4		
C 33			393439					
C 8, 24, 29		CAP,POLYES,0.01UF,+-10%,250V	325548	73445	C280MAE/A10K	3		
C 11		CAP,AL,270UF,+100-10%,20V	602656	89536	602656	1		
C 12		CAP,AL,470UF,+100-10%,12V	602649	89536	602649	1		
C 15, 20		CAP,CER,4700PF,+-20%,100V,X7R	362871	72982	8121-A100-W5R-472M	2		
C 19		CAP,CER,470PF,+-20%,100V,X7R	358275	72982	8111-A100-W5R-471M	1		
C 21, 28		CAP,TA,4.7UF,+-20%,25V	161943	56289	196D475X0025KA1	2		
C 25		CAP,POLYES,0.22UF,+-10%,100V	436113	73445	C280MAH1A220K	1		
C 31		CAP,TA,0.33UF,+-20%,35V	408690	56289	196D334X0035HA1	1		
CR 1- 8, 19	*	DIODE,SI, 50 PIV, 1.0 AMP	379412	04713	1N4933	9		
CR 9, 12- 15,	*	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	9	2	
CR 17, 25, 27,	*		203323					
CR 28	*		203323					
CR 10, 11	*	DIODE,SI, 35 PIV, 10.0 AMP	643023	89536	643023	2	2	
CR 16, 18	*	DIODE,GER,BV125.0V,IO= 75MA,80 MW	150342	89536	150342	2	1	
CR 22, 26	*	DIODE,SI, 20 PIV, 1.0 AMP	507731	83003	VSK120	2	1	
F 1		FUSE,1/4 X 1-1/4,FAST,1.5A,250V	109330	71400	AGC1-1/2	1		
H 1		WASHER,LOCK,INTRNL,STEEL,#4	110403	89536	110403	4		
H 2		SCREW,MACH,PHP,STL,6-32X3/8	152165	89536	152165	2		
H 3		NUT,HEX,MINI,S.STL,6-32	110569	89536	110569	2		
H 4		SCREW,MACH,PHP,STL,4-40X3/8	152124	73734	19024	2		
H 5		NUT,MACH,HEX,STL,4-40	110635	89536	110635	6		
H 6		STUD,THREADED,PENN KFH,4-40,.500	494682	89536	494682	4		
H 7		WASHER,FLAT,STEEL,#5,0.032 THK	195909	89536	195909	4		
H 8		WASHER,LOCK,INTRNL,STEEL,#4	110403	89536	110403	6		
H 9		WASHER,LOCK,SPLIT,STEEL,#6	110692	89536	110692	2		
J 23		CONN,D-SUB,PWB,R/A MOUNT,15 SOCKET	707034	89536	707034	1		
J 25		CONN,D-SUB,PWB,R/A MOUNT,9 SOCKET	714113	89536	714113	1		
K 1		RELAY,REED,1 FORM A,5VDC	461434	15636	R7254-1	1	1	
L 1		INDUCTOR, 76 UH	655639	89536	655639	1		
L 2		INDUCTOR 2-4 MH	629337	89536	629337	1		
MP 1		HEATSINK	428805	13103	6046P8	2		
MP 2		COMPONENT HOLDER	422865	98159	2829-75-2	2		
MP 3		FUSE HLDR,CLIP,PCB,1/4 DIA FUSE	485219	91833	3529	2	5	
MP 4		BAG,SHIELDING,TRANSPARENT,12"X16"	680983	89536	680983	1		
Q 2, 3	*	TRANSISTOR,SI,N-MOS,POWER,TO-220AB	586107	89536	586107	2	1	
Q 4, 5, 7	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	3	1	
Q 6	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	195974	64713	2N3906	1	1	
R 1- 10		RES,CF,30,+-5%,0.25W	442228	80031	CR251-4-5P30E	10		
R 11, 13, 67,		RES,CF,270,+-5%,0.25W	348789	80031	CR251-4-5P270E	4		
R 69			348789					
R 12, 14		RES,CF,5.1K,+-5%,0.25W	368712	80031	CR251-4-5P5K1	2		
R 15, 36, 52,		RES,CF,3.9K,+-5%,0.25W	342600	80031	CR251-4-5P3K9	5		
R 70, 71			342600					
R 16, 44		RES,CF,27,+-5%,0.25W	348763	80031	CR251-4-5P27E	2		
R 17		RES,MF,102K,+-1%,0.125W,100PPM	291286	91637	CMF551023F	1		
R 18		RES,MF,309K,+-1%,0.125W,100PPM	235283	91637	CMF553093F	1		
R 19		RES,MF,29.4K,+-1%,0.125W,100PPM	235135	91637	CMF552942F	1		
R 20, 37, 38		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	3		
R 21, 24		RES,CF,910K,+-5%,0.25W	442533	89536	442533	2		
R 22, 45, 47,		RES,CF,100K,+-5%,0.25W	348920	80031	CR251-4-5P100K	5		
R 53, 63			348920					
R 23		RES,MF,28.7K,+-1%,0.125W,100PPM	235176	91637	CMF552872F	1		
R 25, 29		RES,MF,143K,+-1%,0.125W,100PPM	291336	91637	CMF551433F	2		
R 26		RES,MF,47.5K,+-1%,0.125W,100PPM	289546	91637	CMF554752F	1		
R 27		RES,MF,95.3K,+-1%,0.125W,100PPM	289561	91637	CMF559532F	1		
R 28		RES,MF,18.7K,+-1%,0.125W,50PPM	347088	91637	CMF551872F	1		
R 30		RES,MF,46.4K,+-1%,0.125W,100PPM	188375	89536	188375	1		
R 31		RES,MF,10K,+-1%,0.125W,100PPM	168260	91637	CMF551002F	1		
R 32		RES,MF,10.5K,+-1%,0.125W,100PPM	234096	91637	CMF551052F	1		
R 33		RES,MF,49.9K,+-1%,0.125W,100PPM	268821	91637	CMF554992F	1		
R 34		RES,MF,249,+-1%,0.125W,100PPM	168203	91637	CMF55249F	1		
R 35		RES,MF,2.05K,+-1%,0.125W,100PPM	293704	91637	CMF552051F	1		
R 39		RES,CF,100,+-5%,0.25W	348771	80031	CR251-4-5P100E	1		
R 40, 73		RES,CF,820K,+-5%,0.25W	348979	80031	CR251-4-5P820K	2		

TABLE 6-9. A8 POWER SUPPLY PCA
(SEE FIGURE 6-9.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
R 41- 43, 46,		RES,MF,24.9K,+-1%,0.125W,100PPM	291369	91637	CMF552492F	5		
R 65			291369					
R 48		RES,MF,348,+-1%,0.125W,100PPM	236778	89536	236778	1		
R 49		RES,MF,1.69K,+-1%,0.125W,100PPM	321414	91637	CMF551691F	1		
R 50		RES,MF,14.3K,+-1%,0.125W,100PPM	291617	91637	CMF551432F	1		
R 51		RES,CC,270,+-10%,2W	110189	89536	110189	1		
R 54, 55		RES,MF,2.26K,+-1%,0.125W,100PPM	328294	91637	CMF552261F	2		
R 56, 57		RES,VAR,CERM,100,+-10%,0.5W	275735	11236	360T-101A	2		
R 58		RES,MF,2.67K,+-1%,0.125W,100PPM	289587	91637	CMF552671F	1		
R 59		RES,MF,2.8K,+-1%,0.125W,100PPM	325670	91637	CMF552801F	1		
R 60		RES,CC,560,+-5%,1W	266361	89536	266361	1		
R 61, 62		RES,MF,4.99K,+-1%,0.125W,100PPM	168252	91637	MFF1-84991	2		
R 64		RES,MF,137,+-1%,0.125W,100PPM	235218	91637	CMF551370F	1		
R 66		RES,MF,10.2K,+-1%,0.125W,100PPM	293605	91637	CMF551022F	1		
R 68		RES,CF,1K,+-5%,0.25W	343426	80031	CR251-4-5P1K	1		
R 72		RES,CF,22K,+-5%,0.25W	348870	80031	CR251-4-5P22K	1		
TP 1, 3, 10,		CONN,TAB,FASTON,PRESS-IN,0.110 WIDE	512889	02660	62395	4		
TP 12			512889					
U 1	*	IC,LSTTL,QUAD DIFFERENTIAL LINE DRVR	525295	04713	MC3487P	1	1	
U 2	*	IC,LSTTL,QUAD RS422 LINE RCVR,3-STATE	525303	12040	DS3486N	1	1	
U 3, 5	*	IC, 2.5 V,40 PPM T.C.,BANDGAP REF	472845	04713	MC1403V	2	1	
U 4	*	IC,VOLT REG,FIXED,-12 VOLTS,1.5 AMPS	381665	04713	MC7912CP	1	1	
U 6	*	IC,COMPARATOR,QUAD,14 PIN DIP	387233	12040	LM339N	1	1	
U 7, 8	*	IC,REGULATING PULSE WIDTH MODULATOR	454678	01295	SG3524N	2	1	
U 9	*	IC,COMPARATOR,DUAL,LO-PWR,8 PIN DIP	478354	12040	LM393N	1	1	
U 10	*	IC,OP AMP,SELECTED GBW 600KHZ	418566	12040	LM358N	1	1	
U 11	*	IC,ARRAY,5 TRANS,NPN,3 ISO,2 DIFF CON	419002	89536	419002	1	1	
VR 1	*	ZENER,UNCOMP,6V TRANSIENT SUPPRESSOR	508655	24444	1N5908	1	1	
VR 2	*	ZENER,UNCOMP, 24.0V, 5%, 5.2MA, 0.4W	267807	04713	1N970B	1	1	
VR 3	*	ZENER,UNCOMP, 15.0V, 5%, 8.5MA, 0.4W	266601	04713	1N965B	1	1	
VR 4	*	ZENER,UNCOMP, 18.0V, 5%, 7.0MA, 0,4W	327973	04713	1N967B	1	1	
VR 5	*	ZENER,UNCOMP, 5.1V, 5%, 20.0MA, 0.4W	159798	04713	1N751A	1	1	
Z 1		RES,NET,SIP,10 PIN,5 RES,10K,+-2%	529990	89536	529990	1		
Z 2		RES,NET,SIP,10 PIN,5 RES,56K,+-2%	529131	89536	529131	1		

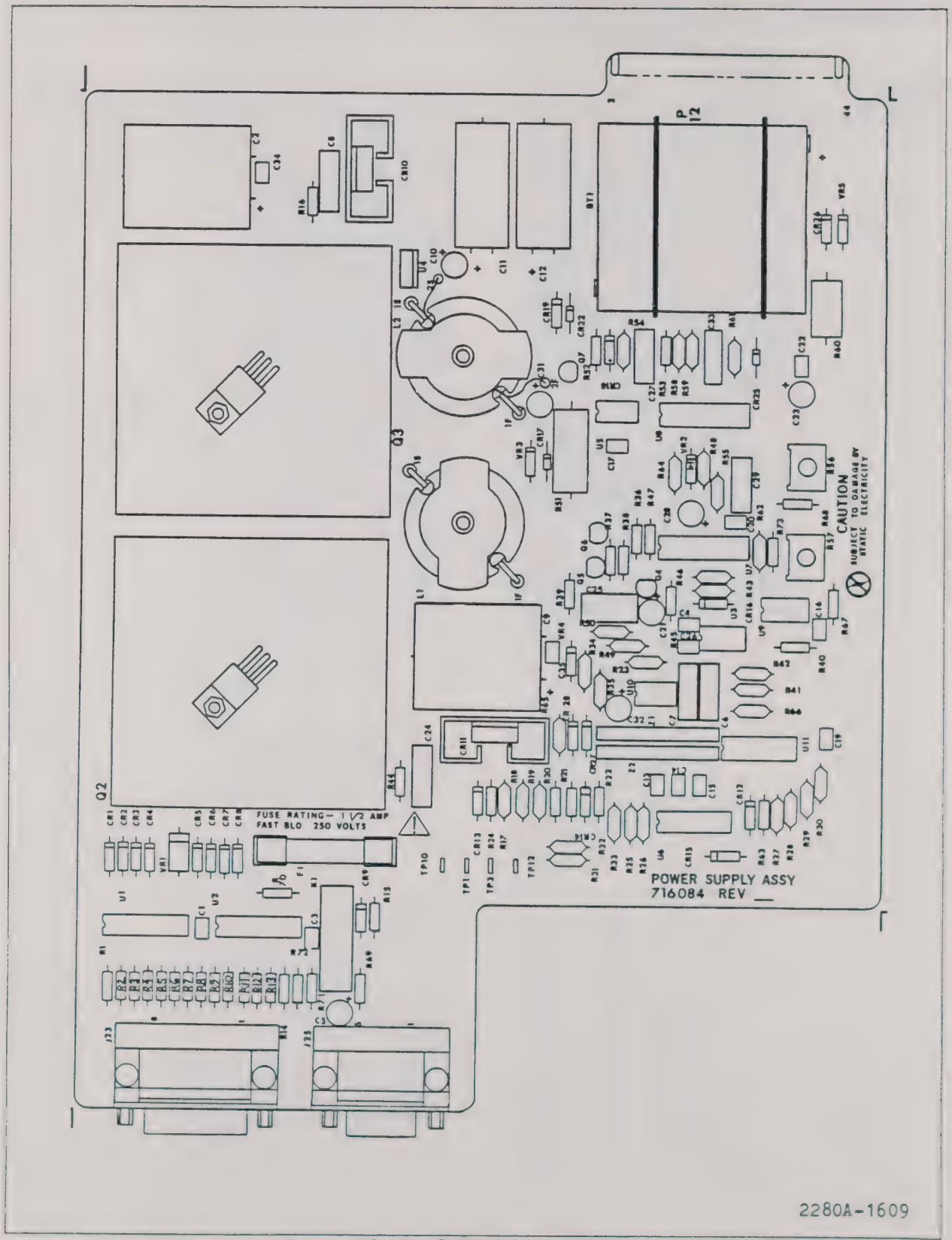
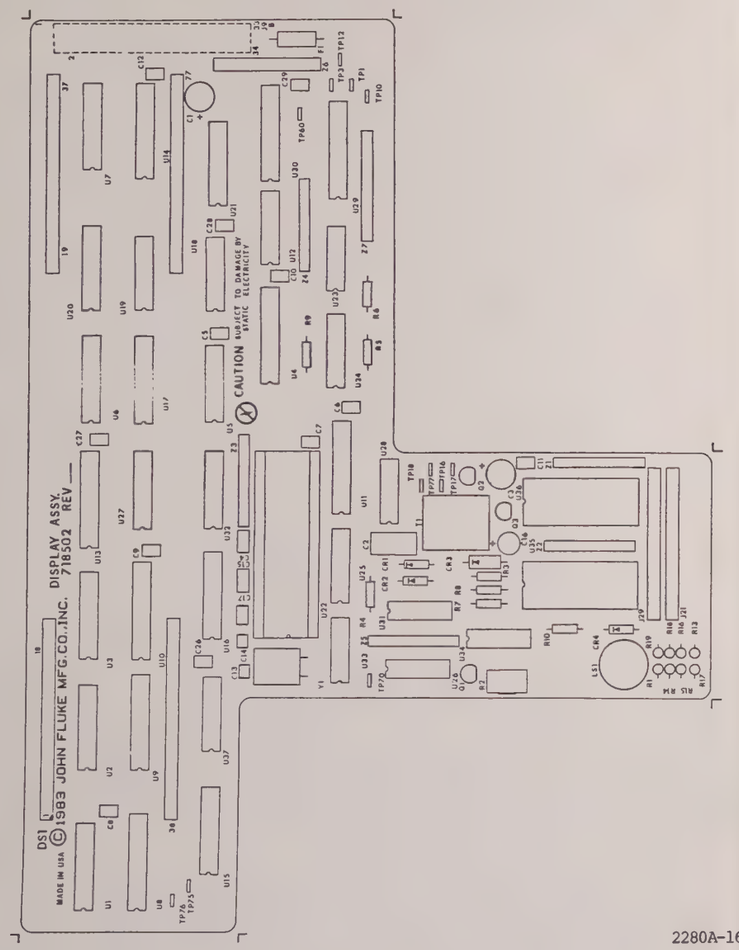
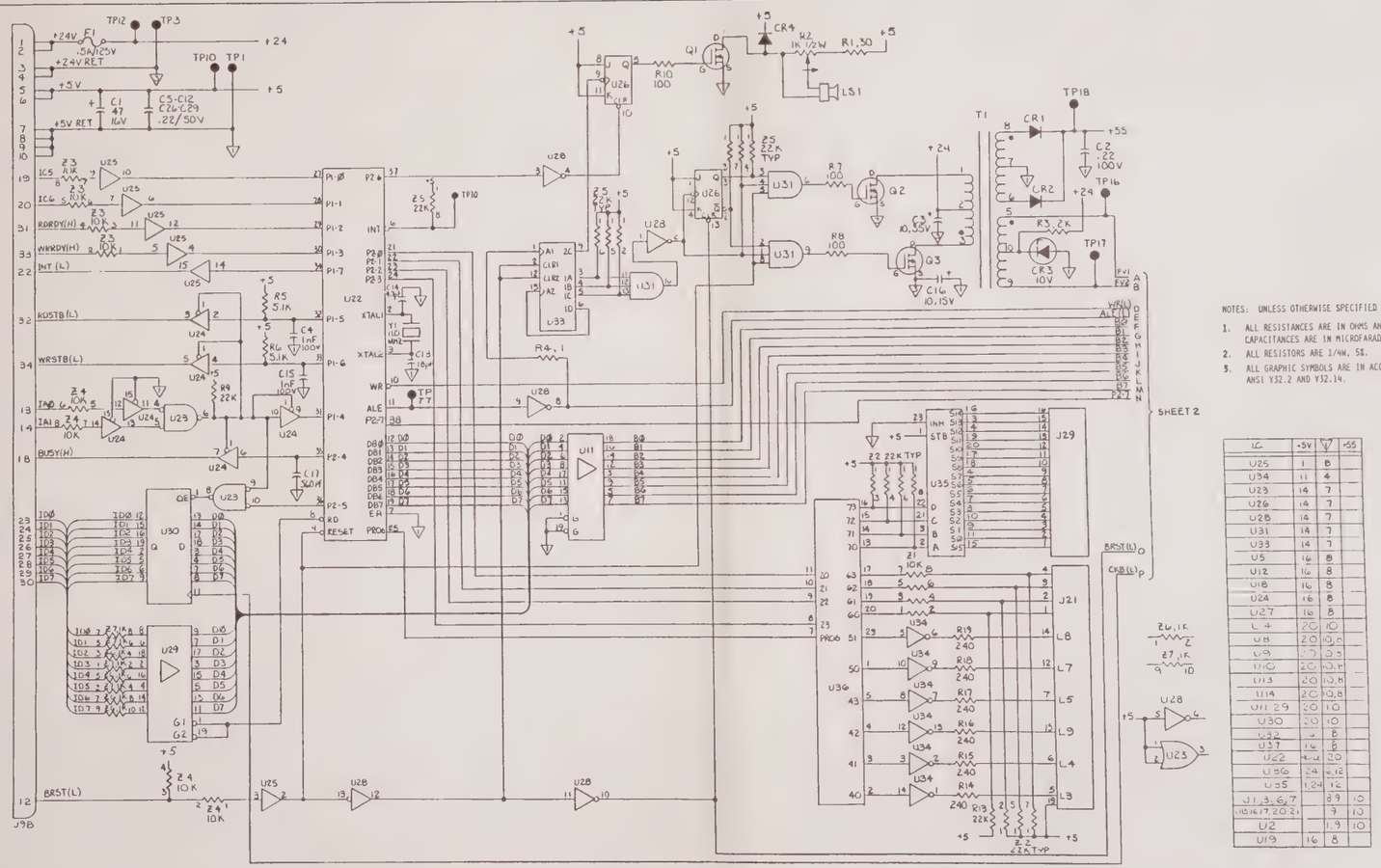


Figure 6-9. A8 Power Supply PCA



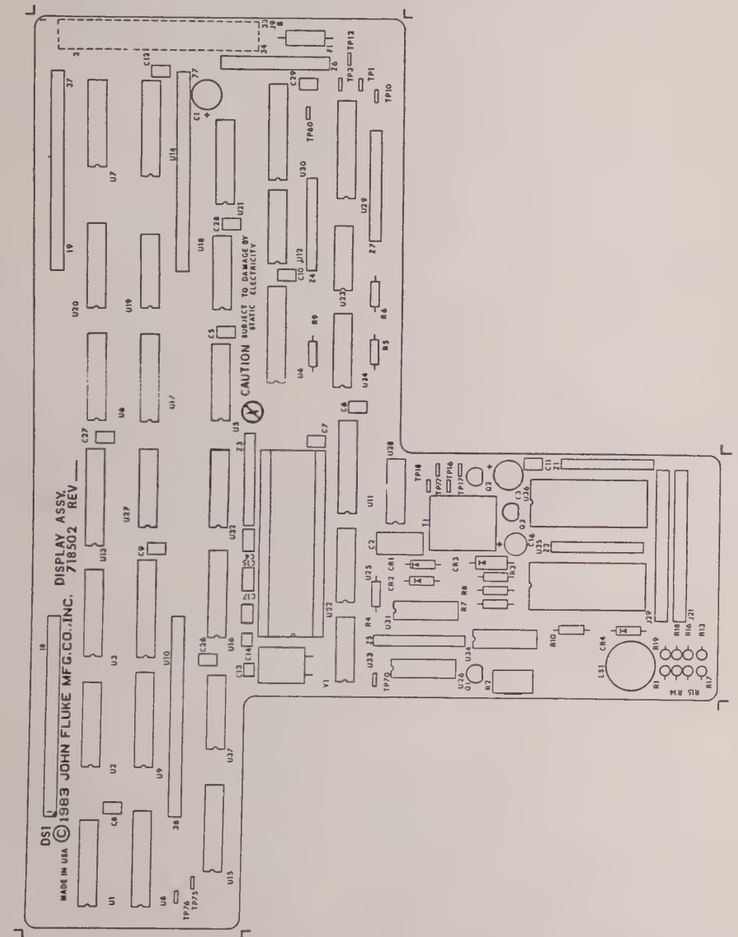
2280A-1606



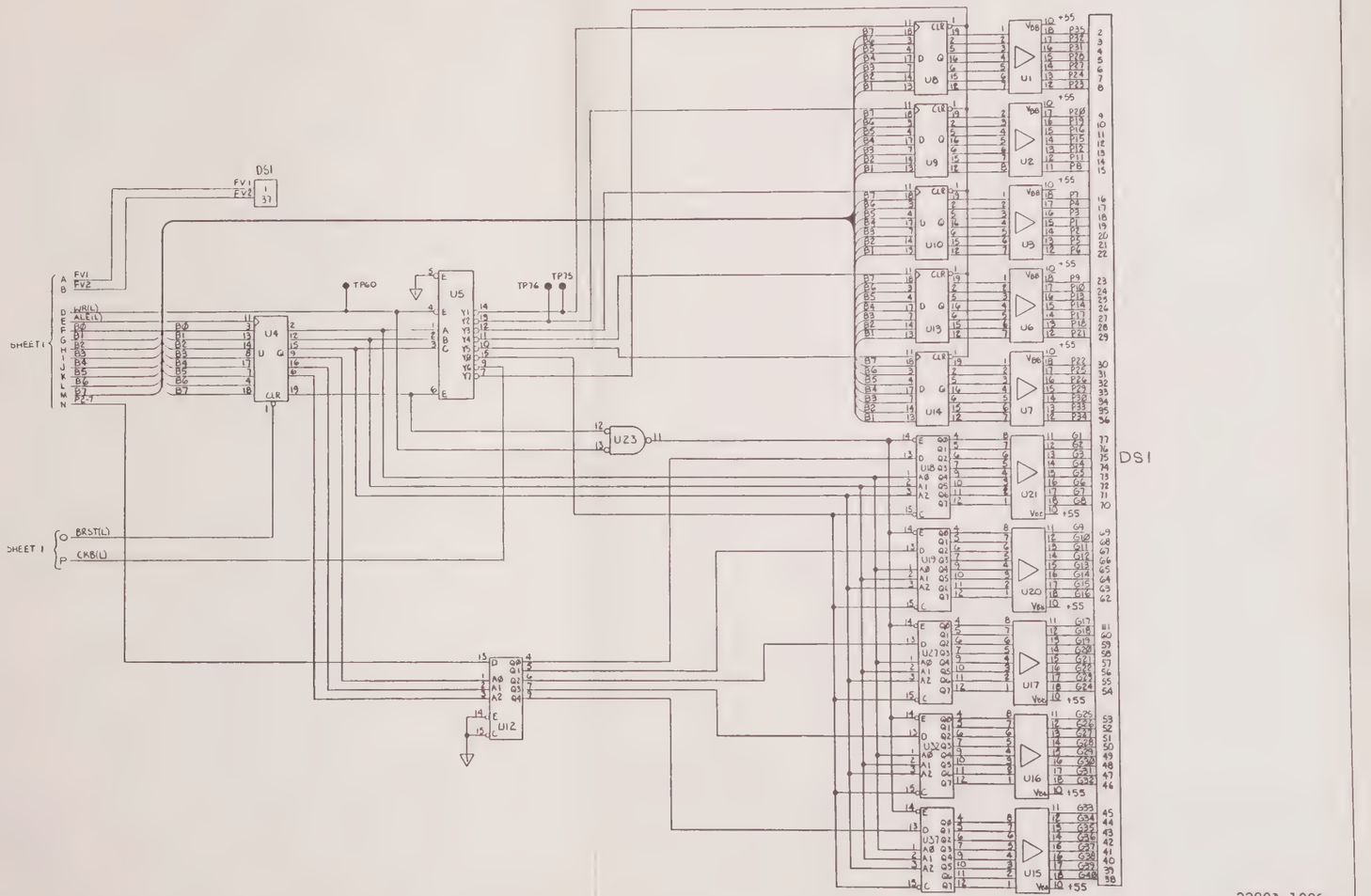
IC	+5V	⏚	+55
U25	1	8	
U34	11	4	
U23	14	7	
U26	14	7	
U28	14	7	
U31	14	7	
U33	14	7	
U5	16	8	
U12	16	8	
U18	16	8	
U24	16	8	
U27	16	8	
U +	20	10	
U8	20	10	
U9	20	10	
U10	20	10	
U13	20	10	
U14	20	10	
U11 29	20	10	
U30	20	10	
U32	16	8	
U37	16	8	
U22	40	20	
U36	24	12	
U35	1,24	12	
U1,3,6,7		8,9	10
U15,16,17,20,21		9	10
U2		1,9	10
U19	16	8	

2280A-1006
(Sheet 1 of 2)

Figure 7-1. A1 Display PCA



2280A-1606



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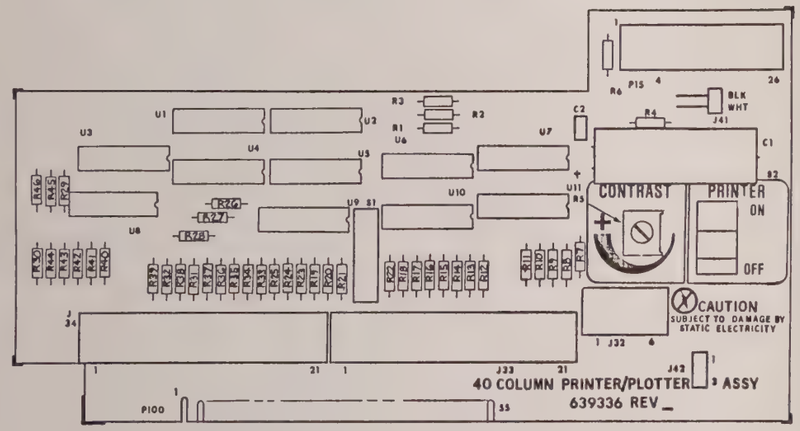
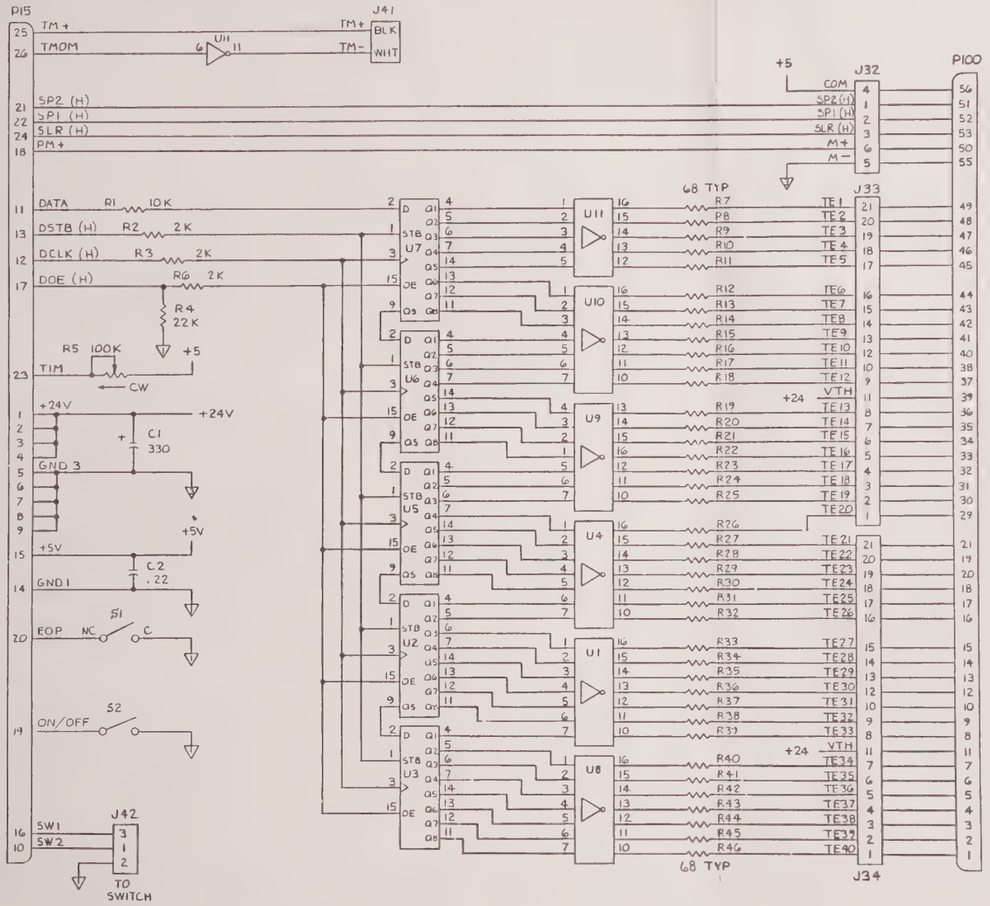
(Sheet 2 of 2)

Figure 7-1. A1 Display PCA (cont.)



2280A-1015



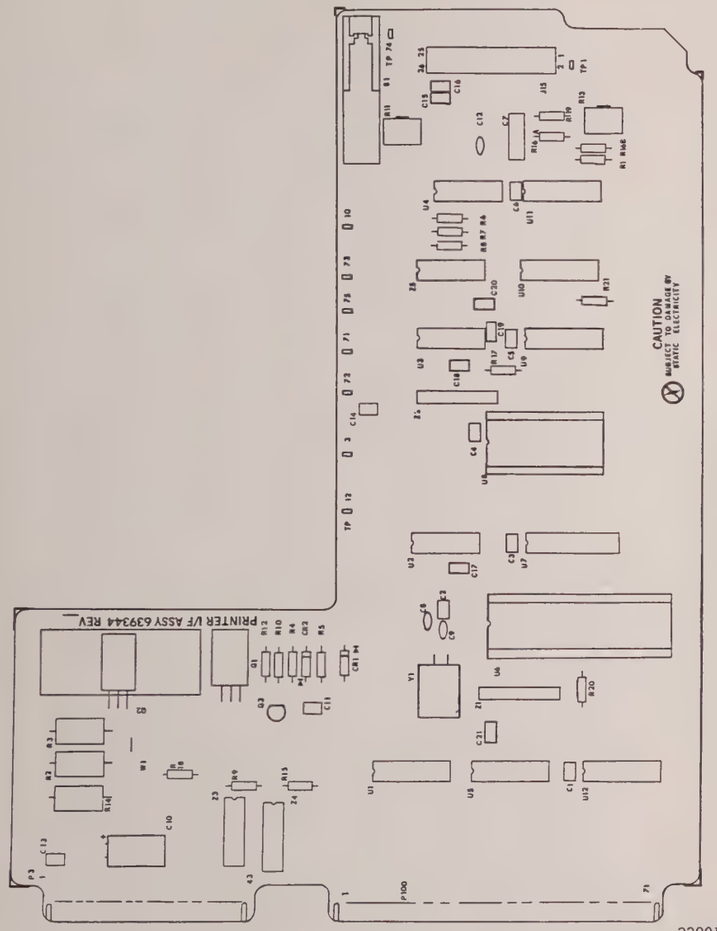
NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL RESISTANCES ARE IN OHMS
2. ALL CAPACITANCE IS IN MICROFARADS.
3. ALL GRAPHIC SYMBOLS ARE IN ACCORDANCE WITH ANSI Y32.2 AND Y32.14.

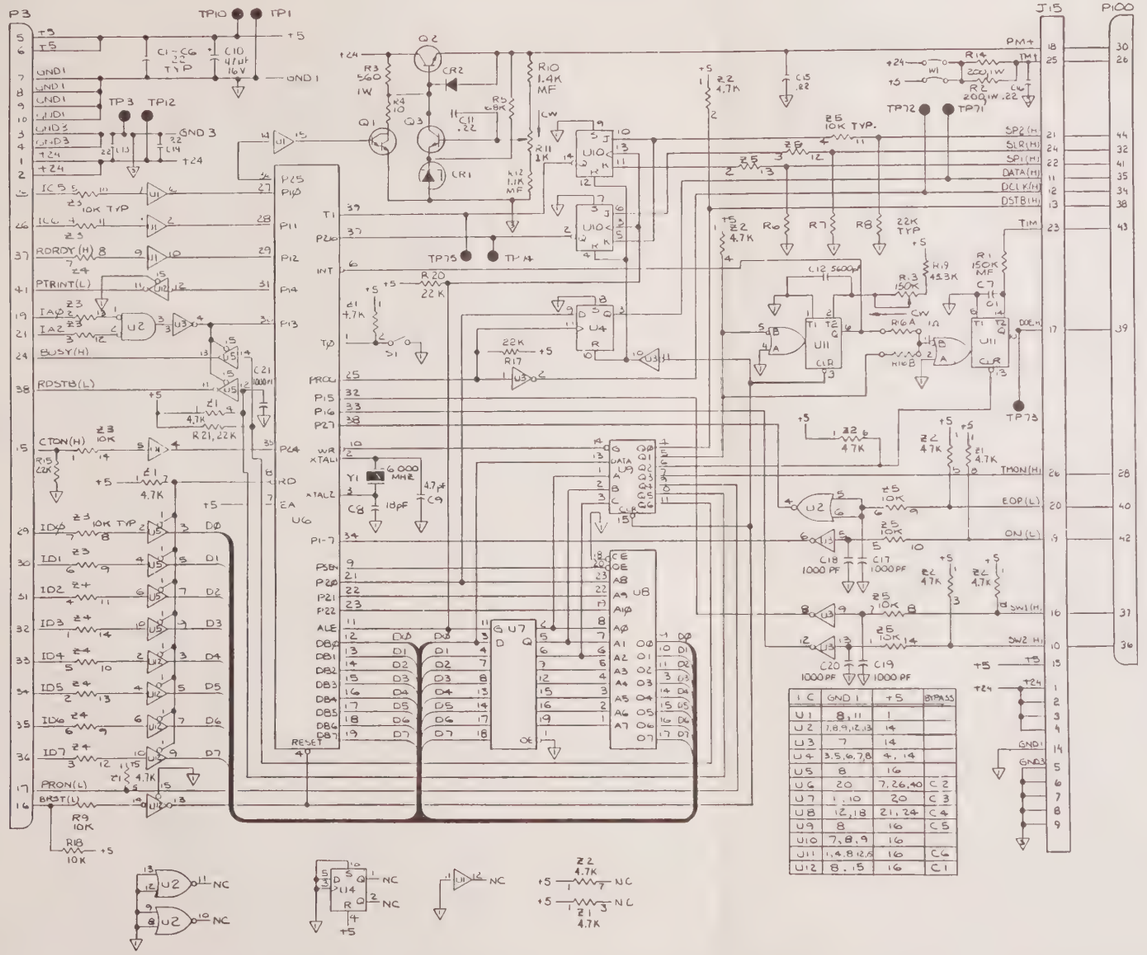
IC PWR & GND					
IC	TYPE	GND1	GND3	+5V	+24V
U2	4094	8	—	16	—
U3	4094	8	—	16	—
U5	4094	8	—	16	—
U6	4094	8	—	16	—
U7	4094	8	—	16	—
U1	ULN2003	—	8	—	9
U4	ULN2003	—	8	—	9
U8	ULN2003	—	8	—	9
U9	ULN2003	—	8	—	9
U10	ULN2003	—	8	—	9
U11	ULN2003	—	8	—	9

2280A-1615

Figure 7-2. A2 Printer Driver PCA



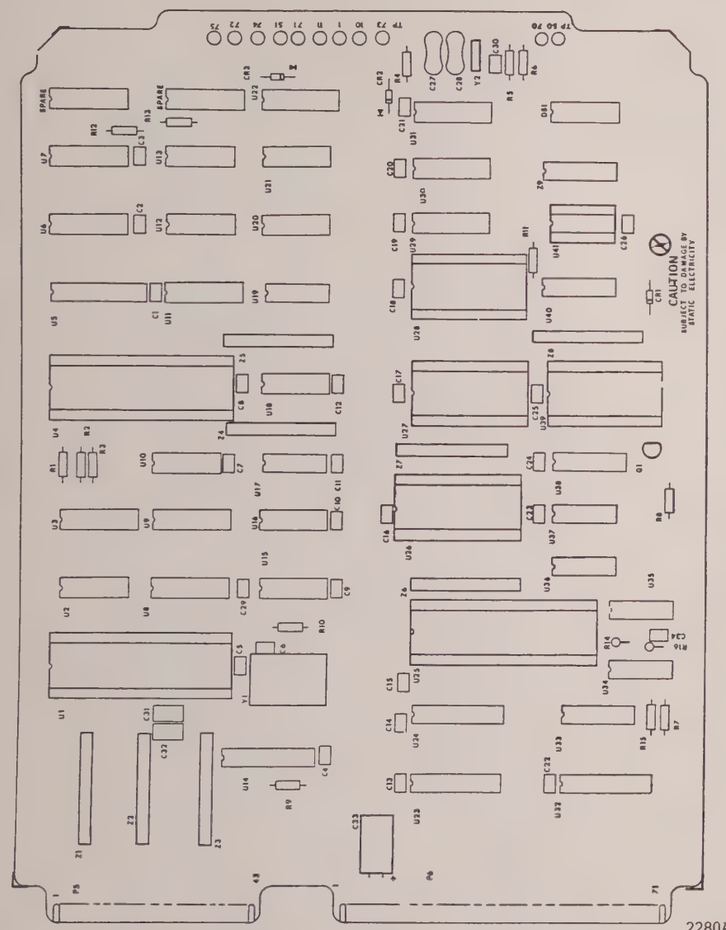
2280A-1616



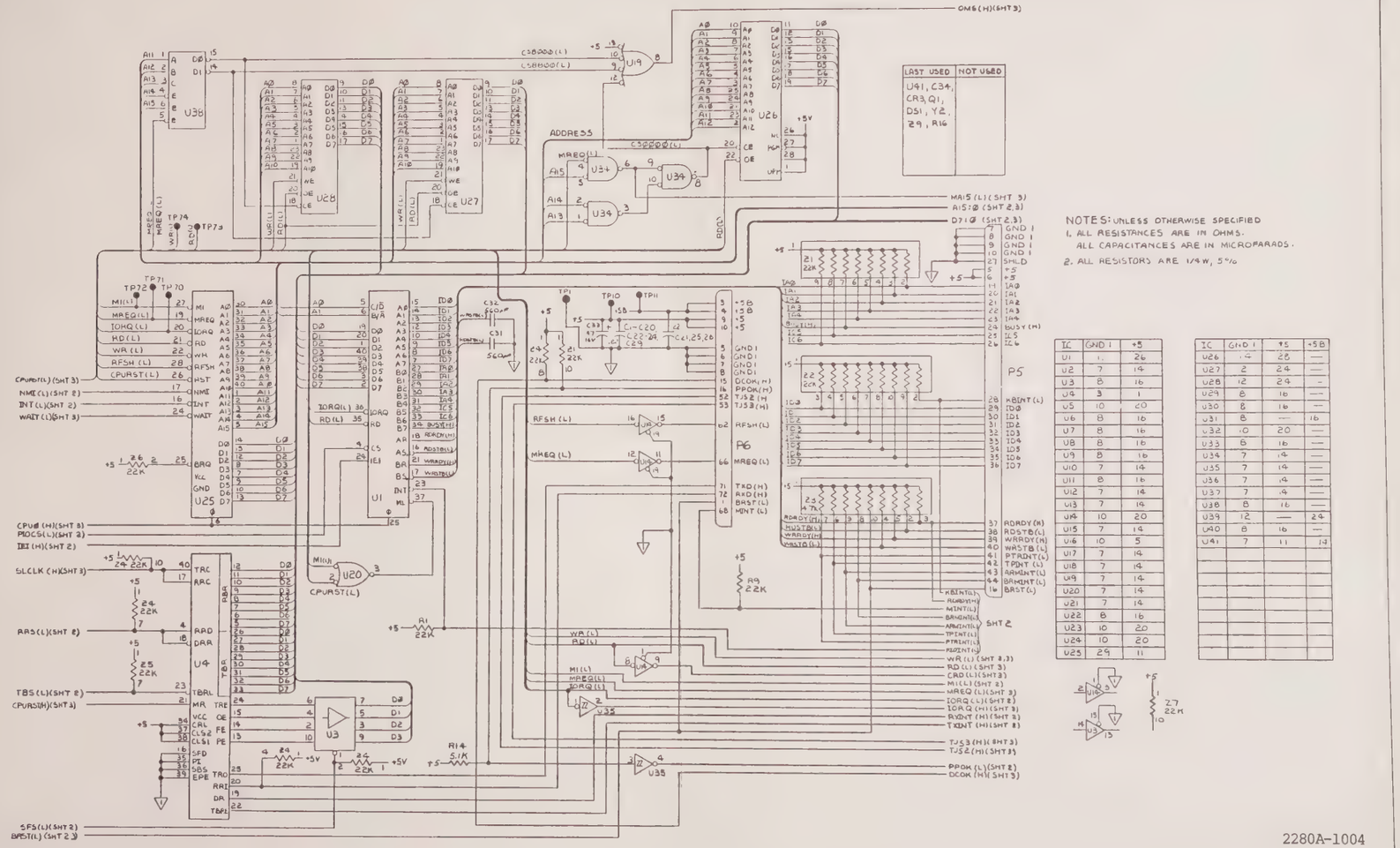
I C	GND I	+5	BYPASS
U1	8, 11	1	
U2	7, 8, 9, 12, 13	14	
U3	7	14	
U4	3, 5, 6, 7, 8	4, 14	
U5	8	16	
U6	20	7, 26, 40	C 2
U7	1, 10	20	C 3
U8	12, 18	21, 24	C 4
U9	8	16	C 5
U10	7, 8, 9	16	
U11	1, 4, 8, 12, 15	16	C 6
U12	8, 15	16	C 1

2280A-1016

Figure 7-3. A3 Printer Interface PCA



2280A-1604


NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCES ARE IN OHMS.
ALL CAPACITANCES ARE IN MICROFARADS.
2. ALL RESISTORS ARE 1/4W, 5%
LAST USED
U41, C34, CR3, Q1, DS1, Y2, Z9, R16
NOT USED

2280A-1004
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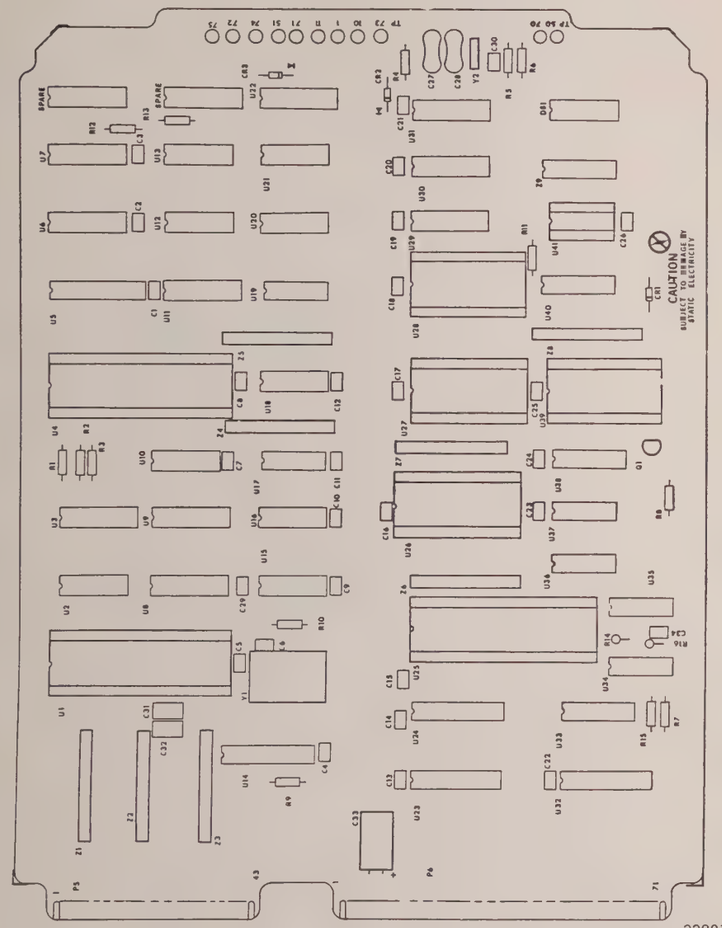
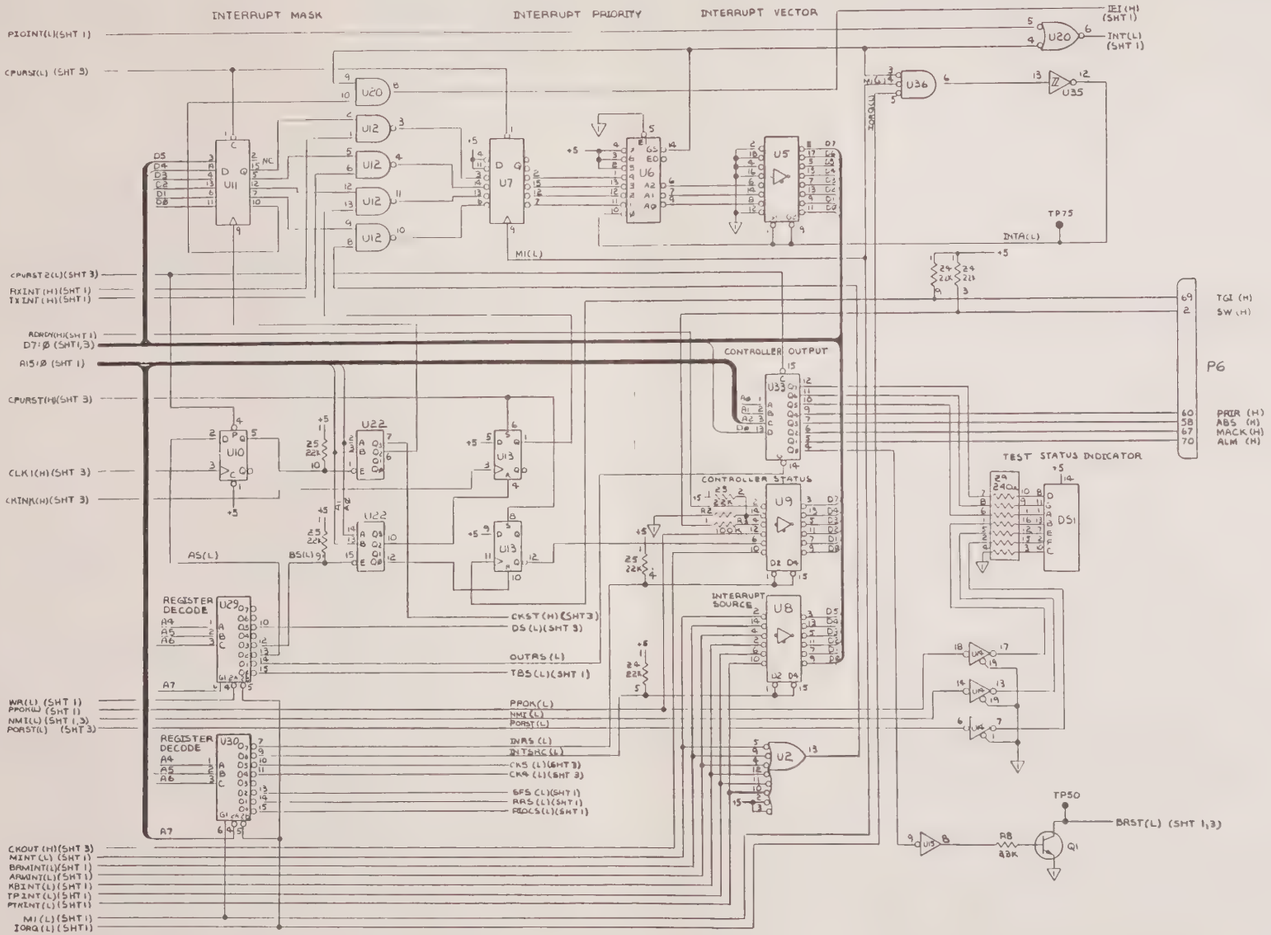
Figure 7-4. A4 Controller PCA

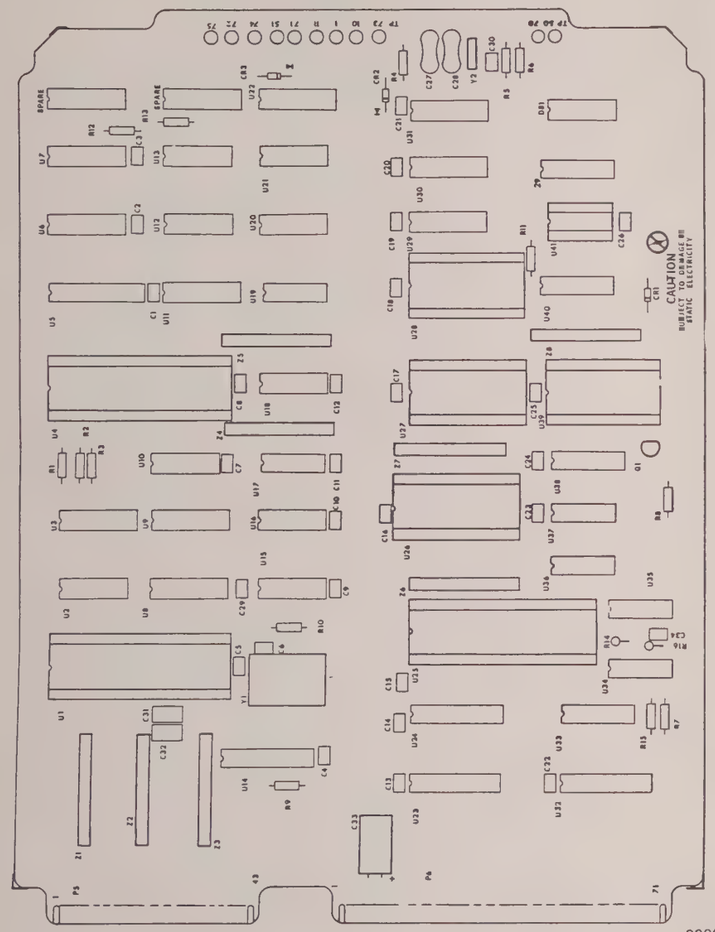


2280A-1604

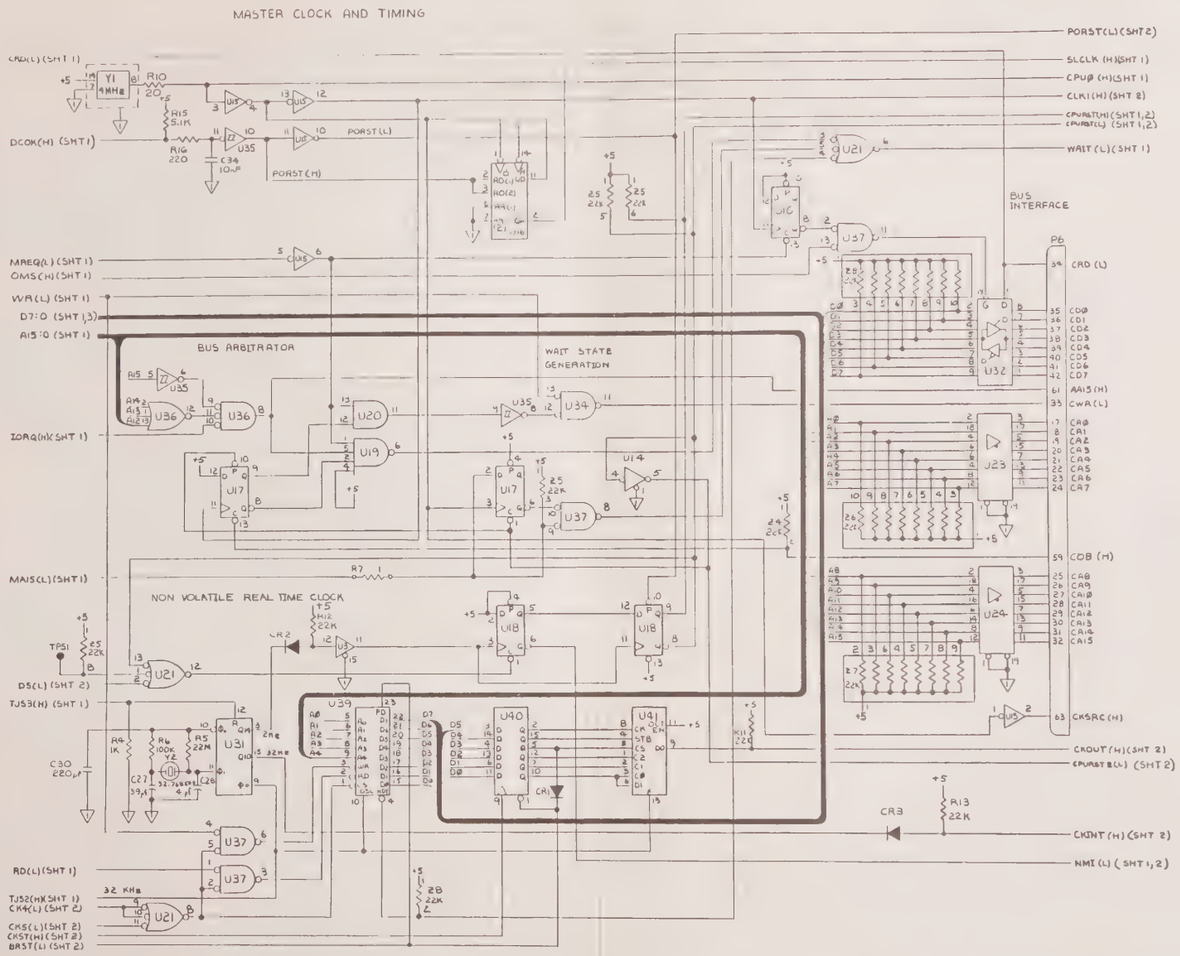


2280A-1004
(Sheet 2 of 3)

Figure 7-4. A4 Controller PCA (cont.)



2280A-1604



2280A-1004
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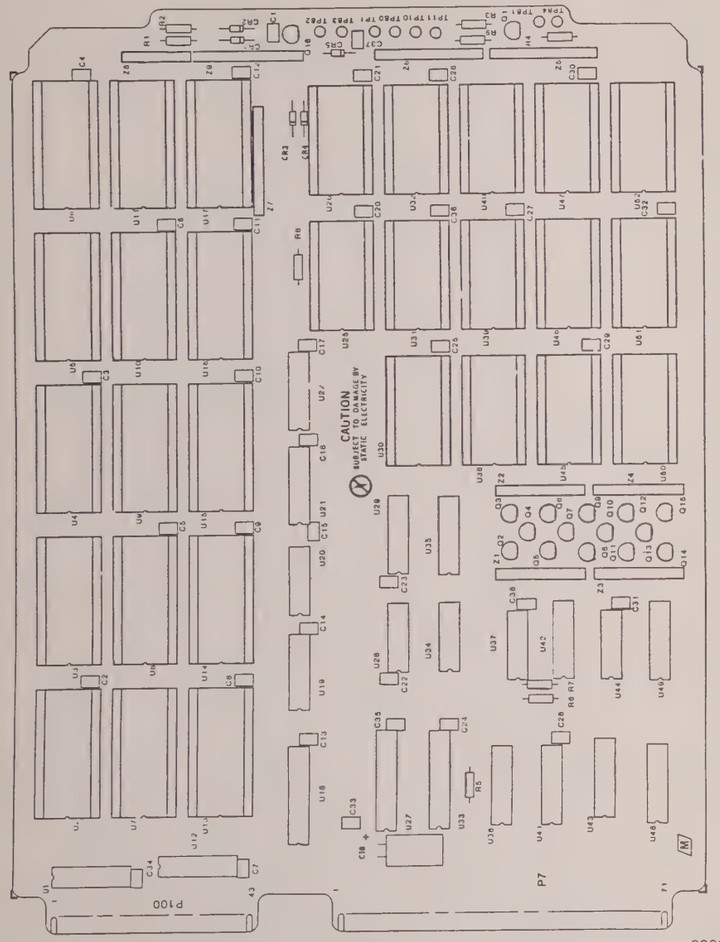
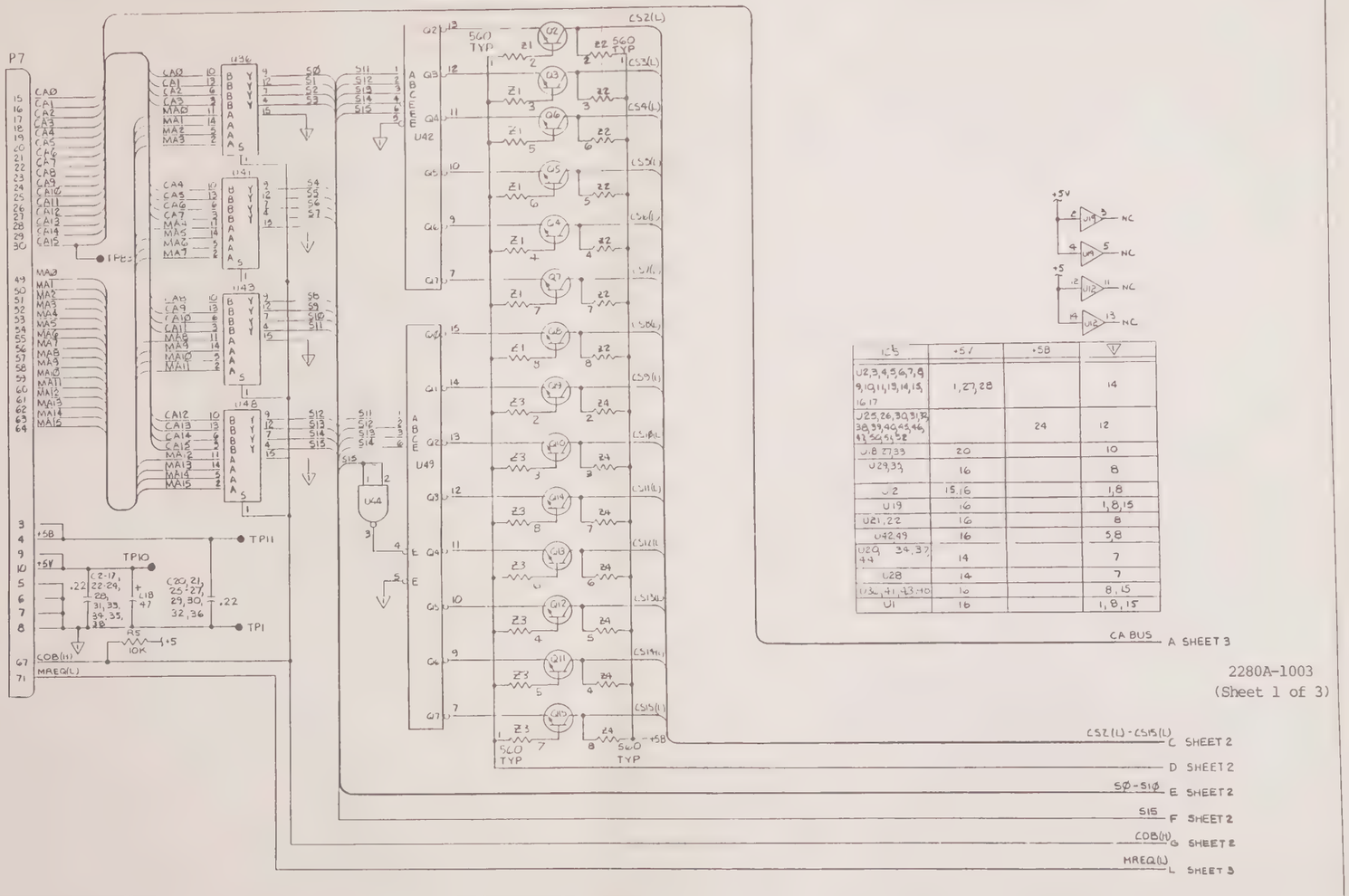
Figure 7-4. A4 Controller PCA (cont.)

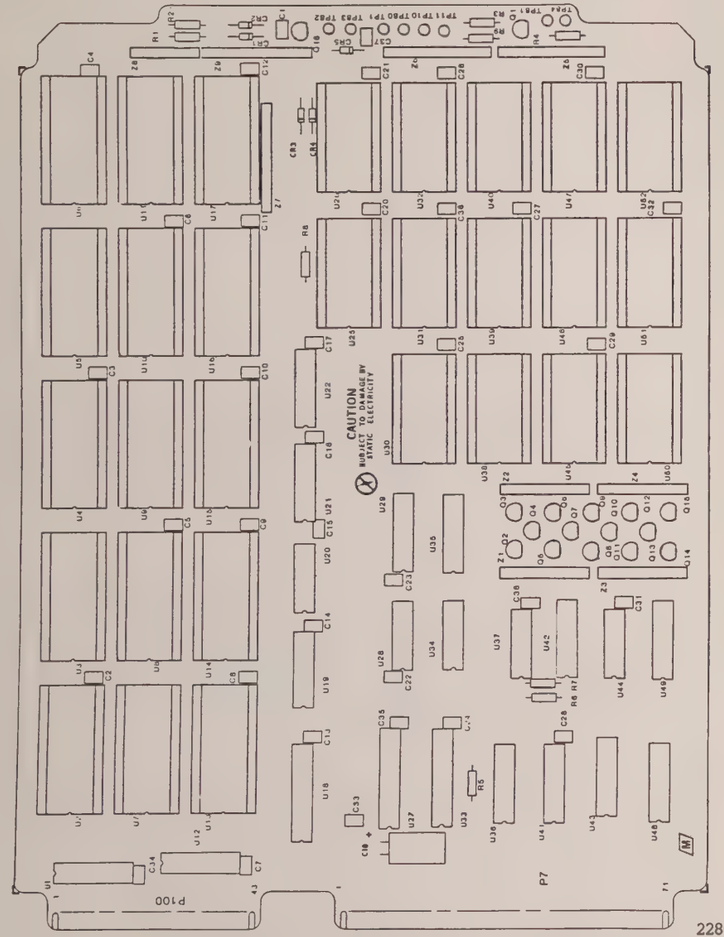


2280A-1603

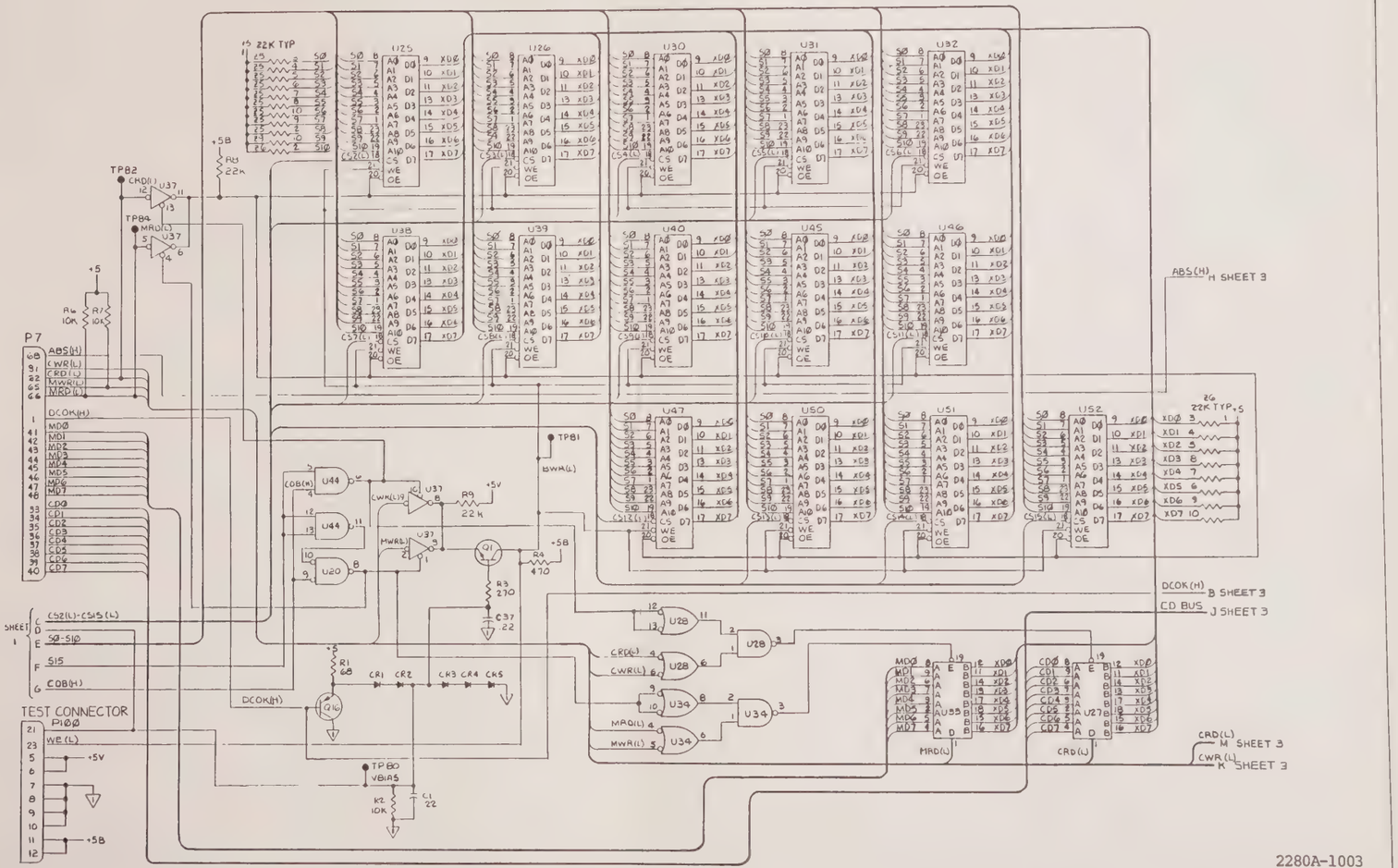


IC'S	+5V	+5B	V
U2,3,4,5,6,7,8,9,10,11,13,14,15,16,17	1,27,28		14
U25,26,30,31,32,38,39,40,45,46,47,50,51,58		24	12
U6,27,33	20		10
U29,34	16		8
U12	15,16		1,8
U19	16		1,8,15
U21,22	16		8
U42,49	16		5,8
U20, 34, 37, 44	14		7
U28	14		7
U36, 41, 43, 48	16		8,15
U1	16		1,8,15

Figure 7-5. A5 Memory PCA

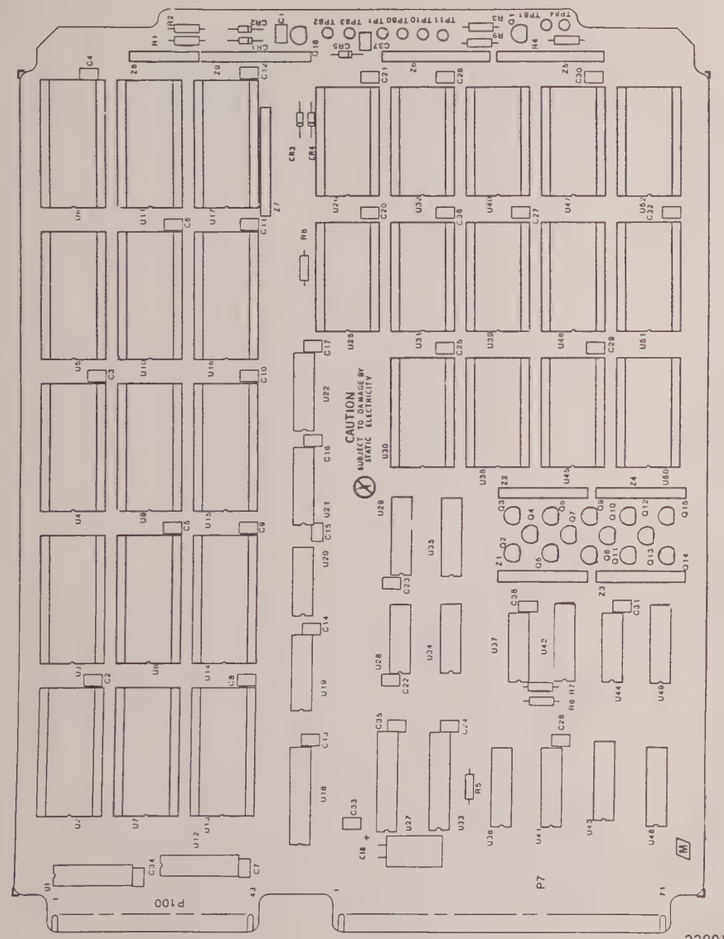


2280A-1603

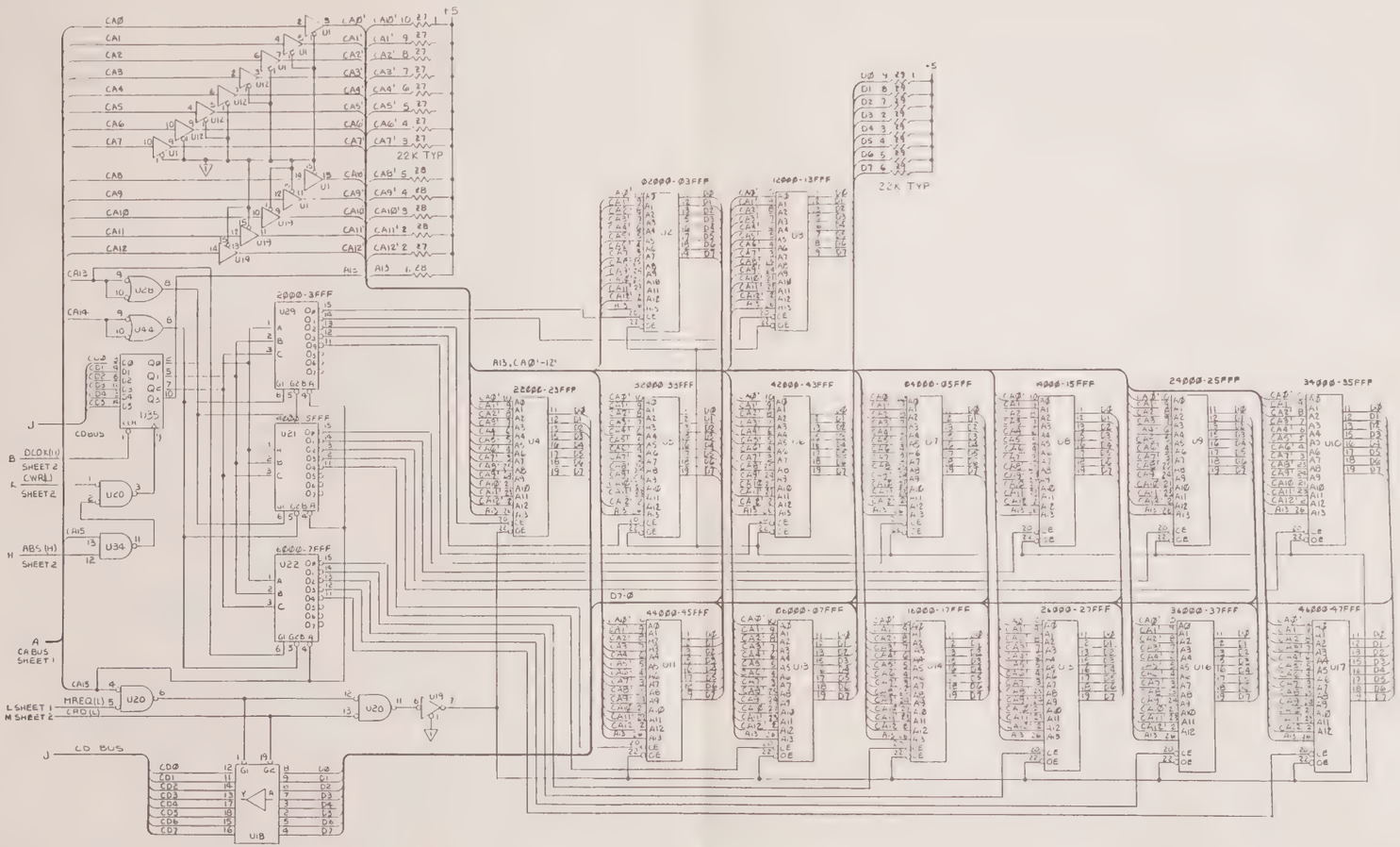


2280A-1003
(Sheet 2 of 3)

Figure 7-5. A5 Memory PCA (cont.)

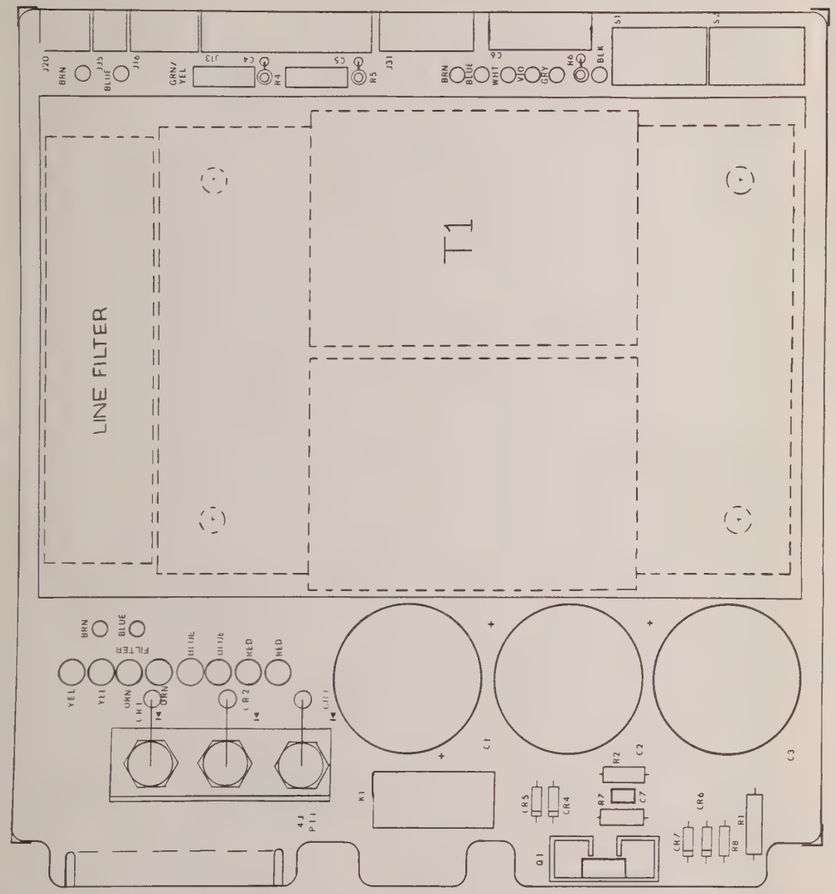


2280A-1603

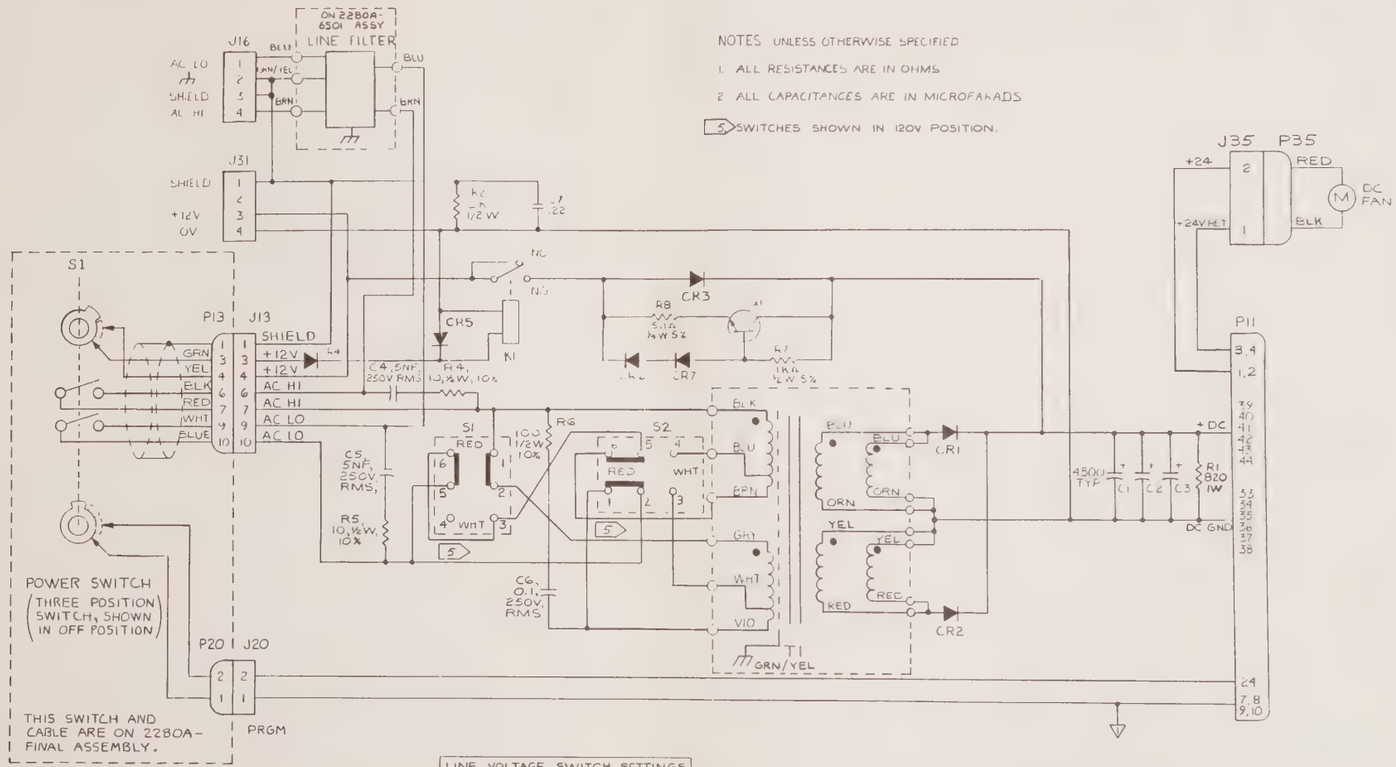


2280A-1003
(Sheet 3 of 3)

Figure 7-5. A5 Memory PCA (cont.)



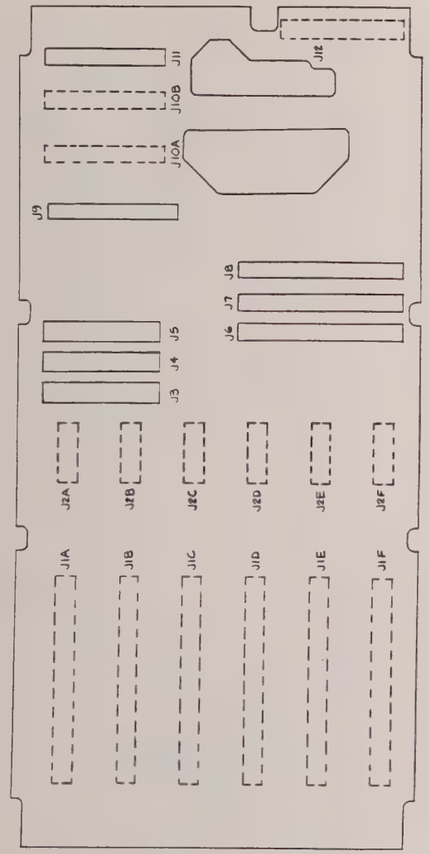
2280A-1602



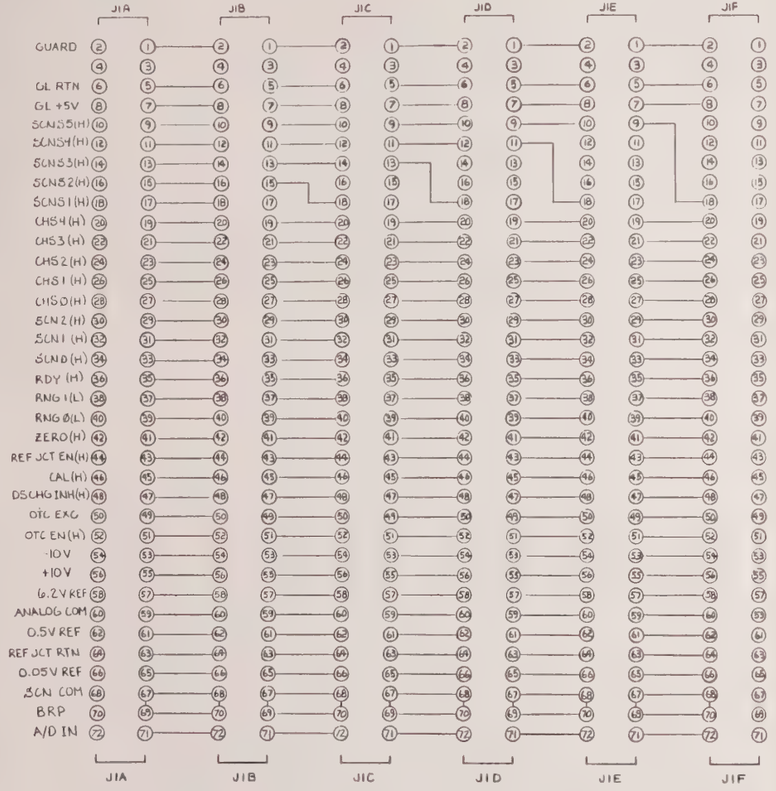
LINE VOLTAGE SWITCH SETTINGS		
VOLTAGE	S1	S2
100	RED	WHT
120	RED	RED
220	WHT	WHT
240	WHT	RED

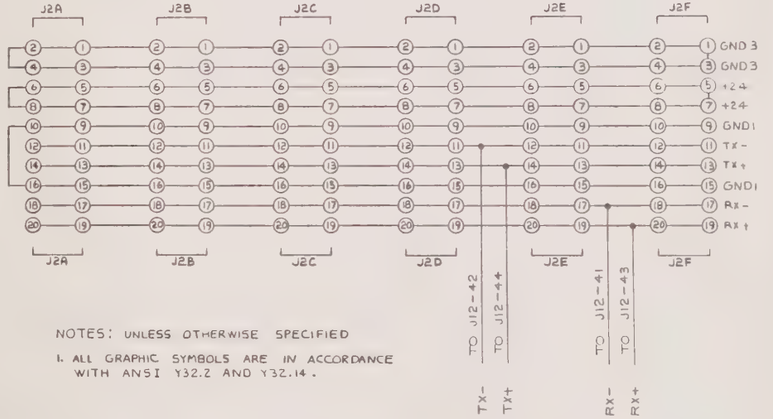
2280A-1002

Figure 7-6. A6 Transformer PCA



2280A-1601



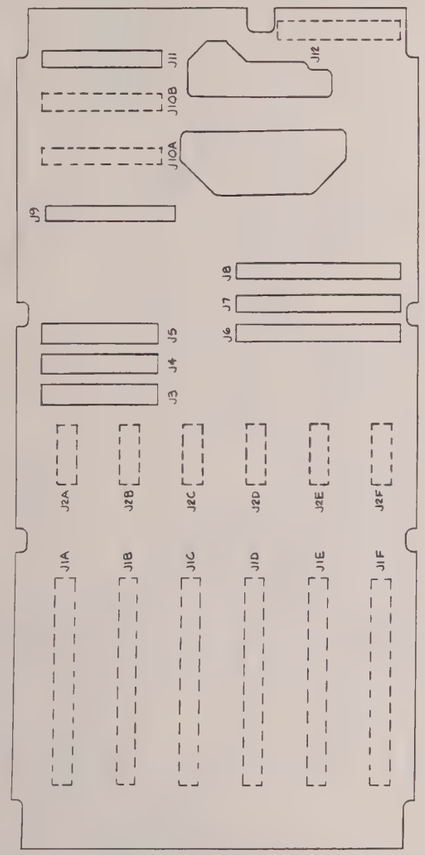


NOTES: UNLESS OTHERWISE SPECIFIED

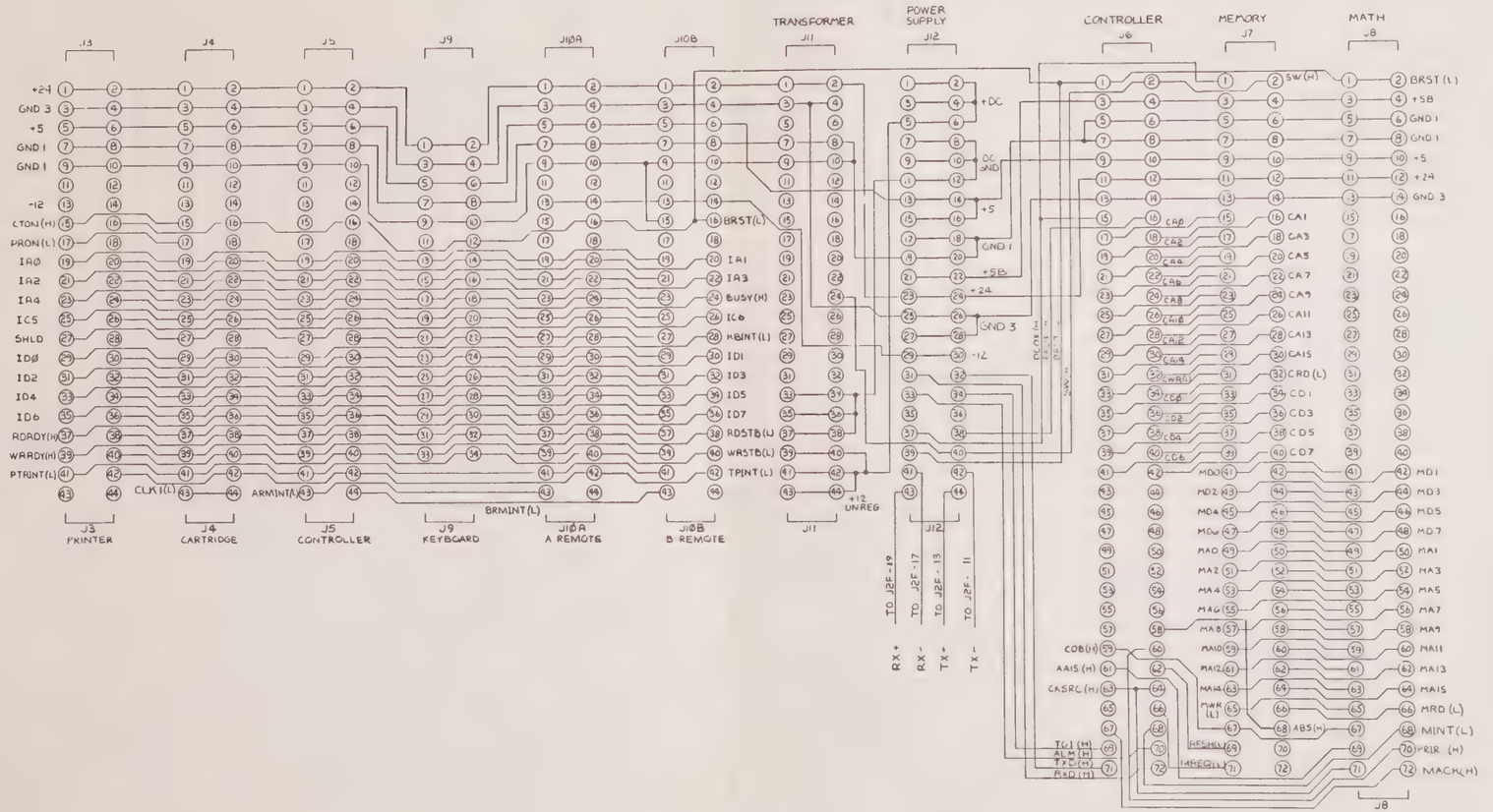
1. ALL GRAPHIC SYMBOLS ARE IN ACCORDANCE WITH ANSI Y32.2 AND Y32.14.

2280A-1001
(Sheet 1 of 2)

Figure 7-7. A7 Motherboard PCA



2280A-1601



2280A-1001
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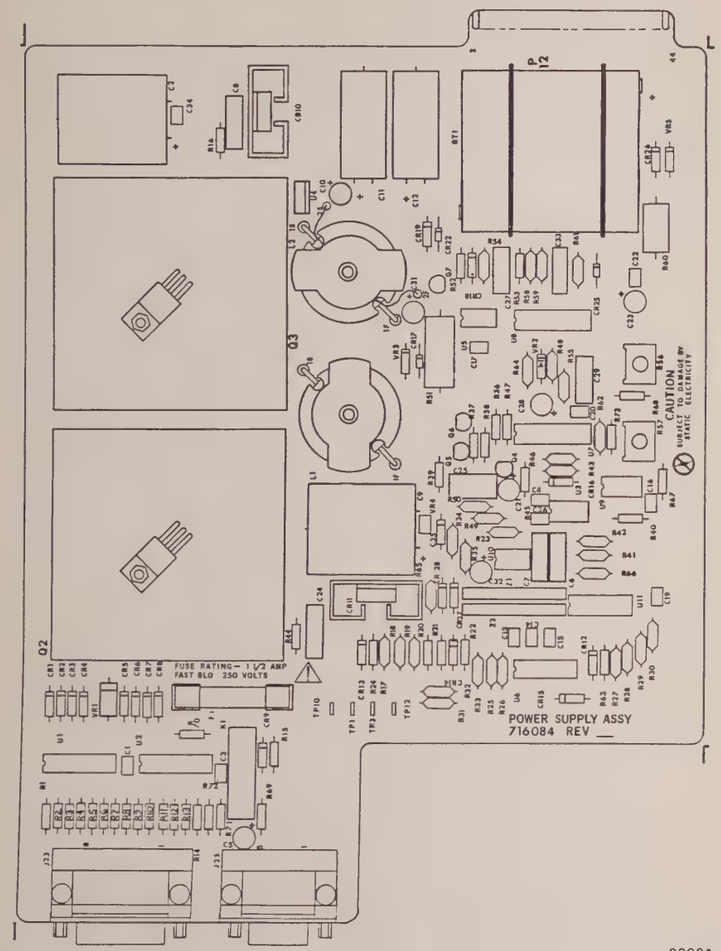
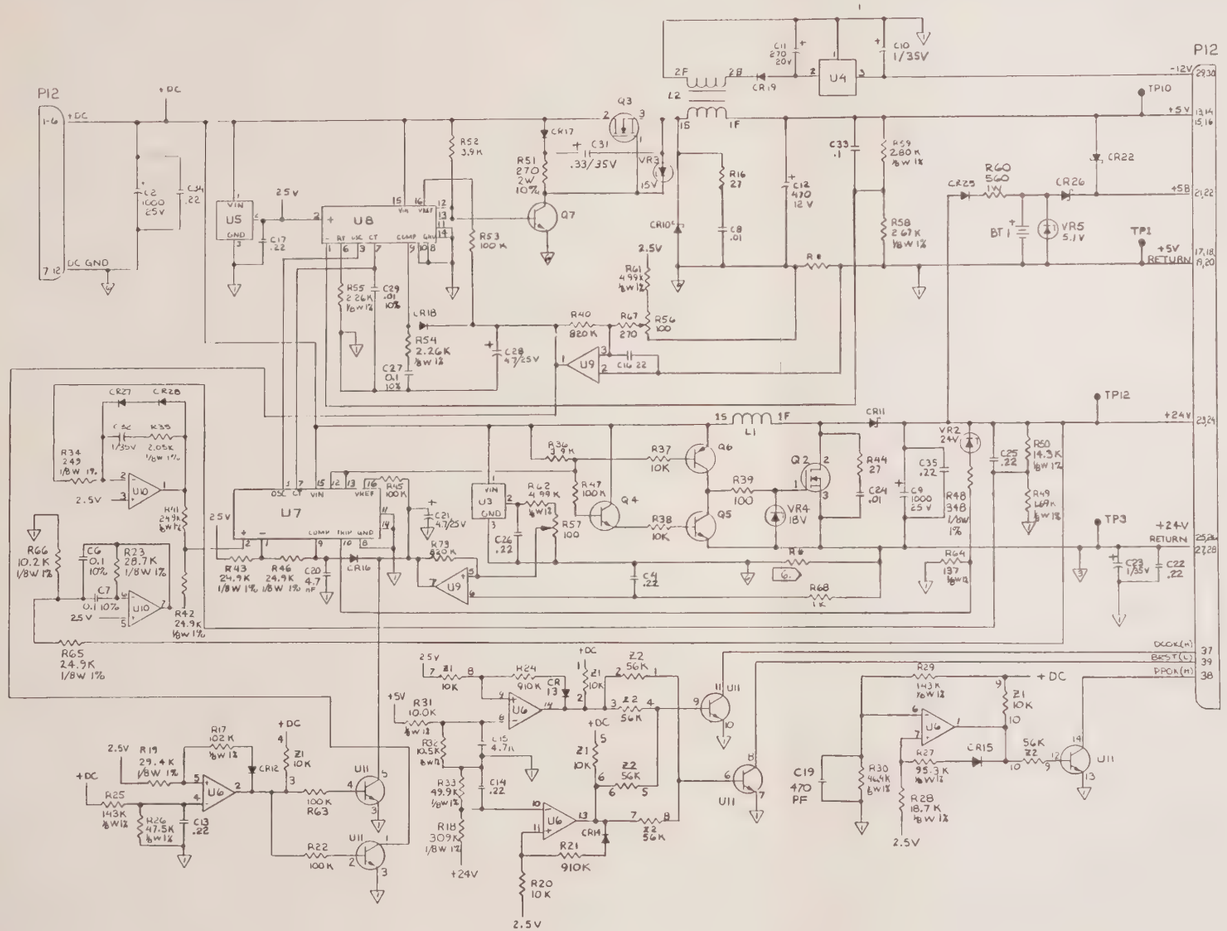
Figure 7-7. A7 Motherboard PCA (cont.)



2280A-1609



NOTES: UNLESS OTHERWISE SPECIFIED

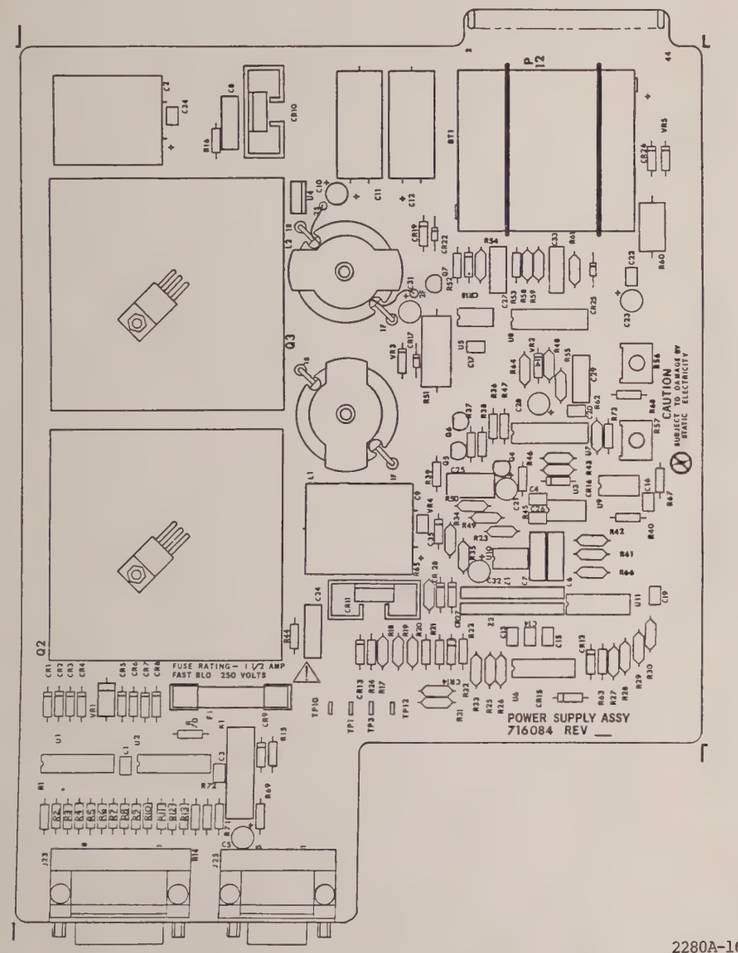
1. RESISTANCE IS IN OHMS AND CAPACITANCE IS IN MICROFARADS.
2. ALL RESISTORS ARE 1/4W, 5%.
3. ALL GRAPHIC SYMBOLS ARE IN ACCORDANCE WITH ANSI Y32.2 AND Y32.14.
4. ALL 1/8W 1% RESISTORS ARE METAL FILM.

IC	+15V	+24V			+DC
U1	16		8	—	—
U2	16		8	—	—
U3	—	—	—	3	1
U4	—	—	1	—	—
U5	—	—	3	—	1
U6	—	—	12	—	3
U7	—	—	4,5,8,11,14	—	15
U8	—	—	4,5,8,10,11,14	—	15
U9	—	—	4	—	8
U10	—	—	4	—	8
U11	—	—	3,7,10,13	—	—

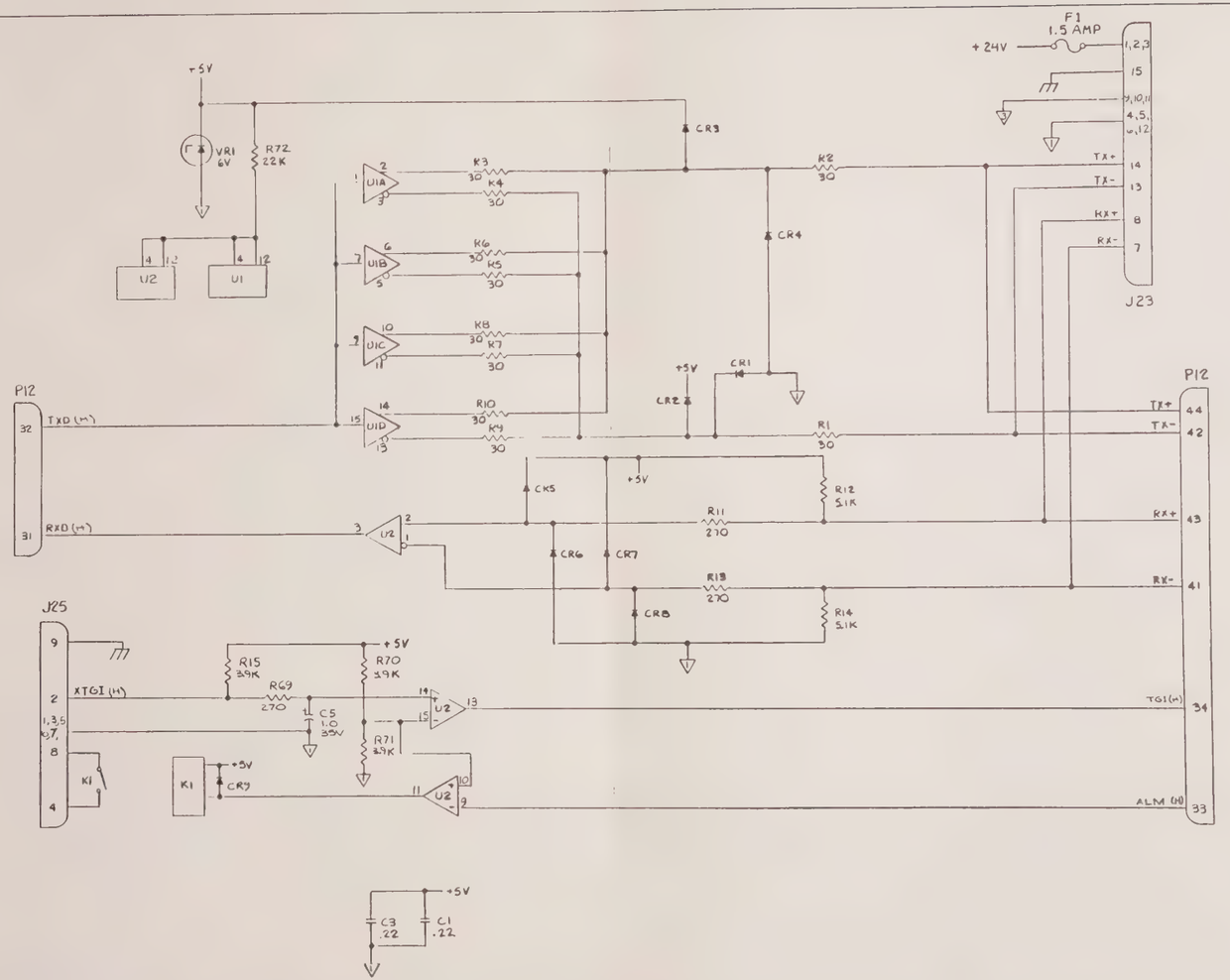
REF DES	
LAST USED	NOT USED
U11	VR5 C18,30
CR28	Q7 CR20 21,23,24
R73	C35 Q1
BT1 L2 K1	
Z2	

2280A-1009
(Sheet 1 of 2)

Figure 7-8. A8 Power Supply PCA



2280A-1609



2280A-1009
(Sheet 2 of 2)

Figure 7-8. A8 Power Supply PCA (cont.)

SECTION 8

OPTIONS -160 THROUGH -169

CONTENTS

Option 2280A-160 AC Voltage Input Connector 160-1
Option 2280A-161 High Performance A/D Converter 161-1
Option 2280A-162 Thermocouple/DC Volts Scanner 162-1
Option 2280B-163 RTD/Resistance Scanner 163-1
Option 2280A-164 Transducer Excitation 164-1
Option 2280A-168 Digital I/O Assembly 168-1
Option 2280A-169 Status Output Connector 169-1

DESCRIPTION

The AC Volts Input Connector mates with the Thermocouple/DC Volts Scanner and converts ac input voltages to dc for input to the scanner. Ten ac-voltage input and ten dc-voltage input channels are provided on the connector. The input connector mates to the Thermocouple/DC Volts Scanner through a card-edge connector. The entire assembly is enclosed in a plastic housing that provides strain relief for the external wiring to the connector terminals.

Two screw terminals labeled HI and LO are provided for each channel. Channels zero through nine are ac voltage input channels and channels ten through nineteen are dc voltage input channels. Channels zero through nine accept and convert ac voltages between 5V ac RMS and 250V ac RMS to dc voltages to be read by the 2280 using the High Performance A/D Converter (2280A-161 option) and the Thermocouple/DC Volts Scanner (2280A-162 option). Channels ten through nineteen can be used to measure dc voltages to 64 volts.

The LO input terminal and a shield are connected together within the assembly so that system guard and the LO input are at the same potential. This helps minimize common mode voltage errors in the measurement.

WHERE TO FIND FURTHER INFORMATION

The AC Voltage Input Connector theory of operation, general maintenance procedures, performance tests, calibration procedure, a parts list, and a schematic diagram can be found in this subsection. Installation and system configuration instructions are located in the 2280 Series System Guide, and operating and programming instructions are in the 2280 Series User Guide. Option specifications are located in the Appendices of this manual and in the System Guide.

Test equipment required to perform the procedures in this subsection is listed in Table 160-1. A summary of test equipment required for all procedures in this manual is given in Table 1-1 in Section 1 of this manual.

Table 160-1. Required Test Equipment

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
AC Voltage Source	10.0V +/- 0.01 V	Fluke 5100B
DC Voltage Source	6.2V +/- 155 uV	Fluke 343
Thermocouple/DC Volts Scanner	.....	Fluke 2280A-162 (no substitute)
High Performance A/D Converter	.....	Fluke 2280A-161 (no substitute)

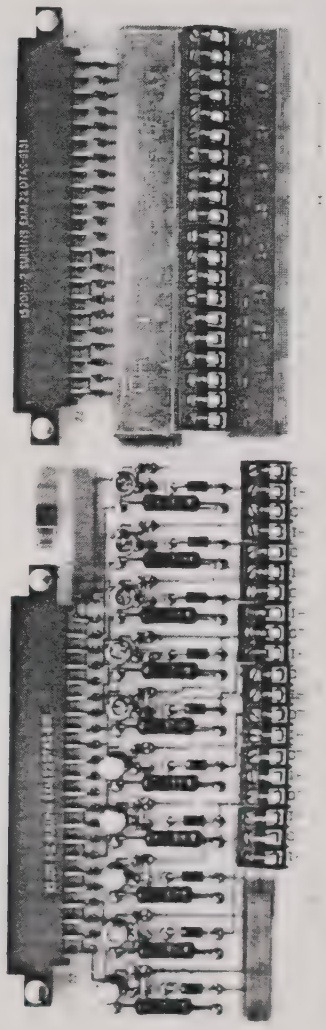


Figure 160-1. AC Voltage Input Connector

THEORY OF OPERATION

The AC Voltage Input Connector theory of operation discussion begins with an overall functional description and follows with a detailed circuit description. The schematic diagram at the end of this option subsection is the quickest reference for the detailed circuit description.

Overall Functional Description

The ac-to-dc conversion circuitry for channels zero through nine consists of a half-wave rectifier, voltage divider and a low-pass filter for each of the ten channels. The converter is average responding and calibrated to indicate the rms value of a sine wave. The conversion process converts a sinusoidal ac voltage to 1/1000 of its rms value minus 0.32 volts.

Detailed Circuit Description

The following description uses the component designations for channel zero although it applies to all channels. Only the component designations change from channel to channel. Diode CR1 rectifies the ac voltage to be measured. This voltage is then divided and filtered by a network consisting of R1, R11, R21 and C1. The dc output voltage equals 1/1000 of the rms value of a sinusoidal input from 45Hz to 450Hz minus 0.32 volts. Overall ripple rejection is from the combination of this low-pass filter and the input filter on the High Performance A/D Converter (Option 2280A-161).

GENERAL MAINTENANCE

The AC Voltage Input Connector PCA normally requires no cleaning unless dirt, dust, or other contamination is visible on the surface. Cleaning instructions are found in Section 4 of this manual.

PERFORMANCE TESTS

To verify that the AC Input Connector is operating properly and within specifications, do the following performance test.

WARNING

THE DATA LOGGER CONTAINS HIGH VOLTAGES WHICH CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE EQUIPMENT. TURN OFF THE DATA LOGGER AND REMOVE ALL POWER SOURCES BEFORE DOING THE FOLLOWING PROCEDURE.

1. Turn the keyswitch to OFF and disconnect the Data Logger power input.

2. Set the address switch on the A/D Converter to 0 (refer to the A/D Converter subsection of the 2280 Series System Guide for switch setting instructions).

3. Install the High Performance A/D Converter (Option 2280A-161) in the top Data Logger option slot, then install the DC Volts Thermocouple

Scanner (Option 2280A-162) in the slot immediately below the A/D Converter.

4. Connect test leads to the HI and LO terminals for channel 0 on the input connector, then install the AC Voltage Input Connector on the Scanner.

5. Reconnect the Data Logger power input (ac line or battery).

6. Turn the keyswitch to the PROGRAM position.

7. Program the Data Logger using the steps given in Table 160-2.

Table 160-2. Performance Test Programming

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>.? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
7	0..19	CHANNEL NUMBER (OR BLOCK) = 0..19
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>?
If you have a 2280B or a 2285B then proceed to step 13.		
10	D	A<D> DC VOLTS/CURRENT
11	ENTER	AD: DC RANGE <1-5>? 1
12	3	AD<3> 512.00 MVDC
Proceed to step 16.		
13	D	A<D> VOLTS/CURRENT
14	ENTER	AD: VOLTS/CURRENT RANGE <1-7>? 6
15	6	AD<6> 250.0 VAC
16	ENTER	AD: CHANNEL MENU CHOICE <1-5>? 1
17	EXIT	A: CHANNEL FUNCTION <A-Z>? D
18	EXIT	CHANNEL NUMBER (OR BLOCK) = C0..19
19	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

8. Connect the ac calibrator output to the HI and LO terminals of the AC Voltage Input Connector. Connect the AC calibrator output to the Hi and Lo test leads of the AC voltage input connector installed on the scanner.

9. Set the calibrator output to 10.00 volts, 60 Hz.

10. Press MONITOR, then 0, then ENTER.

    If you have a 2280B or 2285B, verify that the value displayed for channel 0 is 10.0 +/- 0.2 volts.

    If you have a 2280A, verify that the value displayed for channel 0 is 9.68 +/- 0.2 volts.

    Note

    The 2280A mainframe firmware measures the output of the ac input connector's ac converter using a dc measurement. The firmware does not automatically add in the voltage drop due to the half wave rectifying diode (0.32 volts). This voltage drop can be added back in on the 2280A using a channel expression if desired.

11. Press MONITOR. The Data Logger should display:

    MAIN MENU CHOICE <M FOR MENU>? A

12. Set the calibrator output to zero. Move the AC Voltage Input Connector test leads to the terminals for the next channel to be tested.

13. Repeat steps 9 through 12 for each remaining ac input channel (channels 1-9).

14. The ac portion of the AC Voltage Input Connector performance test is complete.

15. To test the dc voltage input channels (channels 10-19), do the steps for the Option 2280A-176 Voltage Input Connector performance test.

CALIBRATION

The AC Voltage Input Connector requires no calibration.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the AC Voltage Input Connector is given in Table 160-3. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the AC Voltage Input Connector is given in Figure 160-2.

TABLE 160-3. 2280A-160 AC VOLTAGE INPUT CONNECTOR
(SEE FIGURE 160-2.)

REFERENCE DESIGNATOR A->NUMERICS---)	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOT -E
C 1- 10		CAP,AL,47UF,+-20%,10V	613984	89536	613984	10		
CR 1- 10	*	DIODE,SI, 1K PIV, 1.0 AMP	453399	04713	1N4007	10		
H 1		STEEL,CAD.PLATED,.125X .500	276493	89536	276493	4		
H 2		WASHER,FLAT,STEEL,#4,0.030 THK	147728	89536	147728	4		
MP 1		CONNECTOR HOUSING, TOP	578971	89536	578971	1		
MP 2		CONNECTOR HOUSING, BOTTOM	656876	89536	656876	1		
MP 3		DECAL,AC VOLTAGE INPUT CONNECTOR	722975	89536	722975	1		
MP 4		DECAL, OPTION -160	722983	89536	722983	1		
P 36, 37		CONN,PWB EDGE,REC,90,0.156 CTR,44 POS	614313	89536	614313	2		
R 1- 10		RES,MF,1M,+-0.1%,0.5W,25PPM	266114	89536	266114	10		
R 11- 20		RES,MF,150K,+-1%,0.125W,25PPM	257444	89536	257444	10		
R 21- 30		RES,MF,2.26K,+-0.1%,0.125W,25PPM	501320	89536	501320	10		
TB 1		TERM STRIP,PWB,ANGL ENTRY,10 CONTACTS	501403	89536	501403	4	2	

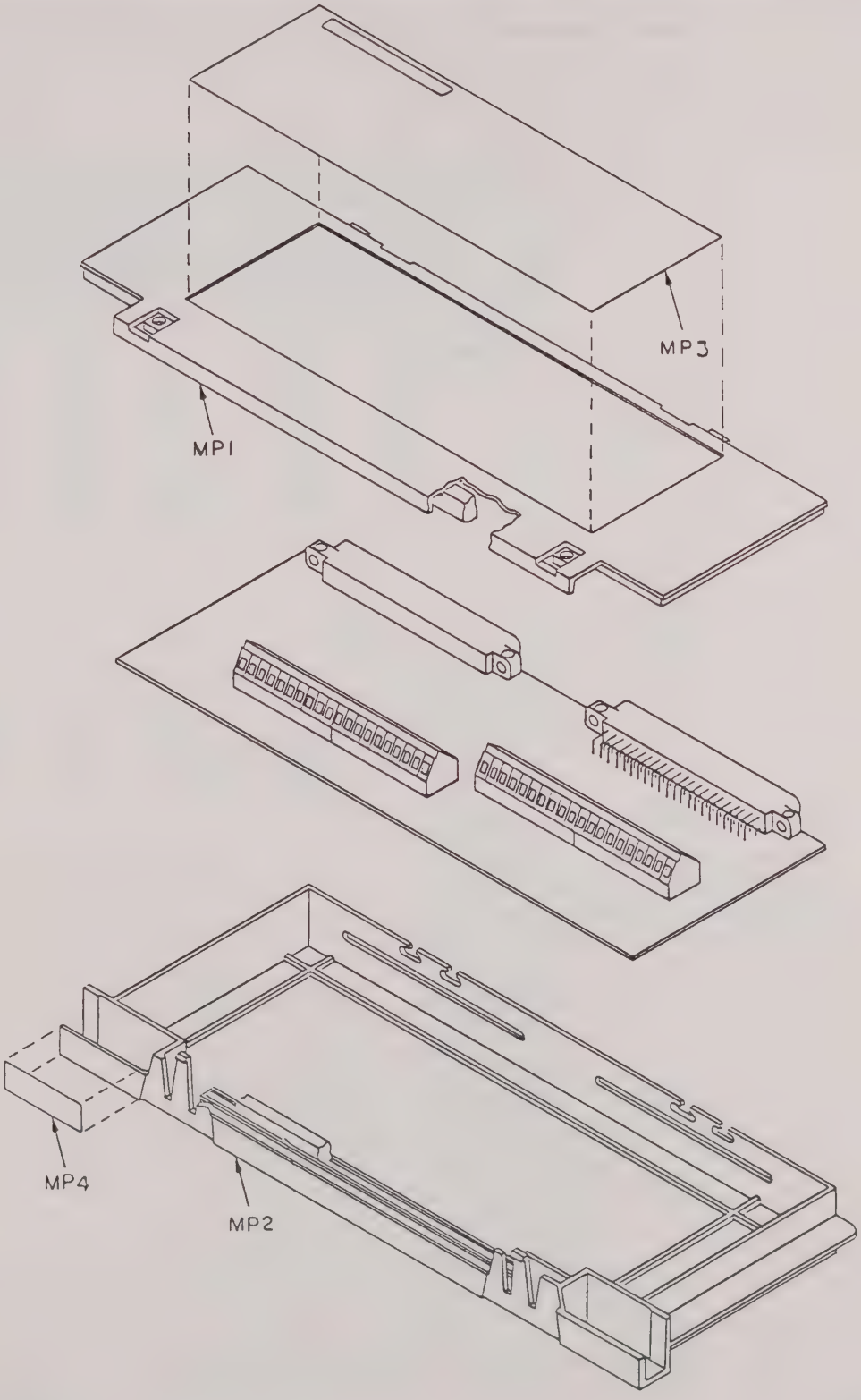
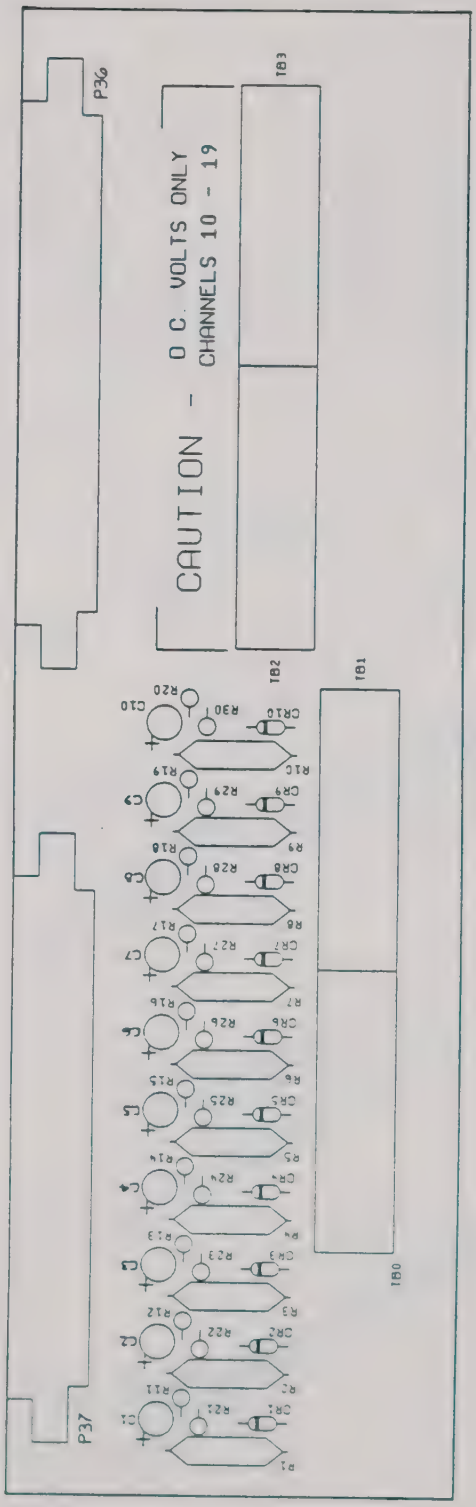


Figure 160-2. 2280A-160 AC Voltage Input Connector



2280A-1660

Figure 160-2. 2280A-160 AC Voltage Input Connector (cont.)

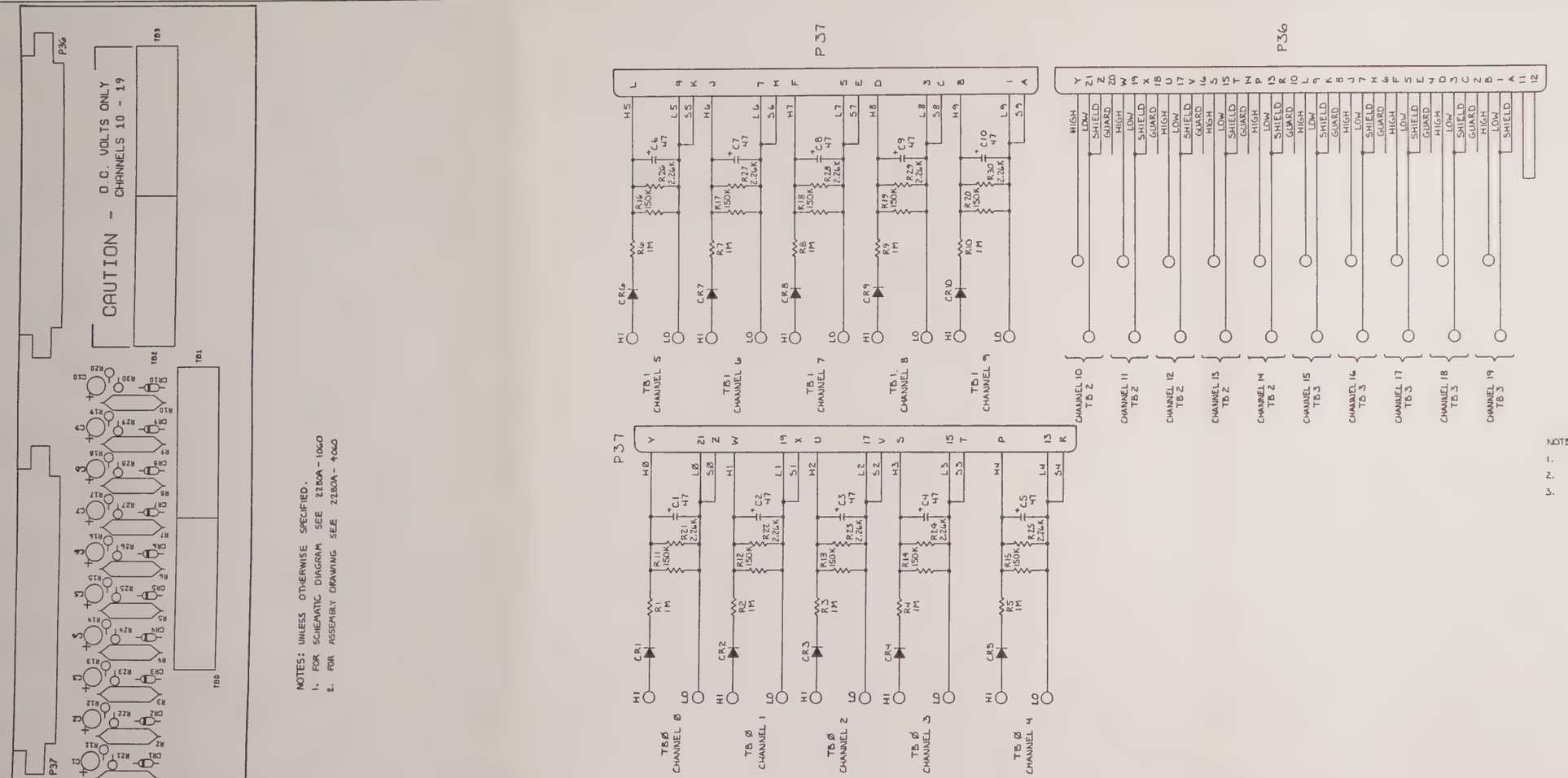


Figure 160-2. AC Voltage Input Connector Schematic Diagram

DESCRIPTION

Option 2280A-161 High Performance A/D Converter is a high-accuracy analog-to-digital converter for measuring scanner input voltages. These dc voltages can represent a variety of phenomena, depending on the input connector and scanner options chosen and installed with the A/D Converter. Figure 161-1 illustrates the A/D Converter.

Operating parameters of the A/D Converter are programmed through the Data Logger front panel keys. With one A/D Converter installed, the Data Logger reads up to 20 input channels per second. If a reading rate higher than 20 channels per second is desired, the rate can be increased by installing one or two additional A/D Converters in the mainframe. Each additional A/D Converter increases the reading rate by varying amounts depending on the system configuration, but reduces the maximum number of mainframe channels by 20 since another slot has been occupied.

Each A/D Converter supports a maximum of five, 20-channel Option 2280A-162 Thermocouple/DC Volts or Option 2280B-163 RTD/Resistance Scanners, thereby providing up to 100 channels. A total of 15 A/D Converters may be installed in a Data Logger system when 2281A Extender Chassis are used. Like the Data Logger mainframe, each 2281A Extender Chassis supports a maximum of 100 channels.

WHERE TO FIND FURTHER INFORMATION

In this subsection, the A/D Converter theory of operation, general maintenance procedures, performance tests, the calibration procedure, the parts list, and a schematic diagram are located. Installation and system configuration instructions can be found in the 2280 Series System Guide, while operating and programming instructions are in the 2280 Series User Guide. Option specifications are located in the Appendices of this manual and the System Guide.

The test equipment required to perform the procedures in this subsection is listed in Table 161-1. A summary of test equipment required to perform all procedures in this manual is given in Table 1-1 in Section 1 of this manual.

THEORY OF OPERATION

The A/D Converter theory of operation discussion begins with an overall functional description of the A/D Converter. A block diagram analysis then describes how each major circuit block on the A/D Converter assembly works. Circuit analysis of each block described in the block diagram analysis ends the theory of operation discussion. Where necessary, block diagrams and simplified schematics are included with the text. The schematic diagrams for the A/D Converter are located at the end of this option subsection.

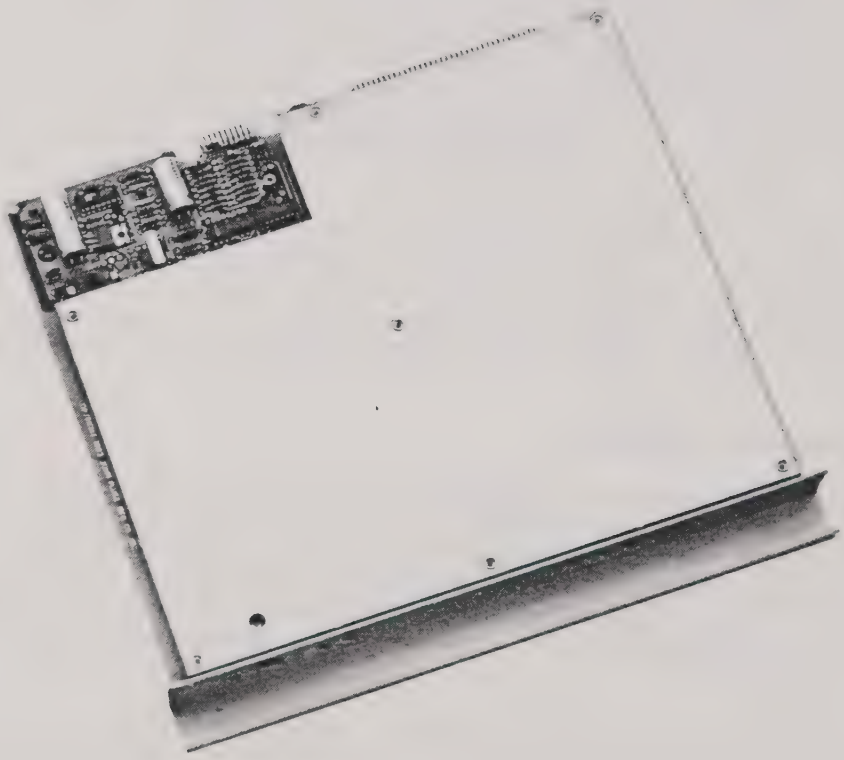


Figure 161-1. A/D Converter

Table 161-1. Required Test Equipment

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
DC Calibrator	+/- 31.3 mV +/- 20 uV +2.048V +/- 50 uV -2.048V +/- 2 uV of +2.048 500 mV +/- 20 uV 6.2V +/- 155 uV 6.8V +/- 0.1V 5.0V +/- 100 uV 7.9V +/- 200 uV *63V +/- 800 uV 1.008V +/- 40 uV	Fluke 343 *63V output used only for one optional test.
100:1 Divider	+/- 0.005%	Fluke Y2022
Digital Multimeter	+/- 10V +/- 0.06V 50.0mV +/- 0.001mV 500.0mV +/- 0.005mV	Fluke 8505A
Resistor	1 kohm +/- 5%	Fluke Part Number (108597)
Resistor	10 kohm +/- 5%	Fluke Part Number (109165)
Thermocouple/DC Volts Scanner	.....	Fluke 2280A-162 (no substitute)
Isothermal Input Connector	.....	Fluke 2280A-175 (no substitute)
Voltage Input Connector	.....	Fluke 2280A-176 (no substitute)
Calibration Fixture Assy	.....	Fluke Y2056

Overall Functional Description

The High Performance A/D Converter measures dc voltages received from scanner option channels, when commanded, and sends the measurement results to the Data Logger controller in digital form over a the serial link bus. At least one scanner and input connector option must be used with the A/D Converter if the Data Logger is to acquire measurement data.

Block Diagram Analysis

Figure 161-2 illustrates the A/D Converter in block diagram form. The following paragraphs discuss the function of each of the blocks in the diagram.

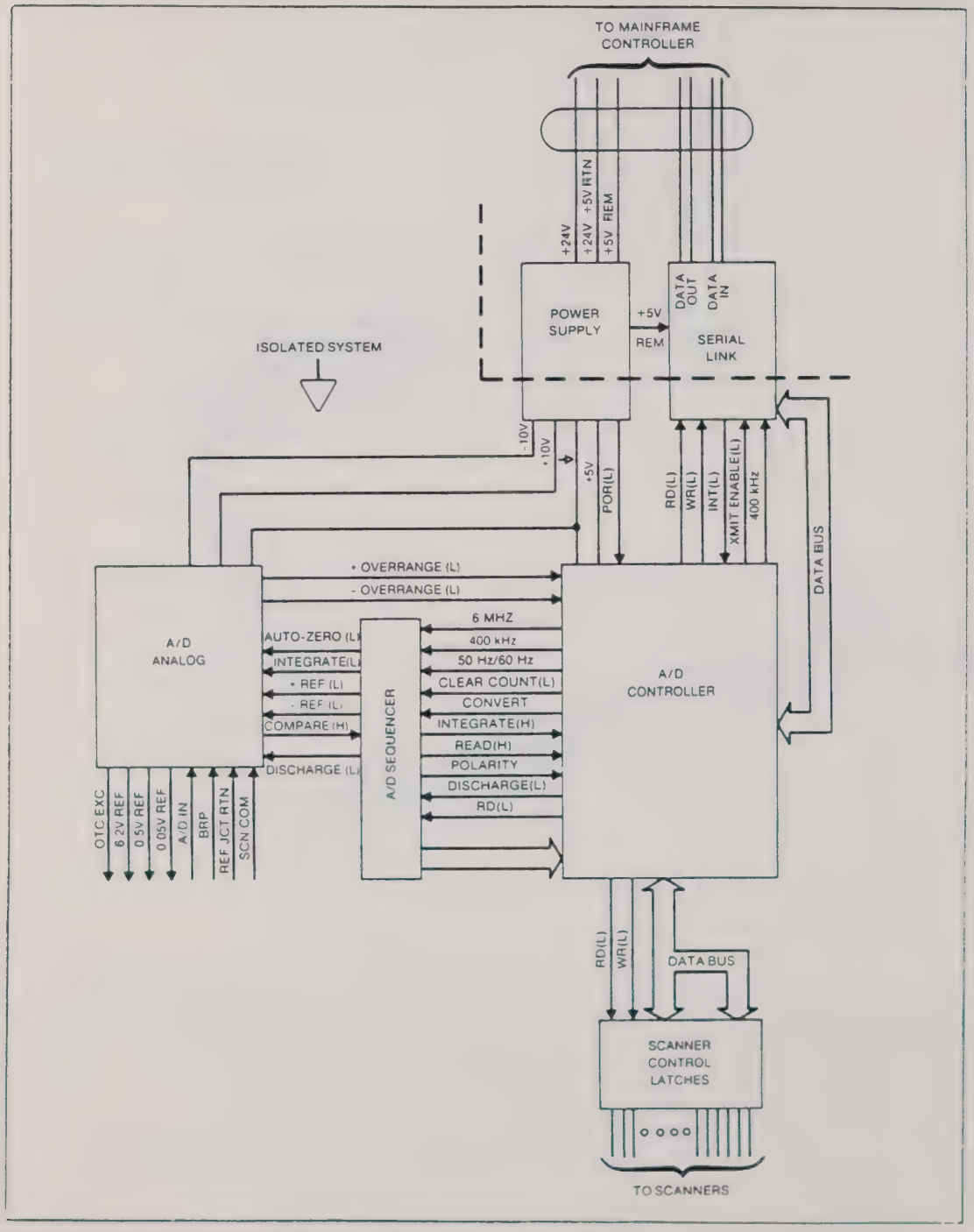


Figure 161-2. A/D Converter Block Diagram

POWER SUPPLY

The Power Supply converts incoming dc power from the serial link into isolated +10V, -10V, and +5V dc for the scanners and the measurement circuitry as well as +5V dc for the serial link. The Power Supply transmits a reset signal to the A/D Controller upon power-up. Reference voltages produced by the A/D Analog block are used by the Power Supply to regulate the +10 and -10 output voltages.

SERIAL LINK

The Serial Link allows the A/D Controller to exchange commands and measurement data with the Data Logger mainframe controller. In this block, the bi-directional serial transmissions are electrically isolated, buffered, and converted to signals that the A/D controller can use. The serial link circuitry sends an interrupt signal and data to the controller while the controller returns data and a transmitter enable signal.

A/D CONTROLLER

The A/D Controller performs the tasks of maintaining the communication link, selecting scanner modes and channels, and invoking A/D conversions. The controller supplies 6 MHz and 400 kHz clocks, line frequency data, and conversion commands to the A/D Sequencer and in return, it monitors the progress of conversions through the incoming integrate, read, and polarity lines. The controller is advised of impending overrange measurements by two additional lines that come from the A/D Analog block. By writing into the Scanner Control Latches the controller manipulates many control lines that direct the scanners.

A/D SEQUENCER

The A/D Sequencer responds to a conversion command from the controller and generates the timed control signals that the A/D Analog section needs to perform a dual-slope analog-to-digital conversion. The read interval of the conversion cycle is timed by this block.

A/D ANALOG

The A/D Analog section accepts dc input voltages from the scanners and converts these inputs to a time interval that is proportional to their magnitude. Here, stable reference voltages are also generated for the Power Supply section and the scanners.

SCANNER CONTROL LATCHES

The scanner control latches are controlled by the A/D Controller, thereby enabling readings on the individual scanner channels.

Detailed Circuit Description

POWER SUPPLY

DC-DC Converter

Isolation of the A/D circuitry is provided by T1 which is also the core of the dc-dc converter, where T1, U1, U34, U49, Q1, and Q2 comprise a "flyback" type of switching regulator converter. Incoming dc power is applied to the primary of T1 for an interval generated by U1, causing the primary current to ramp up to approximately 1 ampere peak before Q1 and Q2 are turned off. The energy stored in T1 is then released through CR10, CR11, CR12, and CR13 into C5, C17, C18, and C19. The 5.4 volt nominal voltage on C18 is sampled by R82 and R11 and a feedback error signal is generated by U49, which is relayed to U1 through isolator U34. The duty cycle of Q1 and Q2 is then adjusted by U1 to maintain C18 at 5.4V despite load changes and variations in the serial link supply voltage. Typical waveforms are shown in Figure 161-3.

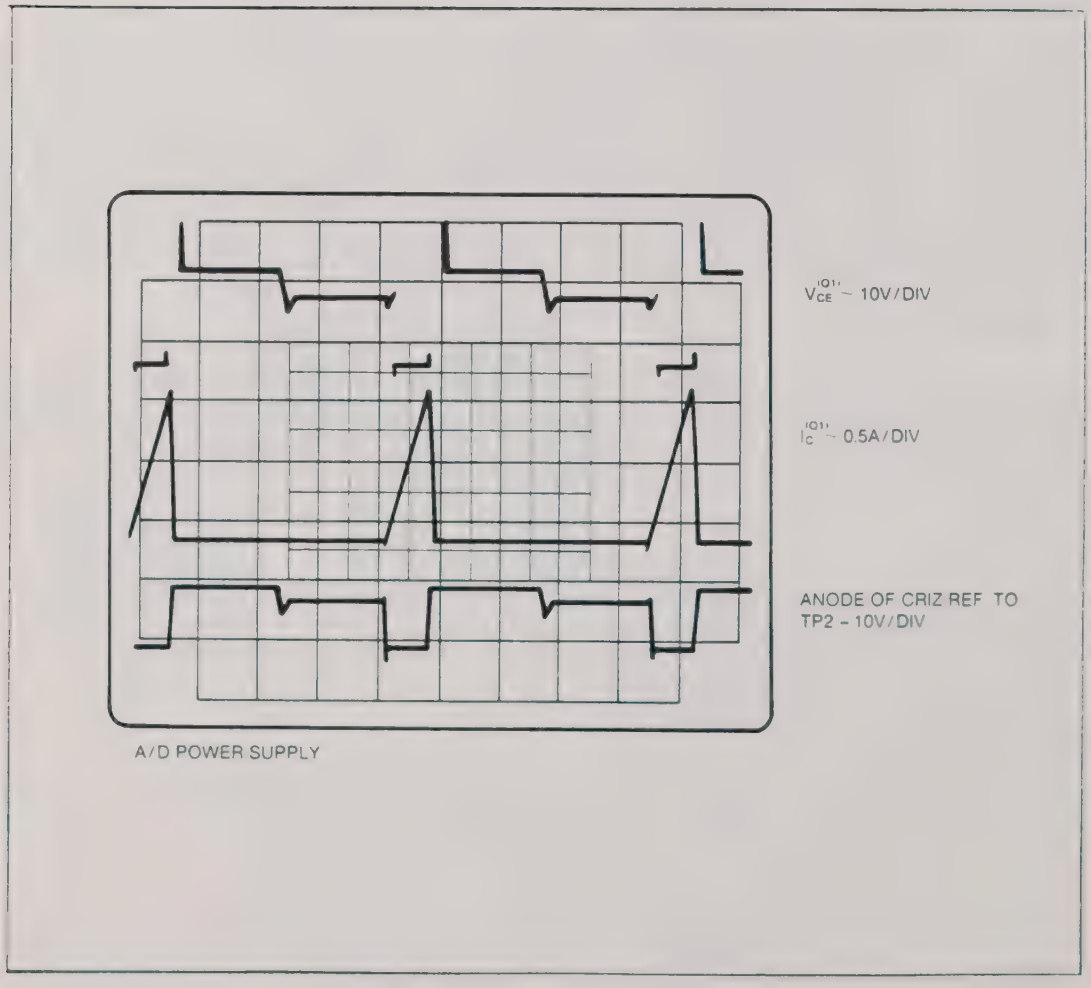


Figure 161-3. DC-DC Converter Typical Waveforms

The voltage on C17, C18 and C19 is regulated further by U33, U49, Q5, Q9, Q10, Q11, Q24, and Q25 to obtain precise +10V, -10V, and +5V dc voltages to power the A/D Converter and scanners. The +10V supply is referenced to zener diode VR5 within the A/D analog section. The -10V supply is referenced to the +10V supply. The +5V supply is derived from U35, a 2.5V reference, which is also the reference for the switching regulator loop.

The voltage on C5 (5V nominal) is used to power the serial link interface circuits and is only regulated by its coupling to the switching regulator loop through T1.

Reset Generator

When power is first applied to the A/D, Q6 is turned on by R53, and the Power-On Reset Line to the controller is held low. U15 compares the voltage on C46 to a 1.22V reference to determine whether the +5V supply is within tolerance. Once the supply voltage has stabilized, C46 is allowed to charge through R48 and R56, generating a delay of approximately 50 ms before C46 charges to 1.22V causing U15 to remove the drive to Q6, and allowing the Power-On Reset line to be pulled high by R51. At this point Q7 is turned on to light the POWER indicator DS1. For test purposes, this reset sequence can be triggered by momentarily grounding Test Point 44 to TP 2.

SERIAL LINK

Differential line drivers U2 and receiver U3 transmit and receive information through transient suppression networks consisting of resistors R12, R13, R14, R15, R18, R19, R20 and R21 and diodes CR1 through CR8 in conjunction with VR2.

Incoming data from the 2280 mainframe controller assembly, which can be monitored at Test Point 30, is fed into UART U17 through optocoupler U5. Upon receipt of a data byte, U17 interrupts microprocessor U10 in the A/D Controller section.

Data destined for the mainframe controller from the A/D is clocked out of the UART through isolator U4 to the line drivers in U2. This data to be transmitted can be observed at Test Point 32. The drivers are enabled by a Xmit Enable signal from the A/D controller that must also pass through U4. The driver outputs remain in a high-impedance state when not enabled.

A/D CONTROLLER

The A/D Control circuitry consists of an 8 bit microprocessor, U10, that executes firmware stored in a PROM, U26. The lower eight bits of the PROM address is captured in an octal latch, U36, on the rising edge of the address latch enable (ALE(L)) signal from the microprocessor. The clock for the microprocessor is derived from a 6.0 MHz crystal, Y1, in conjunction with U18.

U27 and U28 are CMOS RAM's that are used to store the calibration constants of the scanners associated with the A/D. Data is read from or written to the RAMs by the microprocessor by using the RD(L), WR(L), and P1-1 (pin 28 of U10).

A/D SEQUENCER

The A/D Sequencer consists of three functional blocks: the Integrate Timer, the Read Timer, and the Autozero flip-flop. The integrate timer generates the integrate control signal of 16.666 or 20.000 ms duration. The read timer asserts the appropriate polarity reference signal and measures the interval it is applied. The autozero flip-flop places the converter into the autozero mode when not performing a conversion.

- Integrate Timer

  Refer to Figure 161-4 for a simplified schematic and timing diagram of the integrate timer. In response to a convert command from the A/D controller, J-K flip flops U31 and U23 are reset and counters U21 and U22 are loaded. The next ALE pulse sets U23, asserting the INTG(L) signal. Subsequent ALE pulses decrement the counters until both reach zero causing U13 to output a timeout signal.
  The next ALE pulse toggles U23 to terminate the INTG(L) signal and sets U31 to prevent spurious integrate commands.

- Read Timer

  Refer to Figure 161-5 for a simplified schematic and timing diagram of the read timer. The timeout signal from the integrate timer latches the state of the COMP(H) into U12. U12 selects which reference control line (+REF or -REF) is to be asserted during the read interval. The timeout signal is gated through U40 and U13 to U23 allowing the same ALE pulse that terminates the integrate signal to set U23 and commence the read interval. The READ(H) signal (TP 34) enables U19 and U30 to count the 6 MHz system clock and thereby measure the duration of the read period. U13 and U18 detect the eventual change in comparator state and reset U23 when COMP(H) changes, ending the read interval. U32 and U20 prevent switching glitches from appearing as a comparator transition signal by preventing U23 form being reset until 20 microseconds into the read period. The eventual reset to U23 by COMP also resets U31, inhibiting read timer activity until a subsequent integrate cycle is initiated.

- Autozero Flip-flop

  When the conversion cycle ends, U12 is clocked, and the Auto-Zero control signal, AZ(L), is asserted low. The system remains in this state until another integrate cycle is entered when the integrate signal resets the autozero flip-flop causing AZ(L) to go high.

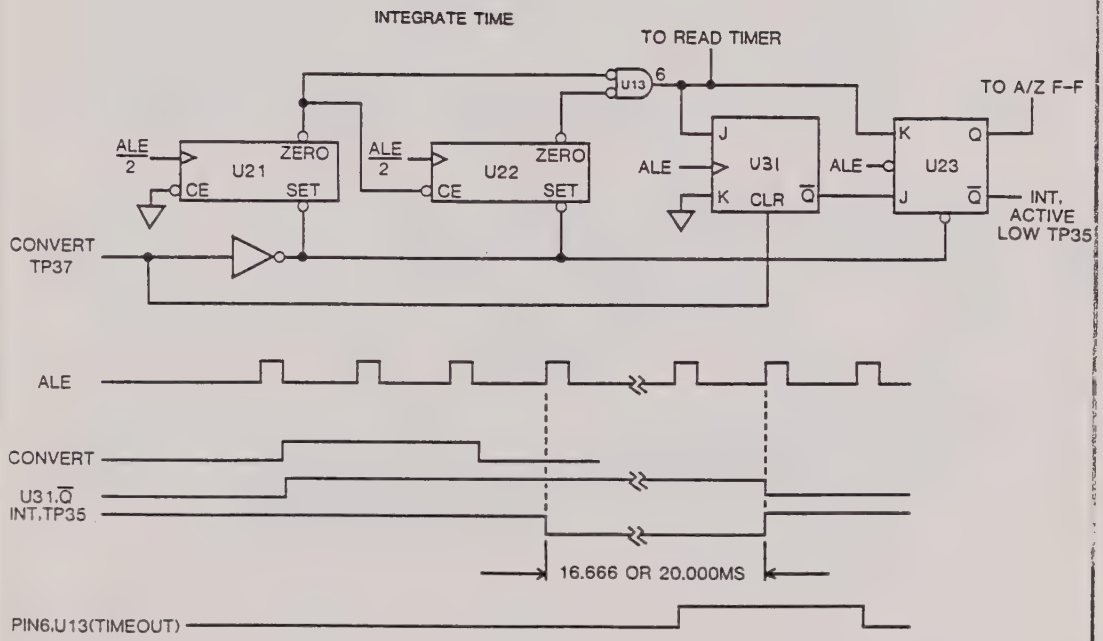


Figure 161-4. Integrate Timer Simplified Schematic and Timing Diagram

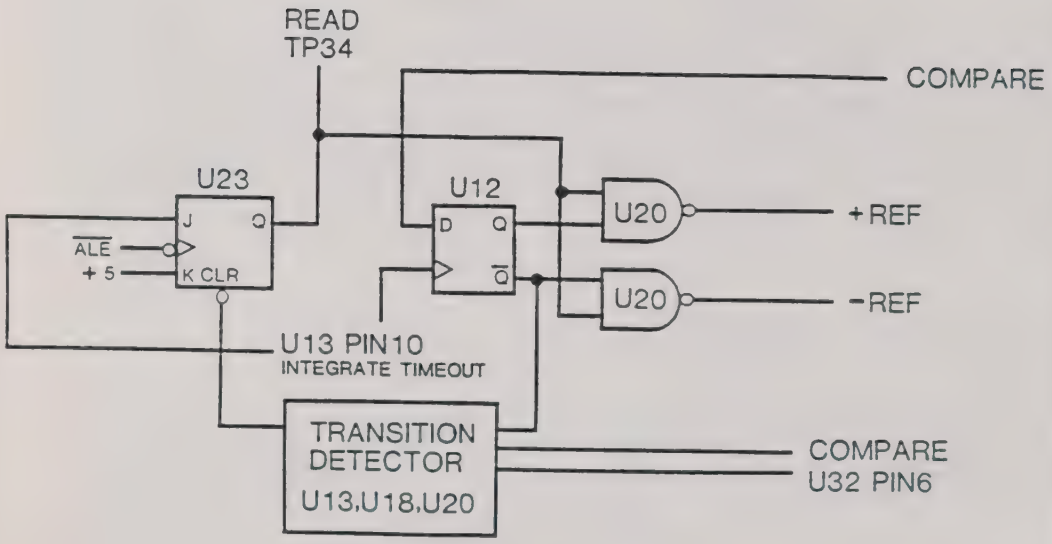


Figure 161-5. Read Timer Simplified Schematic and Timing Diagram

Figure 161-6 shows the major components of the dual-slope converter that dominates this circuit block as well as the timing relationships of the control signals and the circuit waveforms as they appear during typical conversion cycles.

A conversion cycle begins with integrate when Q20 turns on and applies the scanner output voltage to the amplifier consisting of Q16 and U44. The amplifier output is integrated by the stage composed of Q13, U43, R77, and C38 as long as integrate signal is asserted. The intergration of the dc input appears as a ramp waveform that can be observed at Test Point 48.

At the end of the integrate period Q20 is turned off and either Q17 or Q18 is turned on. This applies a stable reference voltage to the integrator with a polarity opposite to the input previously integrated. The integrator in turn ramps back toward zero. The integrator output is amplified by a stage consisting of U43, R87, and R90 before reaching the comparator U42. The amplifier increases the slope of the integrator ramp that is applied to the comparator to facilitate an accurate zero crossing detection by the comparator.

Once the comparator changes state, the reference is removed from the integrator by turning off Q17 or Q18 and turning on Q19, Q12, and Q14 and placing the converter in the autozero mode. During autozero, amplifier offsets are stored on C37 for use in negating the integrate and read errors that would otherwise occur.

Offscale or overvoltage inputs are detected by comparator U47. Should an out-of-range voltage appear at the A/D input, Q21 is turned on to ensure that the input filter capacitor C59 is not adversely effected. At the same time, an overload bit is pulled low to flag the A/D controller so that a measurement will not be made.

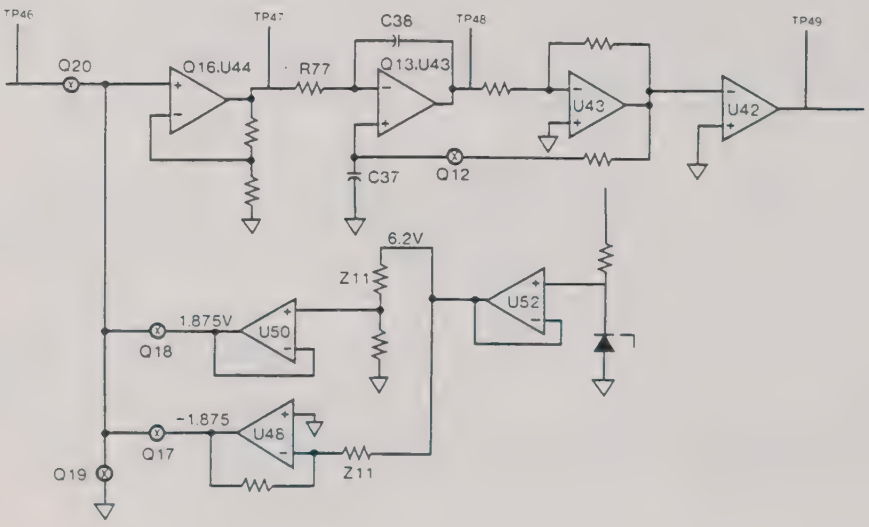


Figure 161-6. A/D Dual-Slope Converter

SCANNER CONTROL LATCHES

The A/D generates 21 control signals to select measurement channels and ranges on the connected scanners. The binary representations of the scanner address and channel address to be measured are latched into U6 and U7 by U10 and U37. The scanner address is further decoded by U11 into one of five scanner select lines SCNS[1:5](H) and a sixth signal that is used by the A/D ANALOG block to discharge its input filter DISCHG(H).

U9 and U14 accept the binary representations of the ranging bits RNG0(L) and RNG1(L) in addition to the bits that determine the scanner mode: Zero (ZERO(H)), calibrate (CAL(H)), discharge inhibit (DISCHG INH(H)), and reference junction enable (REF JCT EN(H)). U14 also stores the line frequency bit that determines the integration period of the Intergrate Timer.

U8 gates the scanner type bits SCN[0:2](H) onto the data bus. U25 gates the setting of the A/D Address switch S1 onto the bus as well as the status of the RDY(H) line that is returned from the scanners.

A/D Operation

The A/D Converter does not initiate tasks independently, but responds to commands from the Data Logger mainframe controller. Six commands direct the A/D through all of the jobs demanded of it. The commands are:

- Reset Command

  This initializes the A/D Controller and its RAM. The reset command elicits no response from the A/D.

- Configuration Request

  The A/D responds to this command by sending the type identifier of each associated scanner. One type identifier is sent for each block or decade of channels. Thus, an A/D with three adjoining DC Volts Scanners would respond with six different block addresses during a system-wide configuration check.

- Calibrate Command

  The A/D measures the offsets and gains of each range of the DC Volts and RTD/Ohms Scanner connected to it. From these measurements the A/D computes and stores correction constants for use in adjusting subsequent measurements. The calibrate command contains line frequency information that the A/D uses to determine the integration period. Calibration is commanded on approximately ten-minute intervals and at power-on. The A/D does not send a response to the calibration command.

- Measurement Command

  The A/D performs measurements on desired scanner channels in the ranges identified within the command. Normally the A/D responds to a measurement request with an acknowledgement that the command was

understood. If the A/D is in an uncalibrated state, as might happen if serial link power had been interrupted, the A/D does not send a response.

- Status Request

  The A/D responds to this command with a Ready or a Not Ready response indicating whether or not it has completed the measurement task previously commanded.

- Measurement Results Request

  The A/D responds by sending back the results of the measurements most recently performed. If the A/D does not have readings to transmit due to a unusual circumstances then it does not send a response.

GENERAL MAINTENANCE

The Option 2280A-161 PCA normally does not require cleaning, unless dirt, dust, or other contamination is visible on the surface. Follow PCA cleaning instructions in Section 4 of this manual.

PERFORMANCE TESTS

There are four performance tests for the 2280A-161 A/D Converter. All four tests may be performed in sequence to verify overall operation of the A/D Converter, or the tests may be run independently. The four tests are:

- Address Response Test

  This test checks to see if the Data Logger mainframe controller can communicate properly with the A/D Converter address switch set to a variety of positions that exercise all address switch lines.

- Accuracy Verification Test

  The accuracy verification test checks the A/D Converter to see if its voltage measurement accuracy is within specifications.

- Overrange Indication Test

  This test determines if the A/D Converter can detect and communicate to the mainframe controller an overrange condition on a channel.

- Open Thermocouple Response Test

  The open thermocouple response test determines if the A/D Converter can detect and communicate to the mainframe controller an open thermocouple condition on a channel. The open thermocouple response test is also part of the performance test for the Thermocouple/DC Volts Scanner (Option 2280A-162). The test is repeated there because each assembly contains part of the circuitry that checks for an open thermocouple. If both the A/D Converter and the Thermocouple/DC Volts Scanner are being tested, the open thermocouple test need only be performed once.

The performance tests verify that the A/D Converter performs properly and meets all specified accuracy tolerances. If it is determined that calibration of the assembly is required, refer to the Calibration section that immediately follows the performance tests in this subsection.

Address Response Performance Test

WARNING

THE DATA LOGGER CONTAINS HIGH VOLTAGES WHICH CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE EQUIPMENT. TURN OFF THE DATA LOGGER AND REMOVE ALL POWER SOURCES BEFORE DOING THE FOLLOWING PROCEDURE.

1. Turn the 2280 keyswitch OFF. Disconnect the line power cord or dc input power and all other high voltage inputs.

2. Install the A/D Converter in the top option slot of the Data Logger and install a scanner in the slot just below the A/D Converter.

3. Connect a pair of test leads to the HI and LO terminals of channel 0 on the Voltage Input Connector (option 2280A-176) or the Isothermal Input Connector (option 2280A-175). Install the input connector on the scanner.

4. Reconnect line or battery power to the Data Logger

5. Turn the keyswitch to PROGRAM.

6. Set the output of the calibrator to 7.9V, and then connect the output of the calibrator to the test leads coming from the input connector mounted on the scanner.

7. Program the Data Logger to measure channels 0 through 1499 on the 8.0000 VDC range using the steps given in Table 161-2.

8. Turn the keyswitch to OFF, remove the A/D Converter from the chassis, and set the A/D address switch to address 0 as shown in Figure 161-7.

9. Reinstall the A/D Converter, and turn the keyswitch to RUN.

10. Press MONITOR, then 0 for channel 0, and then ENTER. The Data Logger should display a measurement value of 7.9000V within a tolerance of +/- 0.001V.

11. Repeat steps 8, 9, and 10 for channel 100 (A/D address 1), 200 (A/D address 2), 400 (A/D address 4), 800 (A/D address 8), and 1400 (A/D address 14). The measurement on each channel should be 7.9000V within a tolerance of +/- 0.001V.

12. The address response test is complete. Continue with the accuracy verification test if you are performing a complete verification test of the High Performance A/D Converter (option 2280A-161).

Table 161-2. Address Response Test Programming Steps

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = CO
7	0..1499	CHANNEL NUMBER (OR BLOCK) = 0..1499
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
10	D	A<D> DC VOLTS/CURRENT
11	ENTER	AD: DC RANGE <1-5>? 1
12	2	AD<2> 8.0000 VDC
13	ENTER	AD: CHANNEL MENU CHOICE <1-5>? 1
14	EXIT	A: CHANNEL FUNCTION <A-Z>? D
15	EXIT	CHANNEL NUMBER (OR BLOCK) = CO..1499
16	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

NOT AVAILABLE AT THIS PRINTING

Figure 161-7. A/D Address Switch Settings

WARNING

THE DATA LOGGER CONTAINS HIGH VOLTAGES WHICH CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE EQUIPMENT. TURN OFF THE DATA LOGGER AND REMOVE ALL POWER SOURCES BEFORE DOING THE FOLLOWING PROCEDURE.

1. Disconnect the Data Logger line power cord and all other high voltage inputs.

2. Set the A/D Converter address switch to 0, and then install the A/D Converter in the top option slot of the Data Logger. Install a scanner in the slot just below the A/D Converter.

3. Connect a pair of test leads to the HI and LO terminals of channel 0 on the Voltage Input Connector (option 2280A-176) or the Isothermal Input Connector (option 2280A-175). Install the input connector on the scanner.

4. Reconnect line or battery power to the Data Logger.

5. Set the calibrator to output 6.2V. Connect the calibrator output to the input of the 100:1 Divider. Connect the output of the divider to the test leads coming from the connector installed on the scanner.

6. Turn the keyswitch to PROGRAM.

7. Program the Data Logger to measure channel 0 on the 64.000mV range using the steps given in Table 161-3.

Table 161-3. Accuracy Verification Test Program

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
7	0	CHANNEL NUMBER (OR BLOCK) = 0
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
10	D	A<D> DC VOLTS/CURRENT
11	ENTER	AD: DC CHANNEL RANGE <1-5>? 1
12	4	AD<4> 64.000 MVDC
13	ENTER	CHANNEL MENU CHOICE <1-5>?
14	EXIT	A: CHANNEL FUNCTION <A-Z>? D
15	EXIT	CHANNEL NUMBER (OR BLOCK) = C0
16	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

8. Press MONITOR, then 0 for channel 0, and then ENTER. The Data Logger should display a measurement of 62.000mV within a tolerance of +/- 0.010mV.

9. Press MONITOR again. The Data Logger should display:

   MAIN MENU CHOICE <M FOR MENU>? A

10. To test the 512mV A/D range, program the Data Logger to measure channel 0 on the 512.00mV range using the steps given in Table 161-4.

Table 161-4. 512 mV A/D Range Test Programming Steps

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
3	0	CHANNEL NUMBER (OR BLOCK) = 0
4	ENTER	PROGRAM COPY DELETE OR LIST <P,D,C,L>? P
5	ENTER	A: CHANNEL FUNCTION <A-Z>? D
6	ENTER	AD: DC RANGE <1-5>? 4
7	3	AD<3> 512.00 MVDC
8	ENTER	AD: CHANNEL MENU CHOICE <1-5>? 1
9	EXIT	A: CHANNEL FUNCTION <A-Z>? D
10	EXIT	CHANNEL NUMBER (OR BLOCK) = C0
11	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

11. Change the calibrator output to 500mV.

12. Remove the 100:1 divider and connect the calibrator output directly to the input connector terminals.

13. Press MONITOR, then 0, then ENTER. Verify that the displayed value is 500.00mV within a tolerance of +/- 0.1mV.

14. Press MONITOR again. The Data Logger should display:

    MAIN MENU CHOICE <M FOR MENU>? A

15. Re-enter the keystrokes listed in Table 161-4, except at step 7. At step 7, enter a 2 instead of a 3 to obtain the prompt AD<2> 8.0000 VDC and then press ENTER. This programs the instrument to measure channel 0 on the 8.0000VDC range.

16. Change the calibrator output to 7.9V.

17. Press MONITOR, then 0, then ENTER. Verify that the displayed value is 7.9000V +/- 0.001V.

18. Press MONITOR again. The Data Logger should display:

    MAIN MENU CHOICE <M FOR MENU>? A

19. Re-enter the keystrokes listed in Table 161-4, except at step 7. At step 7, enter a 1 instead of a 3 to obtain the prompt AD<1> 64.000 VDC and then press <ENTER>. This programs the instrument to measure channel 0 on the 64.000VDC range.

20. Change the calibrator output to 63V.

21. Press MONITOR, then 0, then ENTER and verify that the displayed value is 63.000V within a tolerance of +/- 0.020V.

22. Press MONITOR again. The Data Logger should display:

    MAIN MENU CHOICE <M FOR MENU>? A

23. The accuracy verification test is complete. Continue with the overrange indication test if you are performing a complete verification test of the Data Logger.

Overrange Indication Test

1. Turn the keyswitch to the OFF position. Disconnect the Data Logger line power cord and all other high voltage inputs.

2. Set the A/D Converter address switch to 0, and then install the A/D Converter in the uppermost option slot of the Data Logger. Install a scanner in the slot just below the A/D Converter.

3. Connect a pair of test leads to the HI and LO terminals of channel 0 on the Voltage Input Connector (option 2280A-176) or the Isothermal Input Connector (option 2280A-175). Install the input connector on the scanner.

4. Reconnect line or battery power to the Data Logger.

5. Turn the Data Logger keyswitch to the PROGRAM position.

6. Program the Data Logger to measure channel 0 on the 64.000mVDC range using the steps given in Table 161-5.

7. Connect the calibrator output to the 100:1 divider input, and connect the divider output to the leads coming from the input connector mounted on the scanner.

8. Set the calibrator output to 6.8V.

9. Press MONITOR, then 0, then ENTER. Verify that the Data Logger displays:

    C 0 OVER RANGE

Table 161-5. Overrange Indication Programming Steps

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = CO
7	0	CHANNEL NUMBER (OR BLOCK) = 0
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
10	D	A<D> DC VOLTS/CURRENT
11	ENTER	AD: DC RANGE <1-5>? 1
12	4	AD<4> 64.000 MVDC
13	ENTER	CHANNEL MENU CHOICE <1-5>? 1
14	EXIT	A: CHANNEL FUNCTION <A-Z>? D
15	EXIT	CHANNEL NUMBER (OR BLOCK) = CO
16	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

10. Press MONITOR again. The Data Logger should display:

    MAIN MENU CHOICE <M FOR MENU>? A

11. The overrange indication test is complete. Continue with the open thermocouple response test if you are performing a complete performance verification of the Data Logger.

Open Thermocouple Response Test

1. Disconnect the Data Logger line and dc power and all other high voltage inputs.

2. Set the A/D Converter address switch to 0, then install the A/D Converter in the uppermost option slot of the Data Logger, and install a scanner in the slot just below the A/D Converter.

3. Connect a pair of test leads to the HI and LO terminals for channel 0 on the Isothermal Input Connector (option 2280A-175), then install the connector on the scanner.

4. Reconnect line or battery power to the Data Logger.

5. Turn the keyswitch to the PROGRAM position.

6. Connect the leads from the isothermal input connector to a 1 kohm resistor.

7. Program the Data Logger to measure channel 0 as if a thermocouple were connected using the steps given in Table 161-6.

Table 161-6. Open Thermocouple Response Test Programming Steps

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
7	0	CHANNEL NUMBER (OR BLOCK) = 0
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
10	T	C<T> THERMOCOUPLE
11	ENTER	AT: TC TYPE <J,K,T,E,R,S,B,N,C,H,V>? J
12	ENTER	AT: CHANNEL MENU CHOICE <1-5>? 1
13	EXIT	A: CHANNEL FUNCTION <A-Z>? T
14	EXIT	CHANNEL NUMBER (OR BLOCK) = C0
15	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

8. Press MONITOR, then 0, then ENTER. Verify that the unit displays a measurement value equal to the ambient temperature +/-2 degrees C and not an OPEN TC message.

9. Press MONITOR again. The Data Logger should display:

   MAIN MENU CHOICE <M FOR MENU>? A

10. Replace the 1 kohm resistor connected to the isothermal input connector with a 10 kohm resistor to simulate a high resistance or open thermocouple.

11. Press MONITOR, then 0, and then ENTER. Verify that the unit displays:

    C0 OPEN TC

12. Press MONITOR again. The Data Logger should display:

    MAIN MENU CHOICE <M FOR MENU>? A

13. Disconnect the 10 kohm resistor and the test leads from the input connector. Performance testing is complete.

CALIBRATION

The calibration sequence for the 2280A-161 High Performance A/D Converter is provided in this section. The results of the accuracy verification test in the performance test section will indicate whether calibration of the A/D Converter is required. Perform the calibration only if it is required.

A/D calibration involves two main steps: first the power supply voltages are verified to be within specifications, then the zero, full-scale and reference for the A/D Converter are calibrated. The following steps must be performed in the order given.

Power Supply Verification Procedure

1. Disconnect the Data Logger power input and all other high voltage inputs.

2. Install the A/D Converter in the second slot up from the bottom of the Data Logger, leaving one slot open below it.

3. Install the Calibration Fixture/Extender (Fluke Accessory Y2056) in the bottom slot, just below the A/D Converter. Set the slide switch on the calibration fixture to the CAL position.

   Note

   Do not install a scanner at this time.

4. Reconnect the Data Logger ac line or battery power input.

5. Turn the keyswitch to RUN.

6. Set the DMM to read +5V with 1mV resolution.

7. Connect the DMM to the +5V and LOGIC COMMON test points on the calibration fixture, observing correct polarity.

8. Verify a DMM reading of +5.000V +/- 0.125V.

9. Set the DMM to read 10V with 1mV resolution. Move the DMM positive lead to the +10V test point on the calibration fixture.

10. Verify a DMM reading of +10.000V +/- 0.080mV.

11. Move the DMM positive lead to the -10V test point on the calibration fixture.

12. Verify a DMM reading of -10.000V +/- 0.080V.

13. This completes the power supply verification test. If all voltages are within tolerance, proceed to Zero, Full-Scale, and Reference Calibration below. If the power supply voltages are not within the stated tolerances, the A/D Converter must be repaired.

Zero, Full-Scale, and Reference Calibration

1. Disconnect the Data Logger power input and all high voltage inputs.

2. Remove the A/D Converter, set the address switch to 0, and reinstall the A/D Converter.

3. Reconnect the Data Logger ac line or battery power input.

4. Turn the keyswitch to PROGRAM. Note: Allow the temperature on the A/D Converter to stabilize for at least 30 minutes.

5. Program the Data Logger using the steps given in Table 161-7.

Table 161-7. Zero, Full-Scale, and Reference Programming Steps

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
7	0	CHANNEL NUMBER (OR BLOCK) = 0
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
If your instrument is a 2280B or a 2285B then proceed with step 10b.		
10a	A	A<A> AC VOLTS
11a	ENTER	AA: AC RANGE <1,2> 1
Proceed with step 12.		
10b	A	A<A> A/D CALIBRATION
11b	ENTER	AA: VOLTS RANGE <1,2> 1
12	ENTER	AA: CHANNEL MENU CHOICE <1-5>?
13	3	AA<3> CHANNEL EXPRESSION
14	ENTER	CX=
15	CX*512	CX= CX*512
16	ENTER	AA: CHANNEL MENU CHOICE <1-5>? 4
17	5	AA<5> LOGGING FORMAT
18	ENTER	AA5: LOGGING FORMAT <1-7>? 1
19	7	AA5<7> NNNNN
20	ENTER	AA: CHANNEL MENU CHOICE <1-5>?
21	EXIT	A: CHANNEL FUNCTION <A-Z>? A
22	EXIT	CHANNEL NUMBER (OR BLOCK)= C0
23	C1	CHANNEL NUMBER (OR BLOCK)= C1

Table 161-7. Zero, Full-Scale, and Reference Programming Steps (cont.)

24	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
25	ENTER	A: CHANNEL FUNCTION <A-Z>? P
26	A	A<A> AC VOLTS
27	ENTER	AA: AC RANGE <1,2>? 1
28	ENTER	AA: CHANNEL MENU CHOICE <1-5>? 1
29	3	AA<3> CHANNEL EXPRESSION
30	ENTER	CX=
31	(CX*512)-128000	CX= (CX*512) -128000
32	ENTER	AA: CHANNEL MENU CHOICE <1-5>? 4
33	5	AA<5> LOGGING FORMAT
34	ENTER	AA5: LOGGING FORMAT <1-7>? 1
35	7	AA5<7> NNNNN
36	ENTER	AA: CHANNEL MENU CHOICE <1-5>? 1
37	EXIT	A: CHANNEL FUNCTION <A-Z>? A
38	EXIT	CHANNEL NUMBER (OR BLOCK) = C1
39	C2	CHANNEL NUMBER (OR BLOCK) = C2
40	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
41	ENTER	A: CHANNEL FUNCTION <A-Z>? P
42	A	A<A> AC VOLTS
43	ENTER	AA: AC RANGE <1,2>? 1
44	ENTER	AA: CHANNEL MENU CHOICE <1-5>? 1
45	3	AA<3> CHANNEL EXPRESSION
46	ENTER	CX=
47	(CX*512)+128000	CX= (CX*512)+128000
48	ENTER	AA: CHANNEL MENU CHOICE <1-5>? 4
49	5	AA<5> LOGGING FORMAT
50	ENTER	AA5: LOGGING FORMAT <1-7>? 1
51	7	AA5<7> NNNNN
52	ENTER	AA: CHANNEL MENU CHOICE <1-5>? 1
53	EXIT	A: CHANNEL FUNCTION <A-Z>? A
54	EXIT	CHANNEL NUMBER (OR BLOCK) = C2
55	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

6. Press MONITOR, then 0 for channel 0, then ENTER.

7. Install a 100:1 voltage divider (Fluke Accessory Y2022) on the calibrator.

8. Set the calibrator for an output of +31.3mV (providing +313 uV at the voltage divider output). Turn the A/D Converter ZERO WIDTH potentiometer fully clockwise.

9. Set the A/D zero level as follows:

   a. Connect the voltage divider +volts terminal to the A/D INPUT test point on the Calibration Fixture with a test lead.

   b. Connect the voltage divider -volts terminal to the ANALOG COMMON test point on the Calibration Fixture with another test lead.

c. Note the Data Logger reading. Reverse the test leads and note the Data Logger reading.

d. Adjust the ZERO LEVEL potentiometer on the A/D Converter so that the positive and negative readings are of equal magnitude.

10. Adjust the ZERO WIDTH potentiometer on the A/D Converter until the Data Logger displays a reading of 20 +/-1 count.

11. Reverse the polarity of the test leads to the voltage divider and verify that the Data Logger reads -20 +/-1. If the Data Logger does not read -20 +/-1, repeat steps 9 through 11.

12. Press MONITOR again. The Data Logger should display:

MAIN MENU CHOICE <M> FOR MENU? A

13. Connect a Fluke Model 8505A or equivalent DMM as follows:

a. Connect the LO terminal on the DMM to the ANALOG COMMON test point on the calibration fixture.

b. Connect the HI terminal on the DMM to the 6.2V test point on the calibration fixture.

14. Adjust the 6.2V potentiometer on the A/D Converter for a DMM reading between 6.19995 and 6.20005 volts.

15. Disconnect the DMM from the Calibration Fixture.

16. Remove the divider from the calibrator. Connect the calibrator to the Calibration Fixture as follows:

a. Connect the HI terminal on the DMM to the A/D INPUT test point on the calibration fixture.

b. Connect the LO terminal on the DMM to the ANALOG COMMON test point on the calibration fixture.

17. Set the calibrator to output +2.000V.

18. Press MONITOR, then 1 for channel 1, then ENTER.

19. Adjust the A/D Converter -1.875 REF potentiometer shown in Figure 161-2 for a Data Logger reading of 0 +/- 1 count.

20. Press MONITOR again. The Data Logger should display:

MAIN MENU CHOICE <M FOR MENU>? A

21. By reversing the two connections made on the Calibration Fixture in step 16, apply -2.000V to the A/D input.

22. Press MONITOR, then 2 for channel 2, and then ENTER.

23. Adjust the A/D Converter +1.875 REF potentiometer for a Data Logger reading of 0 +/-1 count.

24. Press MONITOR again.

25. Connect the calibration fixture, and the DMM (Fluke 8505A or equivalent) as follows:

    a. Connect the LO terminal on the DMM to the ANALOG COMMON test point on the calibration fixture.

    b. Connect the HI terminal on the DMM to the 50mV REF test point on the calibration fixture.

26. Set the voltmeter to a range having 1 uV resolution. Wait one minute for the connection and leads to thermally stabilize before continuing. Adjust the 0.05V potentiometer on the A/D Converter for a DMM reading of 50.000mV within a tolerance of +/- 0.001mV.

27. Connect the HI terminal on the DMM to the 500mV REF test point on the calibration fixture.

28. Adjust the 0.5V potentiometer on the A/D Converter for a DMM reading of 500.000mV within a tolerance of +/- 0.005 mV.

29. Calibration is now complete. Turn the Data Logger off and back on to cause new calibration constants to be measured and stored by the A/D Converter, and perform the A/D Converter accuracy verification test in this subsection.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the High Performance A/D Converter is given in Table 161-8. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the High Performance A/D Converter is given in Figure 161-8.

TABLE 161-8. 2280A-161 HIGH PERFORMANCE A/D CONVERTER PCA
(SEE FIGURE 161-8.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
C 1		CAP,AL,330UF,+100-10%,25V	614404	89536	614404	1		
C 2		CAP,CER,1000PF,+-10%,500V,X5S	357806	56289	C016B102G102K	1		
C 3		CAP,CER,1000PF,+-5%,50V,COG	528539	51406	RPE113	1		
C 4, 10, 11,		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	14		
C 12, 13, 14,			519157					
C 15, 21, 22,			519157					
C 23, 25, 47,			519157					
C 54, 58			519157					
C 5, 17, 19		CAP,AL,270UF,+100-10%,20V	602656	89536	602656	3		
C 6		CAP,CER,0.01UF,+80-20%,100V,Z5V	149153	56289	C0238101F103M	1		
C 7, 16		CAP,TA,39UF,+-20%,6V	163915	56289	196D394X0020KA1	2		
C 8		CAP,CER,100PF,+-2%,100V,COG	512848	51406	RPE121	1		
C 9		CAP,CER,47PF,+-2%,100V,COG	512368	89536	512368	1		
C 18		CAP,AL,470UF,+100-10%,12V	602649	89536	602649	1		
C 20, 24, 56		CAP,CER,1.0UF,+-20%,50V,Z5U	436782	72982	8131-050-601-105M	3		
C 27, 28, 30,		CAP,AL,47UF,+-20%,16V	643304	89536	643304	5		
C 31, 57			643304					
C 29, 33, 34,		CAP,AL,10UF,+-20%,35V	643296	74840	RLR-PX	13		
C 39, 40, 44,			643296					
C 45, 49, 50,			643296					
C 51, 52, 60,			643296					
C 61			643296					
C 32, 35, 36		CAP,CER,150PF,+-2%,100V,COG	512988	89536	512988	3		
C 37		CAP,POLYPR,0.47UF,+-10%,100V	446807	89536	446807	1		
C 38		CAP,POLYPR,0.47UF,+-5%,50V	364042	84411	JF788	1		
C 41, 42		CAP,CER,68PF,+-2%,100V,COG	362756	89536	362756	2		
C 43, 46		CAP,POLYES,0.47UF,+-10%,100V	369124	89536	369124	2		
C 53, 62		CAP,CER,0.01UF,+-20%,100V,X7R	407361	72982	8121-A100-W5R-103M	2		
C 55		CAP,CER,0.0012UF,+-10%,500V,Z5R	106732	71590	CF122	1		
C 59		CAP,POLYPR,1500PF,+-5%,50V	706572	89536	706572	1		
CR 1- 8, 11,	*	DIODE,SI, 50 PIV, 1.0 AMP	379412	04713	1N4933	10		
CR 13	*		379412					
CR 9, 14- 25	*	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	13	2	
CR 10, 12	*	DIODE,SI, 20 PIV, 1.0 AMP	507731	83003	VSK120	2	1	
DS 1	*	LED,RED,90 LEAD PREP,LUM INT=2MCD	604884	89536	604884	1	3	
E 1		CONN,PWB,HEADER,SIP,0.100,4 PIN	417329	89536	417329	2		
F 1		FUSE,PICO,FAST,0.5A,125V	603274	71400	GFA	1	1	
H 1		SCREW	241349	89536	241349	3		
H 2		SCREW	413062	89536	413062	4		
H 3		WASHER	147728	89536	147728	4		
H 4		WASHER	110395	89536	110395	4		
MP 1		SPACER,MOUNT,NYLON,	175125	89536	175125	1	1	
MP 2		CABLE TIE,4"L,0.100"W,0.75 DIA	172080	89536	172080	1		
MP 3		BAG,SHIELDING,TRANSPARENT,12"X16"	680983	89536	680983	1		
MP 4		BOTTOM SHIELD ASSY	655506	89536	655506	1		
MP 5		SHIELD, A/D TOP	579037	89536	579037	1		
MP 6		HANDLE, HI PERFORMANCE A/D	633263	89536	633263	1		
MP 7		DECAL, OPTION -161	634469	89536	634469	1		
MP 8		DECAL, A/D CALIBRATION ADJUST	650341	89536	650341	1		
Q 1	*	SILICON, NPN, FAST SWITCHING D44H11	535542	89536	535542	1	1	
Q 2	*	TRANSISTOR,SI,NPN,HI-VOLTAGE	370684	04713	MPS A 42	1	1	
Q 3- 5, 9,	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	195974	64713	2N3906	5	1	
Q 23	*		195974					
Q 6- 8, 22,	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	5	1	
Q 24	*		218396					
Q 10	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	340026	04713	MPS6563	1	1	
Q 11	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	330803	07263	MPS6560	1	1	
Q 12, 14, 17-	*	TRANSISTOR,SI,N-JFET,REMOTE CUTOFF	429977	89536	429977	7	1	
Q 21	*		429977					
Q 13, 16	*	TRANSISTOR,SI,N-JFET,DUAL,TO-71	419283	89536	419283	2	2	
Q 15	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	242065	04713	2N5089	1	1	
Q 25	*	TRANSISTOR,SI,BV= 80V,100W,TO-202	495689	04713	MPSU56	1	1	
R 1		RES,CF,1.8K,+-5%,0.25W	441444	80031	CR251-4-5F1K8	1		
R 2		RES,CF,1.5K,+-5%,0.25W	343418	80031	CR251-4-5F1K5	1		
R 3, 41, 50		RES,CF,330,+-5%,0.25W	368720	80031	CR251-4-5F330E	3		
R 4, 44, 45		RES,CF,510,+-5%,0.25W	441600	80031	CR251-4-5F510E	3		
R 5, 6, 26,		RES,MF,10K,+-1%,0.125W,100PPM	168260	91637	CMF551002F	11		
R 27, 35, 42,			168260					
R 46, 47, 95,			168260					
R 120,121			168260					
R 7		RES,MF,15.8K,+-1%,0.125W,100PPM	293688	91637	CMF551582F	1		
R 9, 51, 90		RES,MF,1K,+-1%,0.125W,100PPM	168229	91637	CMF551001F	3		
R 10		RES,MF,39.2K,+-1%,0.125W,100PPM	236414	91637	CMF553922F	1		
R 11		RES,MF,40.2K,+-1%,0.125W,100PPM	235333	91637	CMF554022F	1		

TABLE 161-8. 2280A-161 HIGH PERFORMANCE A/D CONVERTER PCA
(SEE FIGURE 161-8.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
R 12, 13, 18,		RES,CF,51,+-5%,0.25W	414540	80031	CR251-4-5P51E	4		
R 19			414540					
R 14, 15, 22,		RES,CF,270,+-5%,0.25W	348789	80031	CR251-4-5P270E	5		
R 38, 39			348789					
R 16, 17, 23,		RES,CF,5.6K,+-5%,0.25W	442350	80031	CR251-4-5P5K6	4		
R 40			442350					
R 20, 21		RES,CF,30,+-5%,0.25W	442228	80031	CR251-4-5P30E	2		
R 24, 49, 53,		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	9		
R 55, 57, 58,			348839					
R 81,122,124			348839					
R 25,112,118,		RES,CF,100,+-5%,0.25W	348771	80031	CR251-4-5P100E	4		
R 119			348771					
R 29, 30, 34,		RES,CF,1.1K,+-5%,0.25W	348797	89536	348797	4		
R 74			348797					
R 31		RES,CF,820,+-5%,0.25W	442327	80031	CR251-4-5P820E	1		
R 32, 33		RES,CF,2.2K,+-5%,0.25W	343400	80031	CR251-4-5P2K2	2		
R 36, 59		RES,MF,28.7K,+-1%,0.125W,100PPM	235176	91637	CMF552872F	2		
R 37, 54, 67,		RES,CF,1M,+-5%,0.25W	348987	80031	CR251-4-5P1M	4		
R 69			348987					
R 43		RES,MF,16.2K,+-1%,0.125W,100PPM	226233	89536	226233	1		
R 48		RES,MF,154K,+-1%,0.125W,100PPM	289447	91637	CMF551543F	1		
R 52		RES,CF,8.2K,+-5%,0.25W	441675	80031	CR251-4-5P8K2	1		
R 56		RES,MF,332K,+-1%,0.125W,100PPM	289504	91637	CMF553323F	1		
R 60, 61, 80		RES,CF,47K,+-5%,0.25W	348896	80031	CR251-4-5P47K	3		
R 64		RES,MF,604K,+-1%,0.125W,100PPM	235374	89536	235374	1		
R 65		RES,MF,301K,+-1%,0.125W,100PPM	289488	91637	CMF5530102F	1		
R 66		RES,CF,18K,+-5%,0.25W	348862	80031	CR251-4-5P18K	1		
R 68		RES,CF,5.1K,+-5%,0.25W	368712	80031	CR251-4-5P5K1	1		
R 70, 73, 87		RES,MF,75K,+-1%,0.125W,100PPM	291443	91637	CMF557502F	3		
R 71, 72		RES,MF,23.7K,+-1%,0.125W,100PPM	188367	91637	MFF2372F	2		
R 75		RES,CF,39K,+-5%,0.25W	442400	80031	CR251-4-5P39K	1		
R 76, 85		RES,MF,2K,+-1%,0.125W,100PPM	235226	91637	CMF552001F	2		
R 77		RES,MF,42.2K,+-1%,0.125W,100PPM	221655	91637	CMF554222F	1		
R 78		RES,MF,43.2K,+-1%,0.125W,100PPM	272153	89536	272153	1		
R 79, 88, 89		RES,MF,30.1K,+-1%,0.125W,100PPM	168286	91637	MFF1-83012F	3		
R 82		RES,MF,46.4K,+-1%,0.125W,100PPM	188375	89536	188375	1		
R 83		RES,CC,3.9M,+-5%,0.25W	188417	89536	188417	1		
R 84		RES,MF,100K,+-1%,0.125W,100PPM	248807	91637	CMF551003F	1		
R 86		RES,CF,2K,+-5%,0.25W	441469	80031	CR251-4-5P2K	1		
R 91		RES,MF,619K,+-1%,0.125W,100PPM	288639	89536	288639	1		
R 92		RES,MF,6.81K,+-1%,0.125W,100PPM	268417	91637	CMF556813F	1		
R 93, 94		RES,MF,6.04K,+-0.1%,0.125W,25PPM	512301	89536	512301	2		
R 96, 97		RES,MF,49.9K,+-1%,0.125W,100PPM	268821	91637	CMF554992F	2		
R 98,109		RES,MF,10,+-1%,0.125W,100PPM	268789	91637	CMF5510R0F	2		
R 99,103,110		RES,VAR,CERM,1K,+-20%,0.5W	267856	11236	190PC102B	3		
R 100,108		RES,VAR,CERM,20K,+-20%,0.5W	267898	11236	190PC203B	2		
R 101		RES,VAR,CERM,100K,+-10%,0.5W	288308	89536	288308	1		
R 102,104		RES,MF,24.9,+-1%,0.125W,100PPM	296657	91637	CMF5524R9F	2		
R 105,107		RES,MF,36.5K,+-1%,0.125W,100PPM	235309	91637	CMF553652F	2		
R 106		RES,MF,348K,+-1%,0.125W,100PPM	289512	89536	289512	1		
R 111		RES,MF,2.8K,+-1%,0.125W,100PPM	325670	91637	CMF552801F	1		
R 113		RES,MF,61.9K,+-1%,0.125W,100PPM	237230	91637	CMF556192F	1		
R 114,115	*	ZENER REFERENCE SET	646539	89536	646539	1		
R 5	*		646539					
R 116		RES,VAR,CERM,500,+-20%,0.5W	267849	11236	190PC501B	1		
R 117,123		RES,CF,1K,+-5%,0.25W	343426	80031	CR251-4-5P1K	2		
S 1		SWITCH,ROTARY,1 POLE,16 POS,1 THUMB	615096	97527	1A-21-60-33-G-F	1		
T 1		INVERTER TRANSFORMER	580407	89536	580407	1		
TP 1, 2, 4,		CONN,TAB,FASTON,PRESS-IN,0.110 WIDE	512889	02660	62395	30		
TP 5, 14, 19-			512889					
TP 22, 30- 44,			512889					
TP 46- 49, 50,			512889					
TP 51			512889					
U 1	*	IC,REGULATING PULSE WIDTH MODULATOR	454678	01295	SG3524N	1	1	
U 2	*	IC,BPLR,DUAL DIFF LINE DRVR W/3-STATE	586081	12040	DS1692J	1	1	
U 3	*	IC,BPLR,DIFFERENTIAL LINE RECEIVER	586073	01295	SN55182J	1	1	
U 4	*	ISOLATOR,OPTO,HI-SPEED,DUAL	429894	28480	5082-4355	1	1	
U 5, 34	*	ISOLATOR,OPTO,HI-SPEED,8 PIN DIP	354746	89536	354746	2	1	
U 6, 7, 9,	*	IC,CMOS,QUAD D LATCH,+EDG TRG,W/RESET	412742	12040	MM74C173N	4	1	
U 14	*		412742					
U 8, 16, 25,	*	IC,CMOS,HEX BUFFER W/3-STATE OUTPUT	408773	12040	MM80C95N	5	1	
U 29, 37	*		408773					
U 10		IC,NMOS,8-BIT MICROCOMPUTER	685529	89536	685529	1		
U 11	*	IC,CMOS,BCD-DEC & BIN-OCTAL DCDR	473769	04713	MC14028B	1	1	

TABLE 161-8. 2280A-161 HIGH PERFORMANCE A/D CONVERTER PCA
(SEE FIGURE 161-8.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
U 12	*	IC,CMOS,DUAL D F/F,+EDG TRG W/SET&RST	536433	04713	MC4013BCP	1	1	
U 13	*	IC,CMOS,QUAD 2 INPUT NOR GATE	355172	02735	CD4001AE	1	1	
U 15	*	IC,COMPARATOR,DUAL,LO-PWR,8 PIN DIP	478354	12040	LM393N	1	1	
U 17	*	IC,CMOS,UNIV ASYNC RECEIVR/TRANSMITER	453464	32293	1M6402CPL	1	1	
U 18	*	IC,LSTTL,QUAD 2 INPUT XOR GATE	605626	01295	SN54LS86J	1		
U 19, 23	*	IC,LSTTL,DUAL JK F/F,+EDG TRG,W/CLR	605634	01295	SN54LS107AJ	2	1	
U 20	*	IC,LSTTL,QUAD 2 INPUT NAND GATE	605600	01295	SN54LS00J	1	1	
U 21, 22	*	IC,CMOS,8STAGE SYNC PRSET DWN BIN CNT	508689	02735	CD40103BE	2	1	
U 24	*	IC, 1.22V,100 PPM T.C.,BANDGAP REF	452771	89536	452771	1	1	
U 26		IC,2K X 8 EPROM (PROGRAMMED)	655555	89536	655555	1		
U 27, 28	*	IC,256 X 4 STAT RAM	605238	34371	HM1-6561-9	2	1	
U 30	*	IC,CMOS,7STAGE RIPPLE CARRY BIN CNTR	412965	86684	CD4024AE	1	1	
U 31	*	IC,CMOS,DUAL JK F/F,+EDG TRIG	355230	02735	CD4027AE	1	1	
U 32	*	IC,CMOS,DUAL SYNC BINRY UP CNTR	355164	04713	MC14520BCP	1	1	
U 33, 49	*	IC,OP AMP,DUAL,INDUSTRIAL TEMP RANGE	605550	01295	LM258JG	2	1	
U 35	*	IC, 2.5 V,40 PPM T.C.,BANDGAP REF	472845	04713	MC1403V	1	1	
U 36	*	IC,TTL,OCTAL D F/F,+EDG TRG	473223	01295	SN74LS374N	1	1	
U 38, 48	*	IC,CMOS,HEX INVERTER	404681	02735	CD4069BE	2	1	
U 39	*	IC,LSTTL,QUAD 2 INPUT OR GATE	605618	01295	SN54LS32J	1	1	
U 41	*	IC,CMOS,QUAD 2 INPUT AND GATE	408401	02735	CD4081BE	1	1	
U 42	*	IC,COMPARATOR,CERAMIC,8 PIN DIP	605592	89536	605592	1	1	
U 43, 44	*	IC,OP AMP,DUAL,JFET INPUT,8 PIN DIP	605576	89536	605576	2	1	
U 45, 47	*	IC,COMPARATOR,QUAD,CERAMIC,14 PIN DIP	605584	89536	605584	2	1	
U 46	*	IC,OP AMP,JFET INPUT,8 PIN DIP	605568	89536	605568	1	1	
U 48, 50- 52	*	IC,OP AMP,LO-OFFSET VOLTAGE,LO-NOISE	605980	06665	OP-07DP	4	1	
VR 2	*	ZENER,UNCOMP,6V TRANSIENT SUPPRESSOR	508655	24444	1N5908	1	1	
VR 3, 4	*	ZENER,UNCOMP, 6.2V, 5%, 20.0MA. 0.4W	325811	07910	1N753A	2	1	
W 1, 2		JUMPER, RECEPTACLE	530253	00079	530153-2	2		
XU 10, 17		SOCKET,DIP,0.100 CTR,40 PIN	429282	09922	DILB40P-108	2	5	
XU 26		SOCKET,DIP,0.100 CTR,24 PIN	376236	91506	324-AG39D	1		
XU 27, 28		SOCKET,DIP,0.100 CTR,18 PIN	418228	91506	318-AG39D	2		
XZ 7		SOCKET,DIP,0.100 CTR,16 PIN	276535	91506	316-AG39D	1		
Y 1	*	CRYSTAL,6MHZ,+-0.01%,HC-18/U	461665	89536	461665	1		
Z 1, 13		RES,NET,SIP,6 PIN,5 RES,10K,+-2%	500876	80031	95081002CL	2		
Z 2, 10		RES,NET,SIP,10 PIN,5 RES,10K,+-2%	529990	89536	529990	2		
Z 3, 4		RES,NET,SIP,10 PIN,9 RES,10K,+-2%	414003	80031	95081002CL	2		
Z 5		RES,NET,SIP,8 PIN,4 RES,10K,+-2%	513309	89536	513309	1		
Z 6		RES,NET,SIP,8 PIN,7 RES,10K,+-2%	412924	80031	95081002CL	1		
Z 7		RES,NET,DIP,16 PIN,8 RES,33,+-5%	413575	01121	314	1		
Z 8		RES,NET,DIP,16 PIN,8 RES,47K,+-5%	381996	89536	381996	1		
Z 9		RES,NET,DIP,16 PIN,8 RES,100K,+-5%	380618	89536	380618	1		
Z 11	*	RES NET ASSY TESTED	705509	89536	705509	1		
Z 12	*	RES NET ASSY TESTED	705558	89536	705558	1		

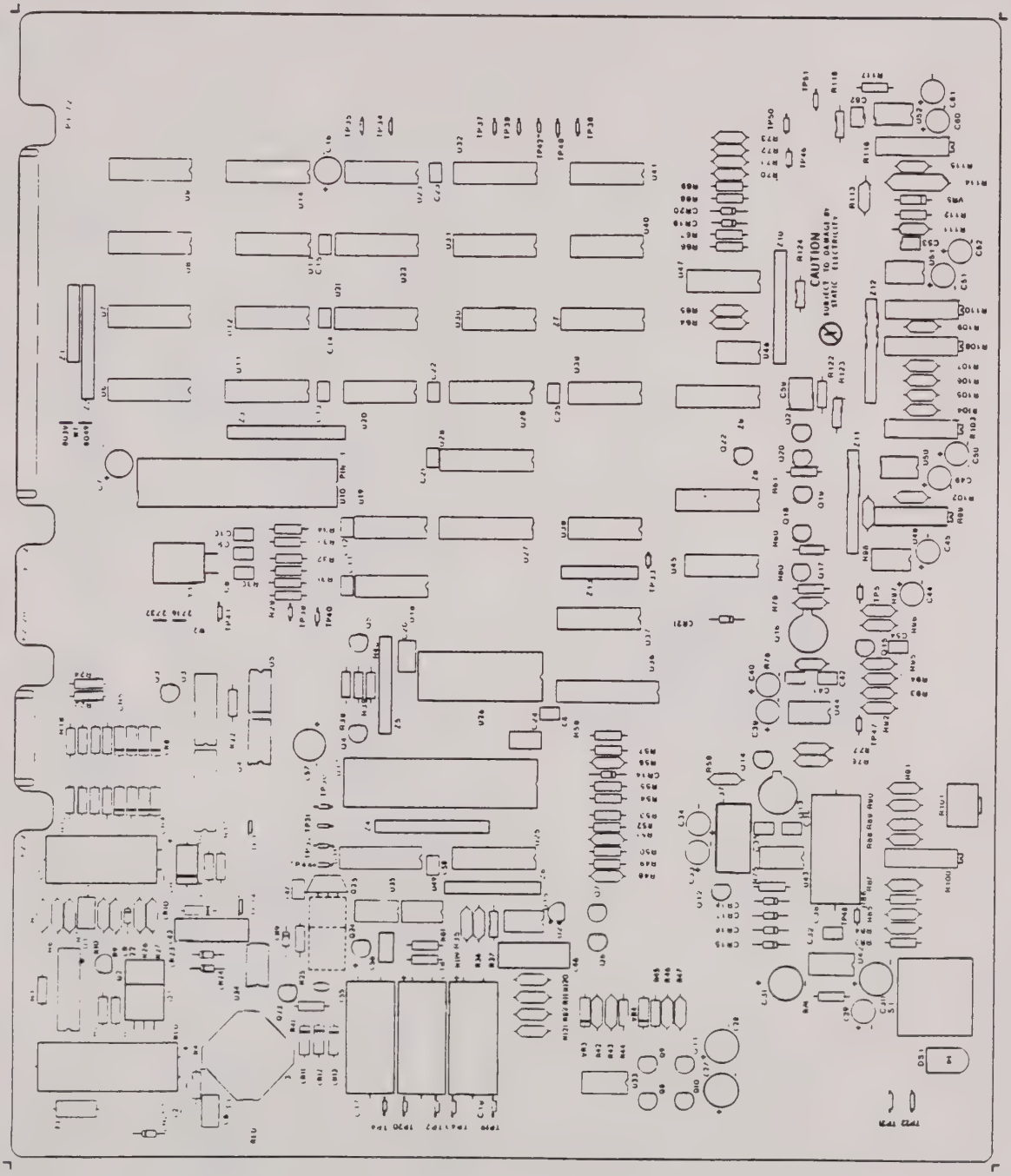
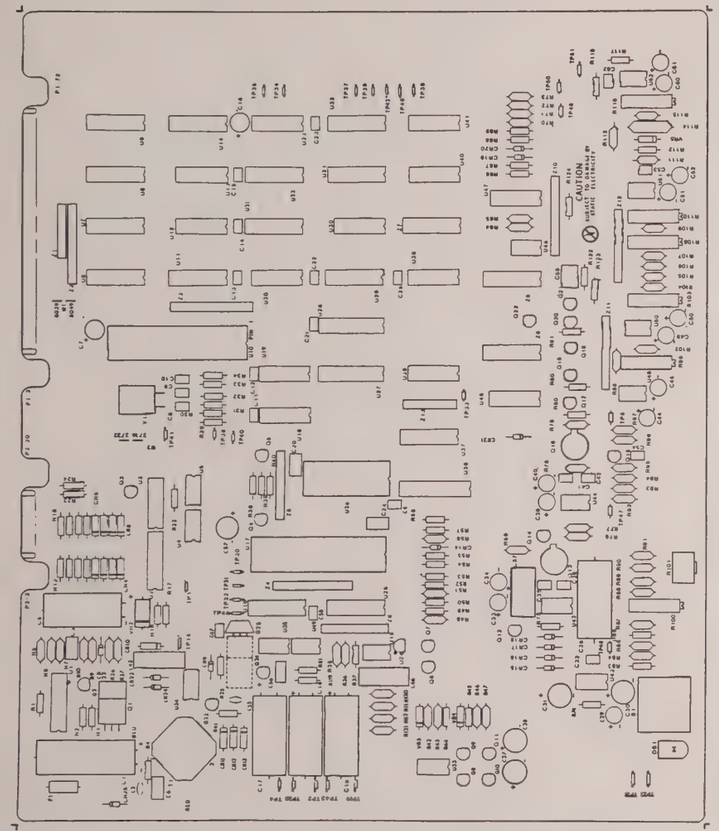


Figure 161-8. 2280A-161 High Performance A/D Converter PCA



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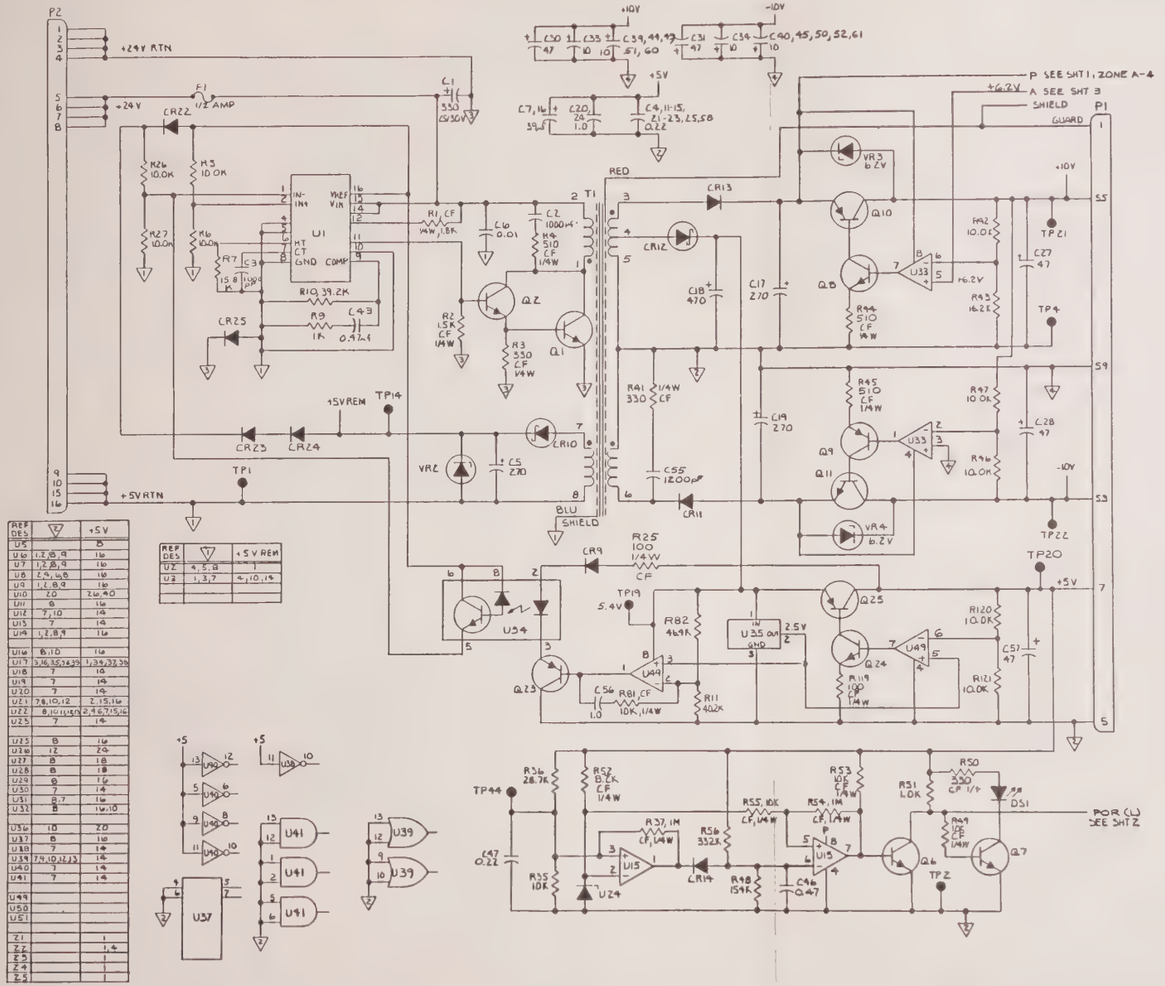


REF DES	▽	+5V
U5		8
U6	1,2,5,9	16
U7	1,2,5,9	16
U8	1,9,14,8	16
U9	1,2,8,9	16
U10	20	20,40
U11	8	16
U12	7,10	14
U13	7	14
U14	1,2,8,9	16
U16	8,10	16
U17	3,6,35,36,39	1,35,37,38
U18	7	14
U19	7	14
U20	7	14
U21	7,8,10,12	2,15,16
U22	8,10,11,49	2,4,6,7,15,16
U23	7	14
U25	8	16
U26	12	20
U27	8	18
U28	8	18
U29	8	16
U30	7	14
U31	8,7	16
U32	8	14,10
U36	10	20
U37	8	16
U38	7	14
U39	7,9,10,12,13	14
U40	7	14
U41	7	14
U49		
U50		
U51		
Z1		1
Z2		1,4
Z3		1
Z4		1
Z5		1

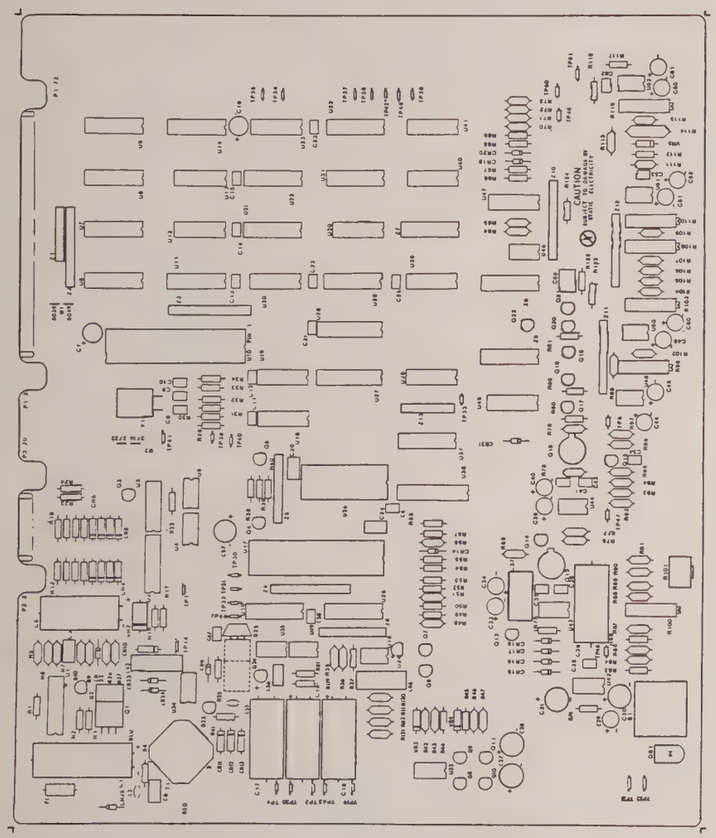
REF DES	▽	+5V REM
U2	4,5,8	1
U2	1,3,7	4,10,14

NOTES: UNLESS OTHERWISE SPECIFIED

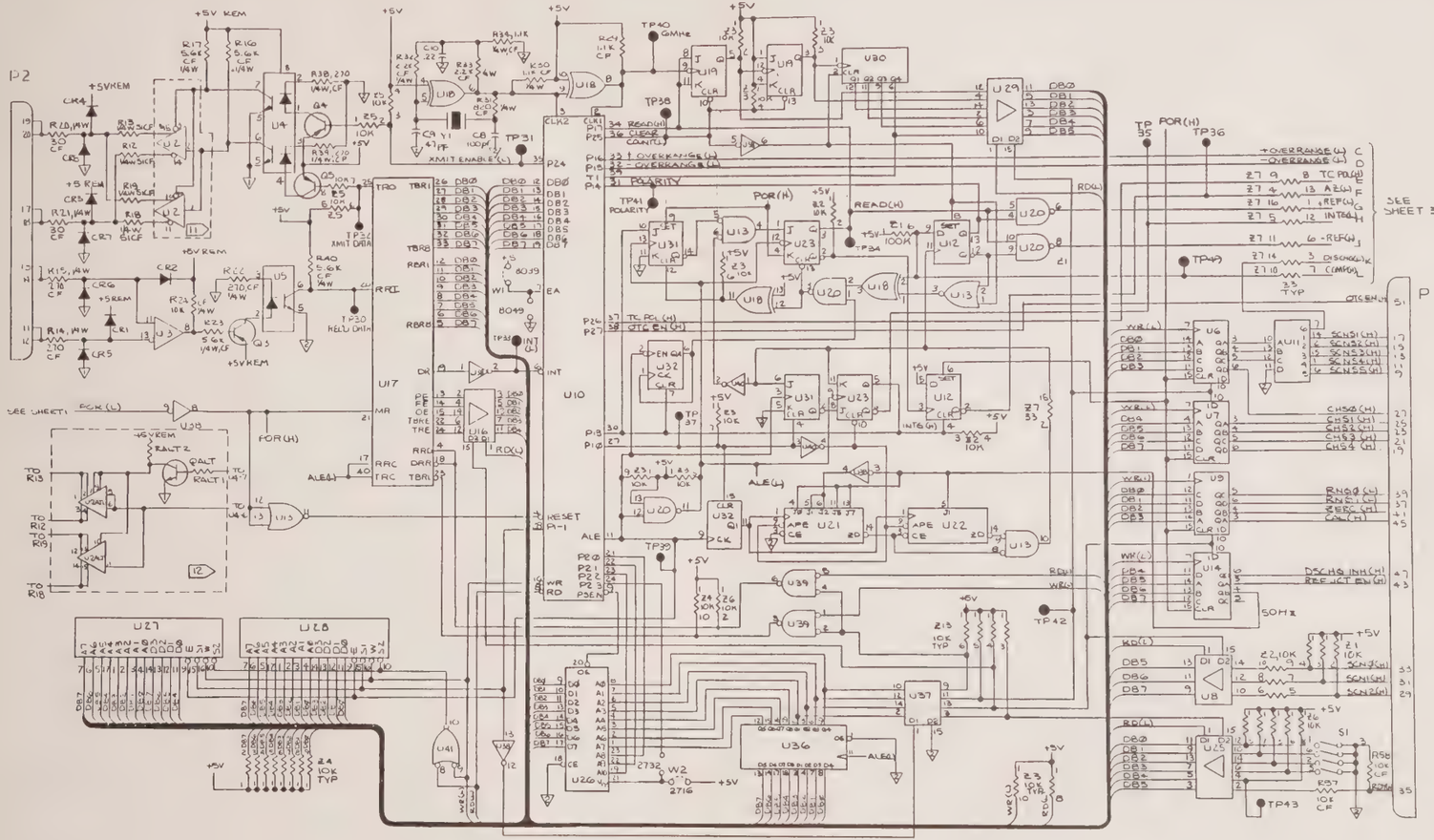
1. ALL RESISTANCES ARE IN OHMS.
2. ALL RESISTORS ARE 1/8W, MF, 1%.
3. ALL GRAPHIC SYMBOLS ARE IN ACCORDANCE WITH ANSI Y32.2 AND Y32.14.
4. ALL CAPACITANCE IS IN MICROFARADS.
7. R114, R115, and VR5 ARE A MATCHED SET.

2280A-1061

Figure 161-8. High Performance A/D Converter Schematic Diagram

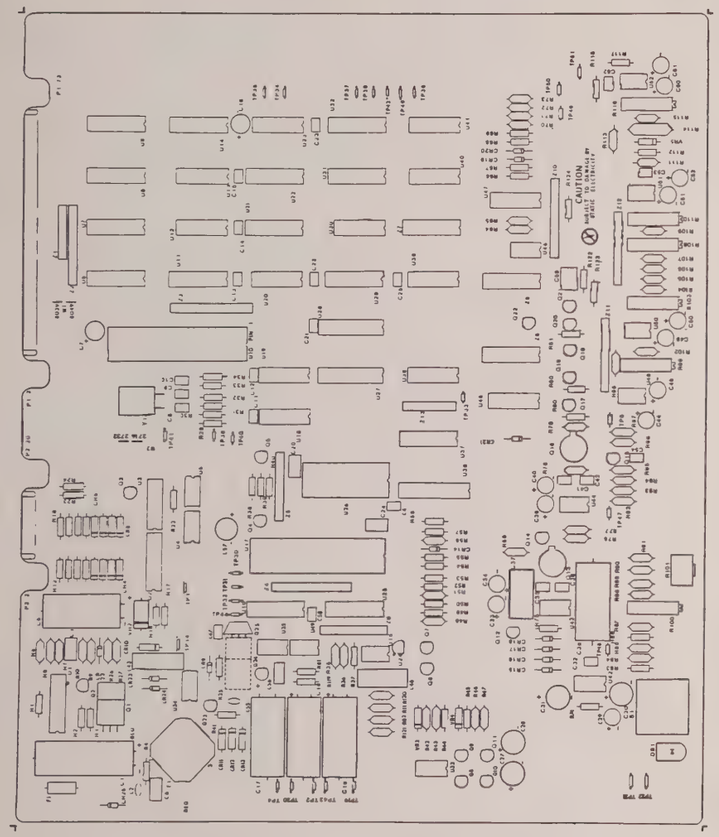


2280A-1661



2280A-1061

Figure 161-8. High Performance A/D Converter Schematic Diagram (cont.)



2280A-1661

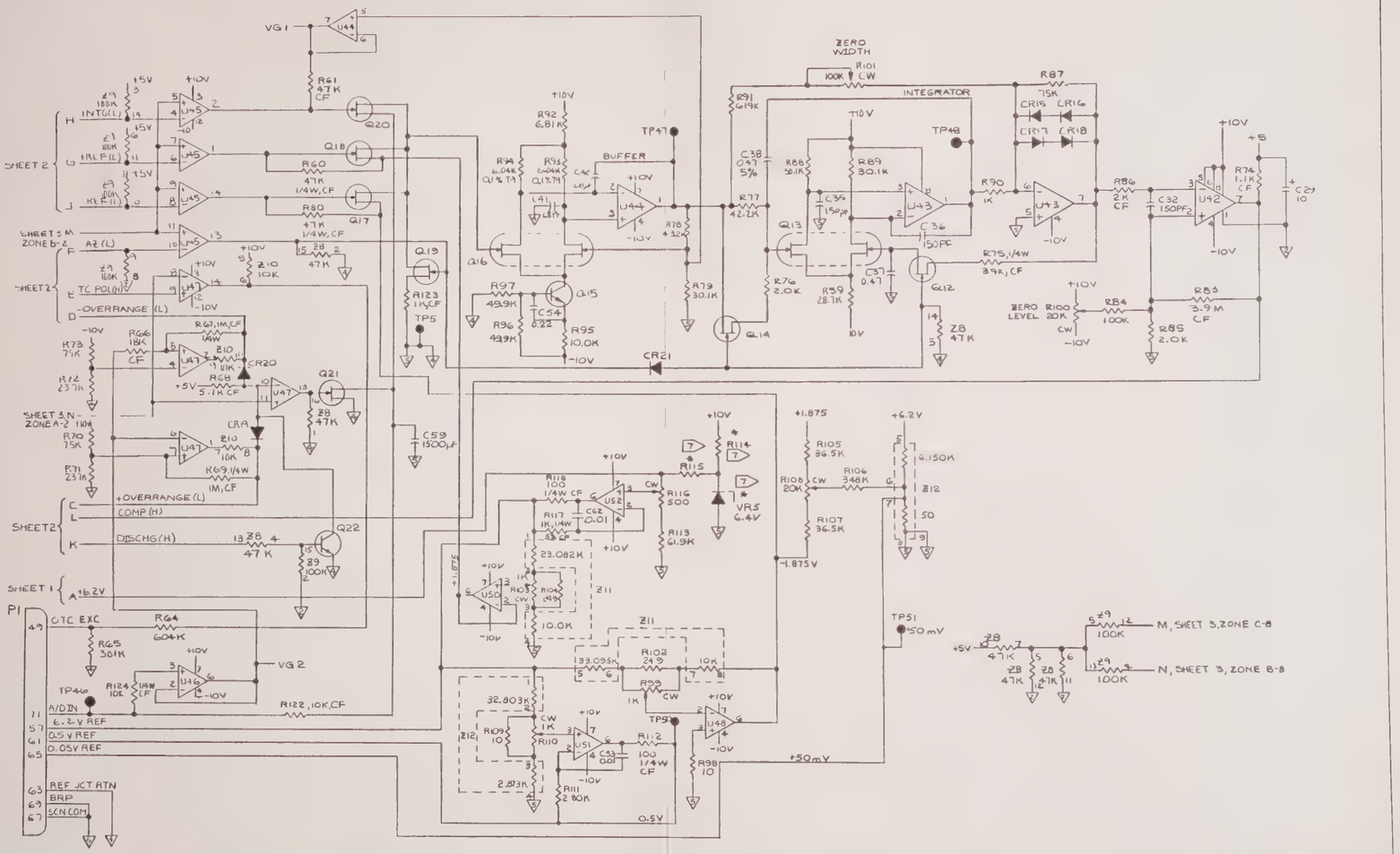


Figure 161-8. High Performance A/D Converter Schematic Diagram (cont.)

Option 2280A-162
Thermocouple/DC Volts Scanner

DESCRIPTION

The 2280A-162 Thermocouple/DC Volts Scanner Option is a plug-in, 1 uV, 20-channel dry-reed relay scanner. This Scanner operates as a self-calibrating analog data multiplexer, linking the A/D Converter to external measurement points. One to five scanners may be installed with each A/D Converter installed in a Data Logger system.

Each channel of the scanner provides a High, a Low, and a Shield input which can be accessed through a connector option plugged onto the scanner's two 44-pin card-edge connectors. The scanner accepts only dc voltage inputs, but several different connector options are available to convert various analog measurements into dc voltages. Available connector options are:

- Option 2280A-160 AC Voltage Input Connector
- Option 2280A-171 Current Input Connector
- Option 2280A-175 Isothermal Input Connector
- Option 2280A-176 Voltage Input Connector

WHERE TO FIND FURTHER INFORMATION

In this subsection the Thermocouple/DC Volts Scanner theory of operation, performance tests, calibration procedure, troubleshooting, parts list, and schematic diagram are given. Installation and system configuration instructions are located in the 2280 Series System Guide, and operating and programming instructions are located in the 2280 Series User Guide. Option specifications are located in the Appendices to this manual and the System Guide.

The test equipment required to perform the procedures in this subsection is listed in Table 162-1. A summary of test equipment required to perform all procedures in this manual is given in Table 1-1 in Section 1 of this manual.

THEORY OF OPERATION

The Thermocouple/DC Volts Scanner theory of operation includes an overall functional description of the Thermocouple/DC Volts Scanner, a block diagram analysis which describes how each major circuit block on the assembly works, and a circuit analysis which explains each block. Block diagrams and simplified schematics are included with the text. A parts lists and a schematic diagram for the Thermocouple/DC Volts Scanner can be found at the end of this option subsection.

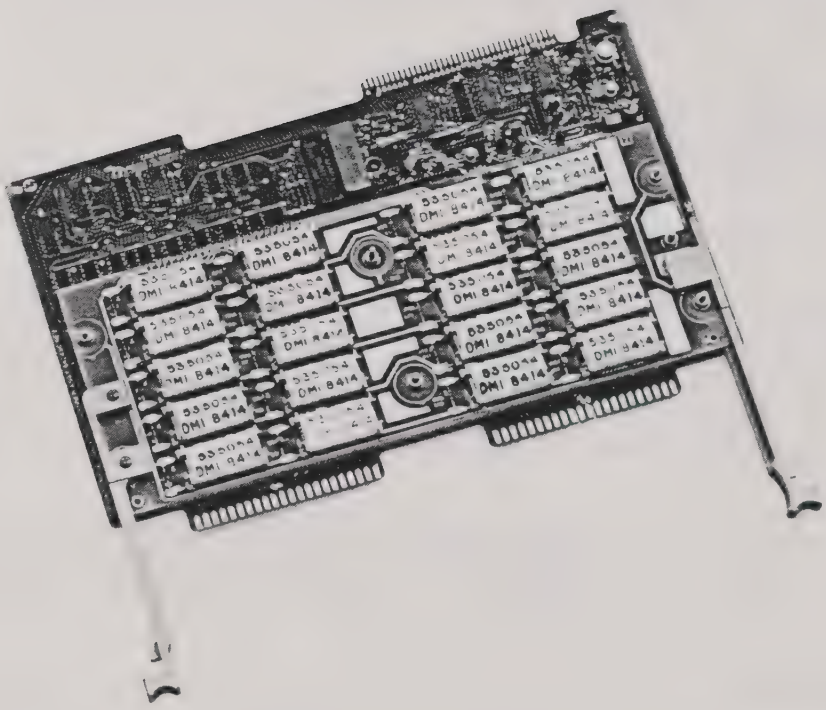


Figure 162-1. Thermocouple/DC Volts Scanner

Table 162-1. Required Test Equipment

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
DC Calibrator	+/- 31.3 mV +/- 20 uV +2.048V +/- 50 uV -2.048V +/- 2 uV of +2.048 500 mV +/- 20 uV 6.2V +/- 155 uV 6.8V +/- 0.1V 5.0V +/- 100 uV 7.9V +/- 200 uV *63V +/- 800 uV 1.008V +/- 40 uV	Fluke 343 *63V output used only for one optional test.
100:1 Divider	+/- 0.005%	Fluke Y2022
Calibration Fixture Assy	.....	Fluke Y2056
Digital Multimeter	+/- 10V +/- 0.06V 0V +/- 1 uV (differential)	Fluke 8505A
Resistor	1 kohm +/- 5%	Fluke Part Number (108597)
Resistor	10 kohm +/- 5%	Fluke Part Number (109165)
High Performance A/D Converter	.....	Fluke 2280A-161 (no substitute)
Isothermal Input Connector	.....	Fluke 2280A-175 (no substitute)
Voltage Input Connector	.....	Fluke 2280A-176 (no substitute)

Overall Functional Description

The Thermocouple/DC Volt Scanner is a reed-relay multiplexer and programmable gain amplifier that allows the A/D Converter access to twenty dc volt or thermocouple input measurement channels.

Gain and zero adjustments need not be made to the scanner amplifier. The A/D directly measures the offset and true gain of each scanner and compensates for those errors during measurements of user inputs.

Various operating modes of the scanner are listed below in Table 162-2. The A/D measures the scanner output for all modes but Discharge, Open Thermocouple Test, and De-Select modes. The user's measurement inputs, channels 0 to 19, are accessed during the Measure modes. The remaining scanner modes are used for the zero and gain correction functions which are transparent to the user.

Table 162-2. Scanner Operating Modes

MODE	OPERATION
Deselect	De-energizes the reed switches of the input channel previously measured, and waits for them to open.
Discharge	Shorts the input filter capacitor to ground in preparation for the next measurement.
Open T/C Test	Bleeds a small current into the input filter capacitor and changes the range to 512 mV. The A/D determines whether the connected thermocouple circuit has low enough resistance.
64mV Zero	The A/D measures the scanner offset with the input to the scanner buffer amplifier grounded through a 39kohm resistor on the 64mV range.
8V Zero	The A/D measures the scanner offset with the input grounded through a 78kohm resistor on the 8V range.
50mV Cal	The A/D measures the scanner output when a 50mV input supplied by the A/D Converter is applied on the 64mV range.
500mV Cal	The A/D measures the scanner output when a 500mV input supplied by the A/D Converter is applied on the 512mV range.
6.2V Cal	The A/D measures the scanner output with an A/D supplied 6.2V input on the 8V range.
64mV Measure	The A/D measures the scanner output with an input channel selected on the 64mV range. Channel reeds are closed.
512mV Measure	The A/D measures the scanner output with the scanner on the 512mV range with an input channel selected. Channel reeds are closed.
8V Measure	The A/D measures an input channel on the 8V scanner range. Selected channel reeds are closed.
64V Measure	An input channel is measured by the A/D with the scanner on the 64V range. Channel reeds are closed.

Table 162-2. Scanner Operating Modes (cont.)

Ref Junction	The A/D measures the output voltage of the semiconductor sensor embedded in the isothermal input connector (when one is used) with the scanner on the 512mV range. This measurement is required for thermocouple temperature measurements.

Scanner operation can be divided into two measurement sequences; calibration and scanning. Calibration is performed approximately every ten minutes at the direction of the mainframe and involves measuring the gains of the scanner amplifier on three ranges. Scanning, the normal mode of operation, occurs when the A/D Converter is instructed to measure user input channels. Both sequences are controlled by the A/D Converter through the scanner control lines: Scanner Selects (SCNS[1:5](H)), Channel Selects (CHS[0:4]), Range Selects (RNG[0:1](L)), Calibrate (CAL(H)), Discharge Inhibit (DSCHG INH(H)), Reference Junction Enable, Open Thermocouple Test (OTC EN(H)) , and Zero (ZERO(H)).

Detailed Circuit Description

The amplifier composed of U11, Q14, Q15, Q16, CR28, R19, and R20, has gains of 4 and 32. Amplifier gain is selected by U10 under control of signal RNG0(L). Components Z5, Q3, Q4, and K20 work as a switchable high-impedance, 125 to 1 ratio, voltage divider. The divider is enabled by the RNG1(L) control signal. To remove high-frequency noise, input signals are filtered by C15 in conjunction with R10 or the output resistance of Z5 depending on the state of the RNG1(L) signal.

The full-scale output of the amplifier is bipolar 2.048 Volts. The two amplifier gains in combination with the high-impedance divider yields four dc volt ranges: 64mV, 512mV, 8V, and 64V full scale.

Decoders U2 and U8, gating in U3, and comparators U7, U9, and U10 select one of several inputs to the amplifier. The selection of an input is performed by the A/D Converter. Table 162-3 identifies the status of FET , and relay switches for all scanner operating modes.

Reed switches provide high voltage isolation from channel to channel and scanner to scanner. Each input channel is connected to the scanner amplifier circuitry by three reed switches closed by a single drive coil (K0 through K19). A unique channel is selected when decoder U2 is presented with an input from 0 through 10 (decimal) via signals CHS[0:3](H) and SCNS1(H) is true. Decoder U2 does not activate any outputs (and therefore no channels are selected) when it's inputs are outside the 0 through 10 range (decimal).

Components U3 and U4 identify the presence of the scanner plus its type to the A/D Converter. In response to the scanner select control line, SCNS1, being asserted, the DC Volt scanner pulls SCN[0:2](H) lines low when an Isothermal Input Connector (option 2280A-175) is installed on the scanner and pulls only SCN0(H) and SCN1(H) low if a voltage input connector (option 2280A-176) or current input connector (2280A-171) or no input connector is installed.

GENERAL MAINTENANCE

The Option 2280A-162 PCA normally does not require cleaning unless dirt, dust, or other contamination is visible on the surface. To clean the PCA, follow the cleaning instructions in Section 4 of this manual.

PERFORMANCE TESTS

Three performance tests that can be performed separately or together verify that the Thermocouple/DC Volts Scanner is operational and meets its accuracy specifications. Since the scanner must be used with the A/D Converter (option 2280A-161), the A/D Converter must be tested and calibrated first. The three tests are:

- Channel Integrity Test: This test verifies that each scanner channel is functional.

- Accuracy Verification Test: The accuracy verification test checks scanner accuracy against specifications. Since all voltage readings displayed by the Data Logger are dependent upon the accuracy of the A/D Converter, the A/D Converter must be calibrated before performing this test.

- Open Thermocouple Response Test: This test checks whether the A/D Converter and scanner respond with an open thermocouple indication when presented with an open thermocouple channel input. Note that this test is also one of the A/D Converter performance tests. It is repeated here because both the scanner and the A/D contain the circuitry which senses open thermocouple conditions. The test need not be repeated if it was performed previously.

These performance tests verify that the Thermocouple/DC Volts Scanner meets its specified accuracy tolerances on all channels. If the scanner fails one of the tests, it must be repaired or replaced since there are no calibration adjustments on the scanner. Test steps marked with an asterisk (*) are optional since they test functions that are not required for many applications.

Table 162-3. Scanner Switch Configurations and Operation Modes

NOT AVAILABLE AT THIS PRINTING

Channel Integrity Test

1. Turn the 2280 keyswitch to OFF. Disconnect the line power cord or battery input power and all other high voltage inputs.

2. Set the address switch on an A/D Converter (Option 2280A-161) to 0 and install it in the top option slot of the Data Logger. Install the Thermocouple/DC Volts Scanner to be tested in the option slot just below the A/D Converter.

3. Connect a pair of test leads to the HI and LO terminals of Channel 0 of a 2280A-175 or 2280A-176 input connector. Install the input connector on the scanner.

4. Reconnect line or battery power to the Data Logger.

5. Turn the keyswitch to PROGRAM.

6. Program all scanner channels such that measurements will be made on the 8.0000VDC range by following the programming steps listed in Table 162-4.

Table 162-4. Channel Integrity Test Programming Steps

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
7	0..1499	CHANNEL NUMBER (OR BLOCK) = 0..1499
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
10	D	A<D> DC VOLTS/CURRENT
11	ENTER	AD: DC RANGE <1-5>? 1
12	2	AD<2> 8.0000 VDC
13	ENTER	AD: CHANNEL MENU CHOICE <1-5>? 1
14	EXIT	A: CHANNEL FUNCTION A-Z>? D
15	EXIT	CHANNEL NUMBER (OR BLOCK) = C0..1499
16	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

7. Connect the calibrator output to the scanner input connector test leads and set the calibrator to output 7.9V.

8. Press MONITOR, then 0, then ENTER.

9. Verify that the Data Logger displays 7.9000V within a tolerance of +/- 0.001V.

10. Test each scanner channel by moving the test leads to the next channel and monitoring that channel by pressing MONITOR, the channel number, then ENTER. The Data Logger reading on each channel should be 7.9000V +/- 0.001V.

12. This completes the channel integrity test. Continue with the accuracy verification test if you are performing a complete verification test of the scanner and you have not already performed the test in the A/D Converter performance test section.

Accuracy Verification Test

1. Disconnect the Data Logger line and/or battery power and all other high voltage inputs.

2. Set the A/D Converter address switch to 0, and install the A/D Converter in the top option slot of the Data Logger. Install a scanner in the slot just below the A/D Converter.

3. Install either a 2280A-175 or 2280A-176 input connector on the Thermocouple/DC Volts Scanner and connect a pair of test leads to the HI and LO terminals for channel 0 on the connector.

4. Reconnect line or battery power to the Data Logger.

5. Set the calibrator to output 6.2V. Connect the calibrator output to the input of the 100:1 Voltage Divider. Connect the output of the divider to the scanner input connector test leads.

6. Turn the keyswitch to PROGRAM.

7. Program the Data Logger to measure channel 0 on the 64.000mV dc range using the steps given in Table 162-5.

Table 162-5. Accuracy Verification Test Program

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = CO
7	0	CHANNEL NUMBER (OR BLOCK) = 0
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
10	D	A<D> DC VOLTS/CURRENT
11	ENTER	AD: DC CHANNEL RANGE <1-5>? 1
12	4	AD<4> 64.000 MVDC
13	ENTER	CHANNEL MENU CHOICE <1-5>? 1
14	EXIT	A: CHANNEL FUNCTION <A-Z>? D
15	EXIT	CHANNEL NUMBER (OR BLOCK) = CO
16	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

8. Press MONITOR, then 0, then ENTER. The Data Logger should display a value of 62.000mV within a tolerance of +/- 0.010mV.

9. Press MONITOR. The Data Logger should display:

   MAIN MENU CHOICE <M FOR MENU>? A

10. Change to the 512mV voltage range on channel 0 by keying in the programming steps listed in Table 162-6.

11. Change the calibrator output to 500mV.

12. Remove the 100:1 divider and connect the calibrator output directly to the channel 0 connector terminals.

13. Press MONITOR, then 0, and then ENTER. Verify that the displayed value is 500.00mV within a tolerance of +/- 0.1mV.

14. Press MONITOR. The Data Logger should display:

   MAIN MENU CHOICE <M FOR MENU>? A

Table 162-6. 512mV Range Programming Steps

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
3	0	CHANNEL NUMBER (OR BLOCK) = 0
4	ENTER	PROGRAM COPY DELETE OR LIST <P,D,C,L>? P
5	ENTER	A: CHANNEL FUNCTION <A-Z>? D
6	ENTER	AD: DC RANGE <1-5>? 4
7	3	AD<3> 512.00 MVDC
8	ENTER	AD: CHANNEL MENU CHOICE <1-5>? 1
9	EXIT	A: CHANNEL FUNCTION <A-Z>? D
10	EXIT	CHANNEL NUMBER (OR BLOCK) = C0
11	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

15. Re-enter the keystrokes listed in Table 161-6, except at step 7. At step 7, enter a 2 instead of a 3 to obtain the prompt AD<2> 8.0000 VDC and then press ENTER. This programs channel 0 to the 8.0000VDC range.

16. Change the calibrator output to 7.9V.

17. Press MONITOR, then 0, and then ENTER. Verify that the displayed value is 7.9000V within a tolerance of +/- 0.001V.

18. Press MONITOR. The Data Logger should display:

    MAIN MENU CHOICE <M FOR MENU>? A

*19. Re-enter the keystrokes listed in Table 161-6, except at step 7. At step 7, enter a 1 instead of a 3 to obtain the prompt AD<1> 64.000 VDC and then press ENTER. This programs the instrument to measure channel 0 on the 64.000VDC range.

*20. Change the calibrator output to 63V.

*21. Press MONITOR, then 0, and then ENTER and verify that the displayed value is 63.000V within a tolerance of +/- 0.020V.

*22. Press MONITOR. The Data Logger should display:

    MAIN MENU CHOICE <M FOR MENU>? A

*23. The accuracy verification test is now complete. Continue with the open thermocouple response test if you are performing a complete verification test of the scanner and you have not already performed the test in the A/D Converter performance test section.

Open Thermocouple Response Test

1. Disconnect line and battery power and all other high voltage inputs from the Data Logger.

2. Set the A/D Converter address switch to 0, install the A/D Converter in the top option slot of the Data Logger, and install the Thermocouple/DC Volts Scanner in the slot just below the A/D Converter.

3. Connect a pair of test leads to the channel 0 HI and LO terminals on the isothermal input connector and install the isothermal connector on the scanner.

4. Reconnect line or battery power to the Data Logger.

5. Turn the Data Logger keyswitch to the PROGRAM position.

6. Connect the leads from the isothermal input connector to a 1 kohm resistor.

7. Program the Data Logger to measure channel 0 as if a thermocouple were connected using the steps given in Table 162-7.

Table 162-7. Open Thermocouple Response Test Programming Steps

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = CO
7	0	CHANNEL NUMBER (OR BLOCK) = 0
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
10	T	C,T> THERMOCOUPLE
11	ENTER	AT: TC TYPE <J,K,T,E,R,S,B,N,C,H,V>? J
12	ENTER	AT: CHANNEL MENU CHOICE <1-5>? 1
13	EXIT	A: CHANNEL FUNCTION <A-Z>? T
14	EXIT	CHANNEL NUMBER (OR BLOCK) = CO
15	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

8. Press MONITOR, then 0, and then ENTER. Verify that the unit displays a measurement value equal to the ambient temperature +/-2 degrees C and not the message OPEN TC.

9. Press MONITOR. The Data Logger should display:.

   MAIN MENU CHOICE <M FOR MENU>? A

10. Replace the 1 kohm resistor with a 10 kohm resistor to simulate a high resistance or open thermocouple.

11. Press MONITOR, then 0, and then ENTER. Verify that the unit displays:

    C 0 OPEN TC

12. Press MONITOR. The Data Logger should display:

    MAIN MENU CHOICE <M FOR MENU>? A

13. Disconnect the 10 kohm resistor and the test leads from the input connector. Performance testing of the Thermocouple/DC Volts Scanner is complete.

CALIBRATION

No calibration is required for the Thermocouple/DC Volts Scanner.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the Thermocouple/DC Volts Scanner is given in Table 162-8. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the Thermocouple/DC Volts Scanner is given in Figure 162-2.

TABLE 162-8. 2280A-162 THERMOCOUPLE/DC VOLTS SCANNER PCA
(SEE FIGURE 162-2.)

REFERENCE DESIGNATOR A->NUMERICS---)	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	RS -Q	NOT -E
C 1- 8, 16		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	9		
C 9, 13		CAP,CER,1.0UF,+-20%,50V,Z5U	436782	72982	8131-050-601-105M	2		
C 10		CAP,CER,33PF,+-2%,100V,COG	513226	51406	RPE121	1		
C 11, 12		CAP,CER,1800PF,+-5%,50V,COG	528547	89536	528547	2		
C 15		CAP,POLYPR,6800PF,+-5%,50V	706564	89536	706564	1		
C 17		CAP,TA,10UF,+-20%,15V	193623	56289	196D106X0015A1	1		
CR 1- 6, 8-	*	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	26		
CR 27	*		203323					
CR 7	*	DIODE,SI,2 PELLET,BV= 20.0V,400 MW	375477	09214	MPD200	1	6	
CR 28	*	DIODE,SI,N-JFET,CURRENT REG,IF=0.43MA	393454	89536	393454	1	1	
H 1		WASHER,FLAT S STEEL,#4,0.032 THK	146225	89536	146225	1		
H 2		SCREW,MACH,PHP,S STL,4-40X3/4	681973	89536	681973	1		
H 3		NUT,HEX,S.STL,4-40	147611	89536	147611	1		
J 1- 22		CONN,POST,PWB,.025SQ,NON-INSUL,GOLD30	513861	00779	1-87022-7	22		
K 0- 19		RELAY COIL ASSY	535054	89536	535054	20		
K 20		RELAY,REED,1 FORM A,5VDC	404061	71707	CR-3201-5-710	1		
K 21		RELAY,REED,1 FORM A,5VDC	520247	71707	UF-40115	1		
MP 1		SPACER,REED	617415	89536	617415	1		
MP 2		SPACER,SWAGED,RND,BRASS,0.125IDX0.187	436675	89536	436675	5		
MP 3		SPACER,SWGD,RND,BRASS,0.150IDX0.125	335075	89536	335075	1		
MP 4		BAG,SHIELDING,TRANSPARENT,12"X16"	680983	89536	680983	1		
MP 5		BOTTOM GUARD	579151	89536	579151	1		
MP 6		PCB RETAINER	579078	89536	579078	2		
MP 7		INSULATOR, BOTTOM	579102	89536	579102	1		
P 1- 22		CONN,PWB,REC,BOARD MOUNT,1/16 THICK	267476	00779	85861-2	22		
Q 1- 4, 6-	*	TRANSISTOR,SI,N-JFET,TO-92	376475	15818	U2810J	13	1	
Q 12, 15, 16	*		376475					
Q 5	*	TRANSISTOR,SI,N-JFET,DUAL,TO-71	419283	89536	419283	1	1	
Q 13	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	418707	04713	MPS56562	1	3	
Q 14	*	TRANSISTOR,SI,N-JFET,DUAL,TO-71	461772	17856	DN1675	1	1	
Q 17	*	TRANSISTOR,SI,N-JFET,REMOTE CUTOFF	429977	89536	429977	1	1	
R 1, 2		RES,CF,20K,+-5%,0.25W	441477	80031	CR251-4-5P20K	2		
R 3, 6- 9,		RES,CF,100K,+-5%,0.25W	348920	80031	CR251-4-5P100K	7		
R 14, 16			348920					
R 4, 21		RES,CF,100,+-5%,0.25W	348771	80031	CR251-4-5P100E	2		
R 5, 33, 36,		RES,CC,150,+-5%,0.25W	147934	01121	CB1515	21		
R 37, 40, 41,			147934					
R 44, 45, 48,			147934					
R 50, 52, 53,			147934					
R 55, 58, 60,			147934					
R 61, 63, 66,			147934					
R 68, 69, 71			147934					
R 10		RES,TINOX,39K,+-2%,2W	615435	89536	615435	1		
R 11, 13, 15,		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	4		
R 32			348839					
R 17		RES,CF,470,+-5%,0.25W	343434	80031	CR251-4-5P470E	1		
R 18, 23		RES,CF,39K,+-5%,0.25W	442400	80031	CR251-4-5P39K	2		
R 19, 20		RES,MF,15.4K,+-0.1%,0.125W,25PPM	340604	91637	CMF551542F	2		
R 31		RES,CF,1K,+-5%,0.25W	343426	80031	CR251-4-5P1K	1		
R 34, 35, 38,		RES,CC,470,+-5%,0.25W	147983	01121	CB4715	20		
R 39, 42, 43,			147983					
R 46, 47, 49,			147983					
R 51, 54, 56,			147983					
R 57, 59, 62,			147983					
R 64, 65, 67,			147983					
R 70, 72			147983					
S 1- 60		SWITCH,REED,1 FORM A,10VA,36AT	647578	89536	647578	60	3	
U 1, 5, 6,	*	IC,CMOS,DUAL 2 IN NAND DRVR W/OPN DRN	604207	02735	CD40107BE	11	1	
U 12- 19	*		604207					
U 2	*	IC,CMOS,BCD-DEC & BINRY-OCTAL DECODER	650689	89536	650689	1	1	
U 3	*	IC,CMOS,QUAD 2 INPUT NOR GATE	355172	02735	CD4001AE	1	1	
U 4	*	IC,CMOS,HEX BUFFER W/3-STATE OUTPUT	407759	12040	MM80C97N	1	1	
U 7, 9, 10	*	IC,COMPARATOR,QUAD,CERAMIC,14 PIN DIP	605584	89536	605584	3	1	
U 8	*	IC,CMOS,DUAL 1 OF 4 DECODER	584987	04713	MC14555BP	1	1	
U 11	*	IC,OP AMP,GENERAL PURPOSE,TO-78 CASE	418368	89536	418368	1	1	
Z 1, 3		RES,NET,SIP,8 PIN,7 RES,100K,+-2%	412908	89536	412908	2		
Z 2		RES,NET,SIP,6 PIN,5 RES,100K,+-2%	412726	89536	412726	1		
Z 4	*	GAIN RES NET ASSY TESTED-2280A	611186	89536	611186	1		
Z 5	*	INPUT DIVIDER RESNET ASSY TESTED2280A	616011	89536	616011	1		

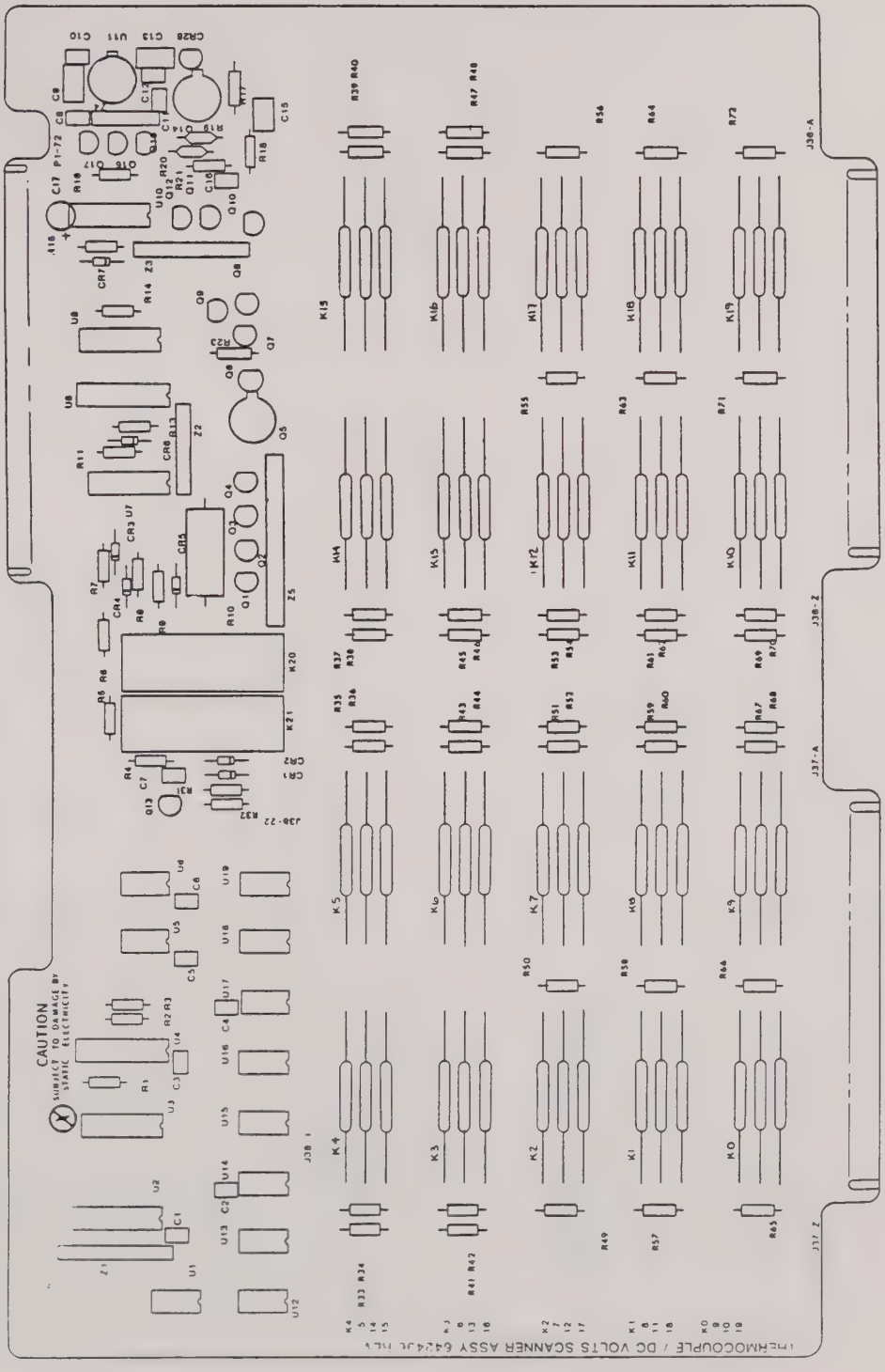
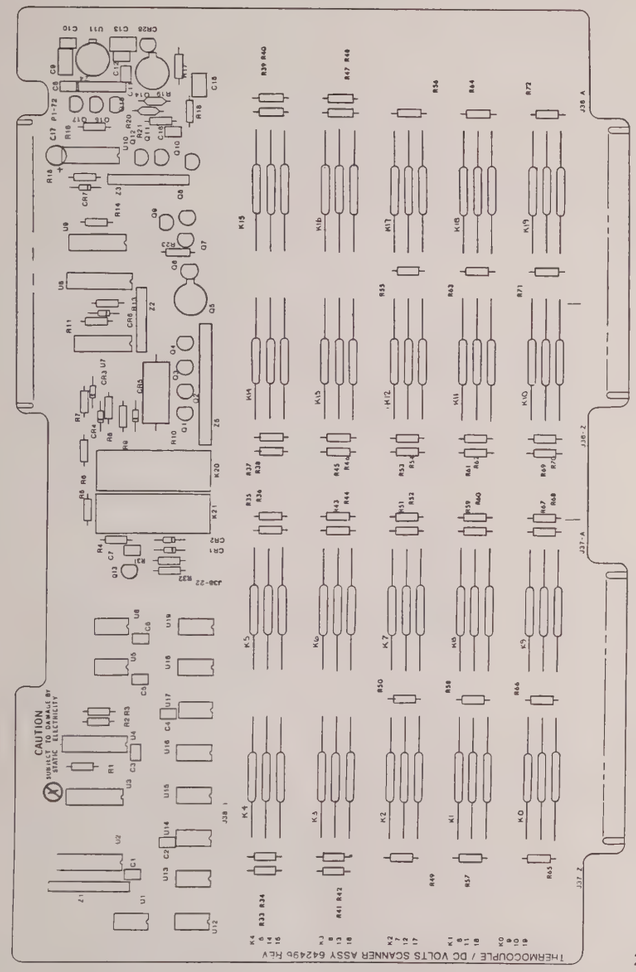
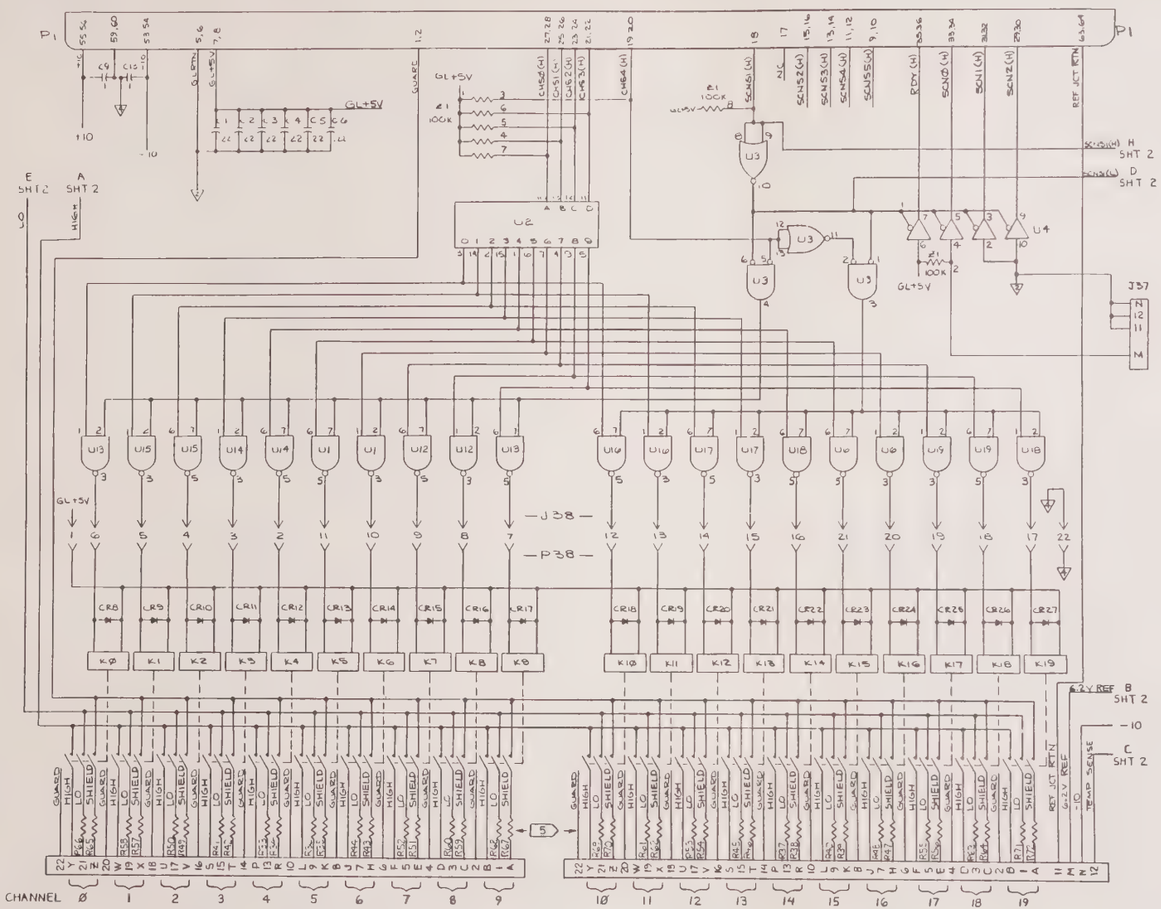


Figure 162-2. 2280A-162 Thermocouple/DC Volts Scanner PCA



2280A-1662



NOTES: UNLESS OTHERWISE SPECIFIED

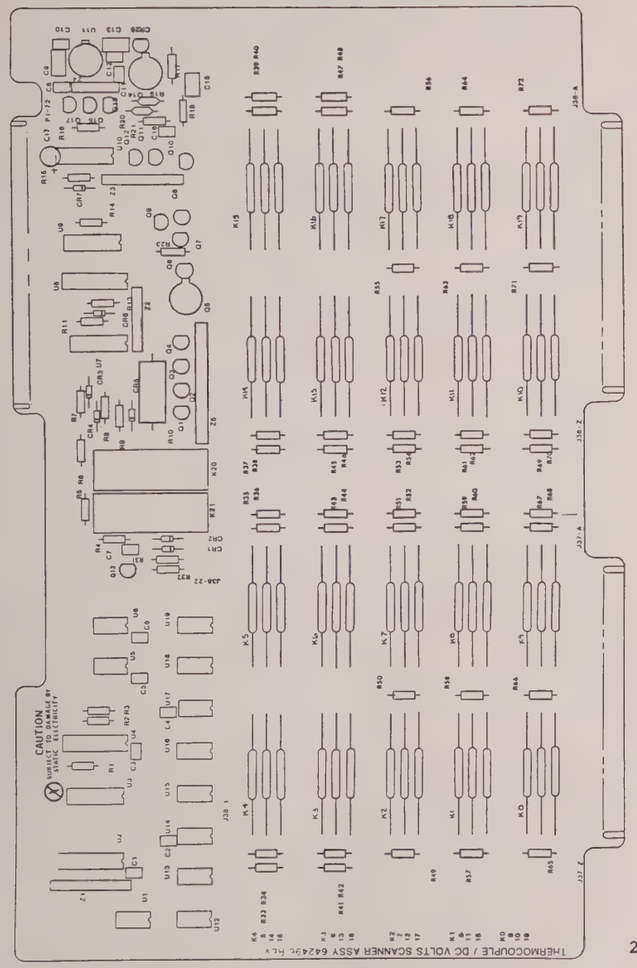
1. RESISTANCE IS IN OHMS, CAPACITANCE IS IN MICROFARADS.
2. ALL RESISTORS ARE 1/4W, 5%.
3. ALL GRAPHIC SYMBOLS ARE IN ACCORDANCE WITH ANSI Y32.2 AND Y32.14.

5. R33 - R72; ALL RESISTORS CONNECTED TO LO ARE 150Ω, ALL RESISTORS CONNECTED TO SHIELD ARE 470Ω.

IC POWER AND GROUND					
REF DES	⏚	GL+5V	+10V	-10V	VG
U1,5,6,12,-12	4	8			
U2	8	16			
U3	7	14			
U4	2,8,10,14	6,12,16			
U7			3	10-13	
U8	8	16			
U9,10			3	12	
U11			7	4	
Z2,3					1

2280A-1062

Figure 162-2. Thermocouple/DC Volts Scanner Schematic Diagram



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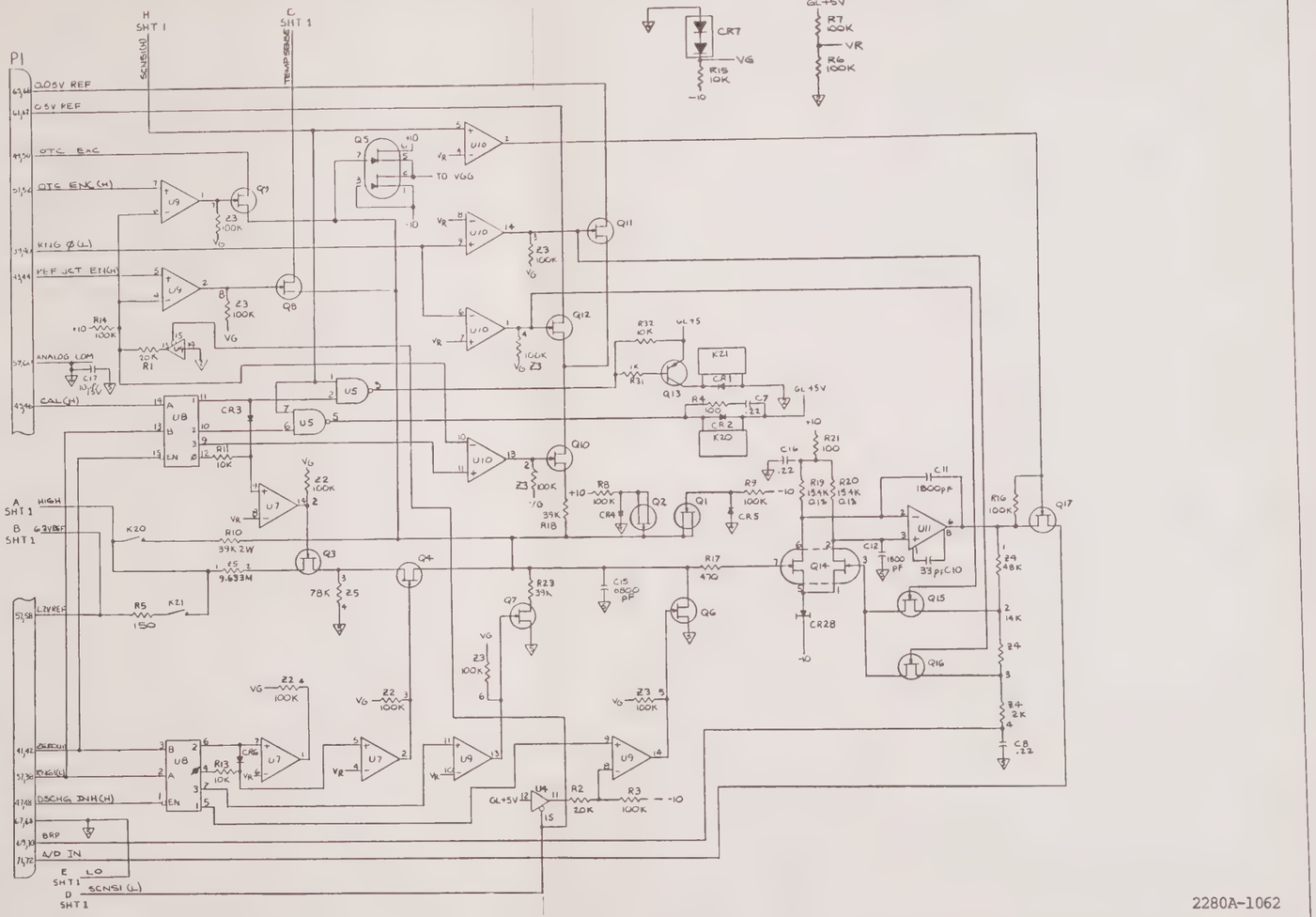


2280A-1062

Figure 162-2. Thermocouple/DC Volts Scanner Schematic Diagram (cont.)

Option 2280B-163
RTD/Resistance Scanner

DESCRIPTION

The RTD/Resistance Scanner multiplexes 20 input channels, with 3 or 4 poles per channel, and makes them available in sequence to the A/D Converter. Option 2280B-177, the RTD/Resistance Input Connector, is used with the RTD/Resistance Scanner to provide connection terminals for the external wiring.

WHERE TO FIND FURTHER INFORMATION

In this subsection are RTD/Resistance Scanner theory of operation, general maintenance, performance tests, calibration procedure, a guide to troubleshooting, a parts list, and a schematic diagram. Installation and system configuration instructions are in the 2280 Series System Guide, and operating and programming instructions are in the 2280 Series User Guide. Option specifications are in the Appendices in this manual and the System Guide.

Test equipment required to perform the procedures in this subsection is listed in Table 163-1. A summary of test equipment required for all procedures in this manual is given in Table 1-1 in Section 1 of this manual.

Table 163-1. Required Test Equipment

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
A/D Converter	.....	Fluke Option 2280A-161 rev E-2, F-1, G-1, H-1, or newer (no substitute)
RTD/Ohms Input Connector	.....	Fluke Option 2280B-177 (no substitute)
Resistors R1 - R3	100ohm, 0.01%, 5ppm/C hermetically sealed wirewound	Fluke Part #491720
Resistors R4, R5	100ohm, 0.1%, T9 metal film	Fluke Part #357400
Toggle Switch	SPDT	Fluke Part #493825

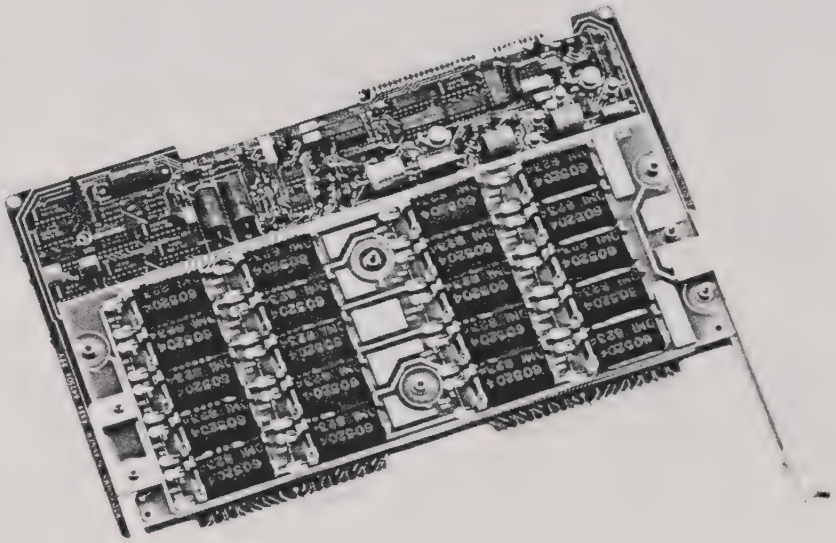


Figure 163-1. The RTD/Resistance Scanner

THEORY OF OPERATION

The following theory of operation discussion begins with an overall functional description of the RTD/Resistance Scanner, followed by a block diagram description. A detailed circuit analysis then describes how each major circuit block on the RTD/Resistance Scanner assembly works. Where necessary, block diagrams and simplified schematics are included with the text. Schematic diagrams for the RTD/Resistance Scanner are at the end of this option subsection.

Overall Functional Description

The RTD/Resistance Scanner assembly and its companion input connector (Option 2280B-177) work together with an Option 2280A-161 A/D Converter to measure resistance inputs with high accuracy and stability. Power for the scanner is supplied as +/- 10 volts and + 5 volts from the A/D Converter.

When instructed by the Controller, the RTD/Resistance Scanner selects and conditions one of 20 channels. A resistance to be measured is selected by reed relays and excited by one of two current levels, and one of two amplifier gains is chosen to condition the resulting voltage in preparation for conversion by the A/D.

Compensation is provided for the two 3-wire modes of operation: 3-Wire Accurate (3WA) and 3-Wire with Common Mode (3WCM). Also, reed resistance errors are eliminated in the 4-Wire (4W) and 3-Wire Accurate (3WA) modes. Auto-zero and auto-calibration features are incorporated for use by the A/D, and three measurement ranges, 256 ohms, 2048 ohms, and 64 kohms full scale are included in the RTD/Ohms Scanner. One operation mode is selected by two jumpers for all 20 channels on each scanner, while ranges for each channel are selected by the 2280B mainframe.

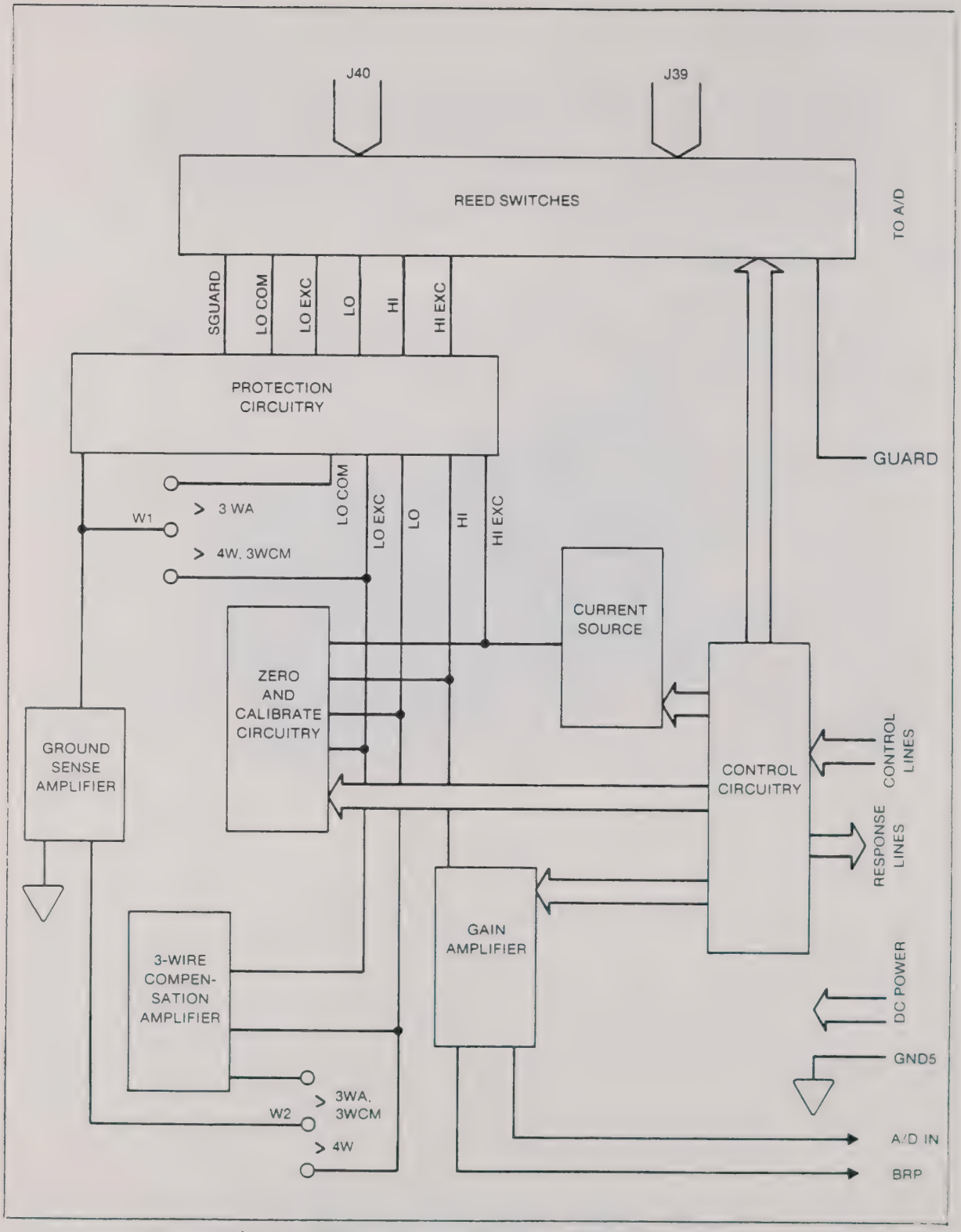


Figure 163-2. RTD/Resistance Scanner Block Diagram

REED SWITCHES

Reed switches provide high voltage isolation from channel to channel and scanner to scanner. Each input channel is connected to scanner circuitry by four reed switches driven by a single drive coil. An additional individual reed relay, K21 or K22, pulls in to provide a common current-return path for the decade of channels that the channel selected resides in, eliminating reed resistance errors in the 3-Wire Accurate (3WA) mode of operation. One more individual reed relay, K20, connects the A/D Converter guard to a LO line whenever the scanner is selected by the A/D Converter.

Figure 163-3 shows one channel of reed switches, with the components used in other channels listed in parentheses. The reeds for one channel, Sxx-A,B,C,D, are pulled in by the corresponding drive coil Kxx, while K21 or K22 is pulled in at the same time to provide the LO COM return for a decade of channels in the 3WA mode of operation. Relay K20 is pulled in whenever the scanner is selected by the A/D, connecting the A/D guard to LO of the resistance being measured through K20 and the LO COM or LO EXC reed switches.

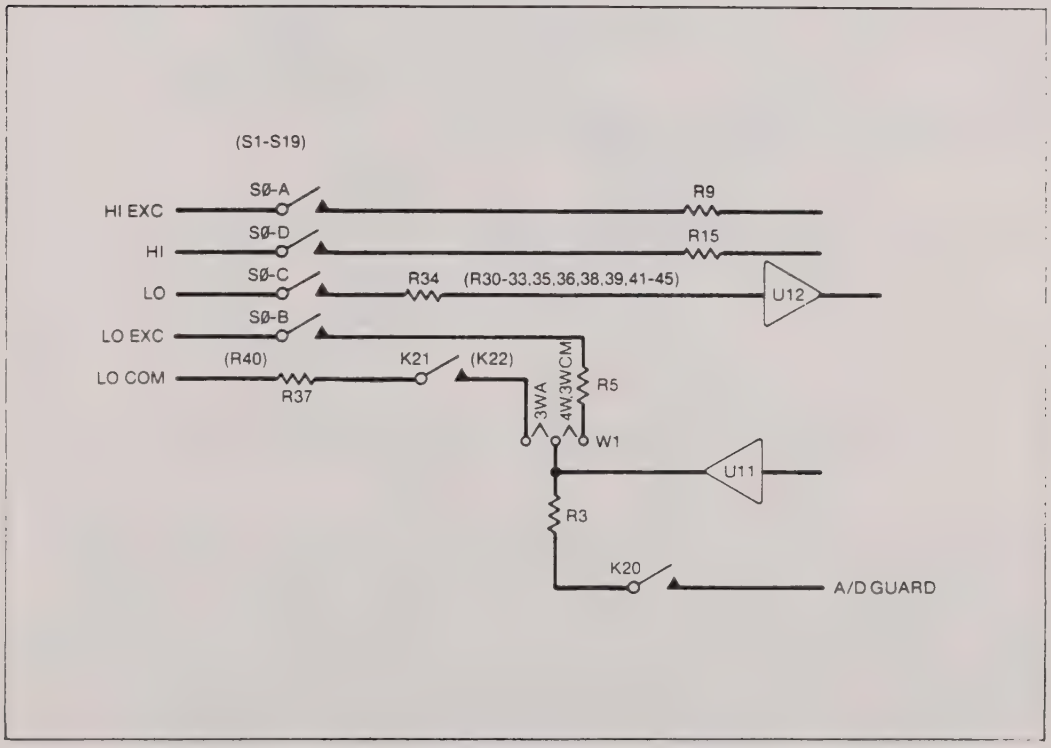


Figure 163-3. One Reed-Switch Channel

PROTECTION CIRCUITRY

To protect scanner and A/D circuitry, channel inputs are isolated, energy limited, and diode clamped. Figure 163-4 shows a schematic diagram of the protection circuitry.

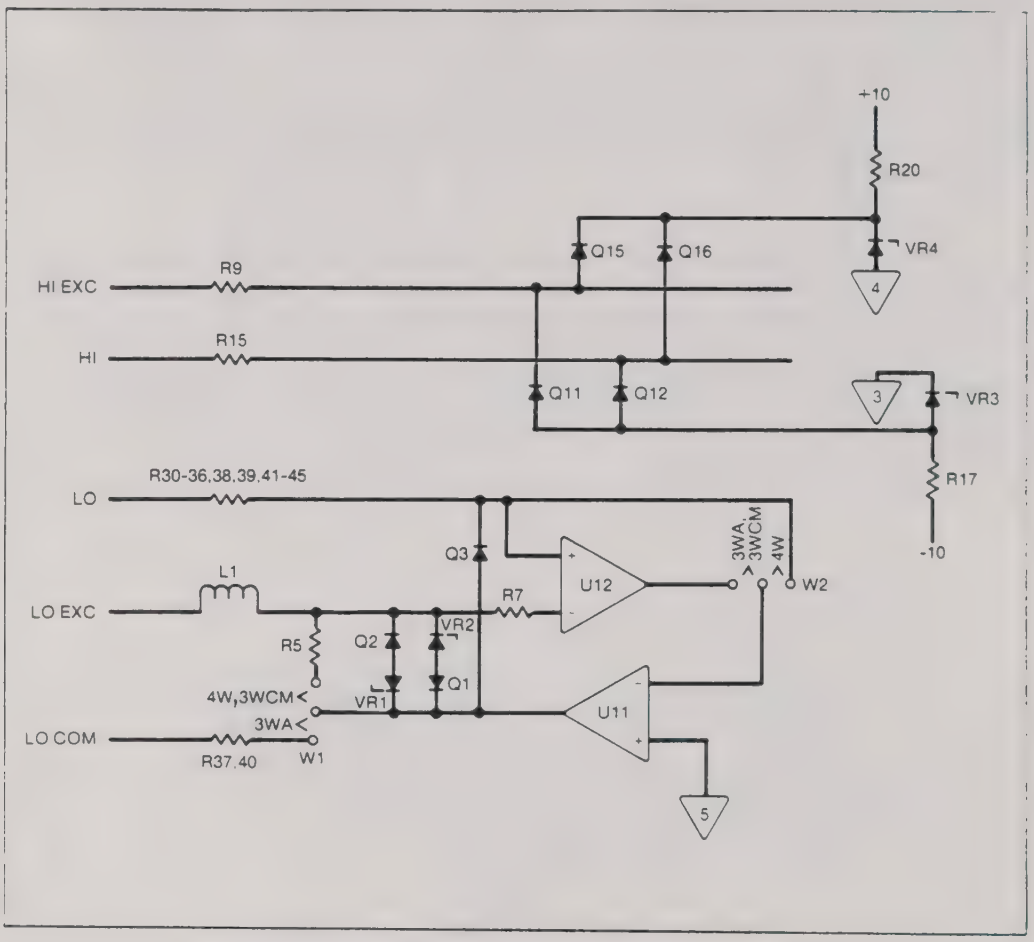


Figure 163-4. Protection Circuitry

Here, input terminals are clamped to defined voltages through series resistances. A positive clamp voltage of approximately 3 to 5 volts is provided by VR4, which is biased by R20, while a negative voltage is provided by VR3, which is biased by R17. R9 dissipates overvoltages to the HI EXC terminal in combination with Q15 and VR4 or Q11 and VR3. Both Q15 and Q11 are reverse biased in normal operation. R15 dissipates overvoltages to HI, passing current through Q16 or Q12, which are reverse biased in normal operation. LO terminals are protected by series resistors R30-36, R38, R39, and R41-45, and by the input protection diodes of U11 and U12, and Q3. L1 slows down fast transient voltages entering LO EXC terminals, while VR1, VR2, Q1, and Q2 clamp LO EXC to LO COM through W1 in the 3WA mode of operation, with R37 and R40 limiting current and dissipating power. R7 also serves to limit LO EXC current into the input of U12.

GAIN AMPLIFIER

This circuit filters and amplifies the signal on the HI terminal. The gain is set to 8 for the 256 ohm range, and unity for the other two ranges. One input filter is used with the high ohms range, while the other is used with the 256 ohm and 2048 ohm ranges. The scanner output is enabled whenever the scanner is selected by the A/D.

Figure 163-5 is a schematic diagram of the gain amplifier. Two voltage gains are provided by U20 and associated components, with the output to the A/D enabled by turning on Q23. Q25 sets the gain at unity, while Q26 and Z4 set the gain at 8.00. BRP, which stands for beta return path, returns currents flowing through Z4 to the A/D, and C16 shunts ac signals on BRP to Ground 5. The resistance being measured plus R15, and C15 provide noise filtering of the HI input for the 64 kohm range, with C14 switched in parallel with C15 by Q24 for the two lower resistance ranges. The VHG amplifier, U21, drives guard traces surrounding all HI circuit traces to prevent leakage under high humidity conditions.

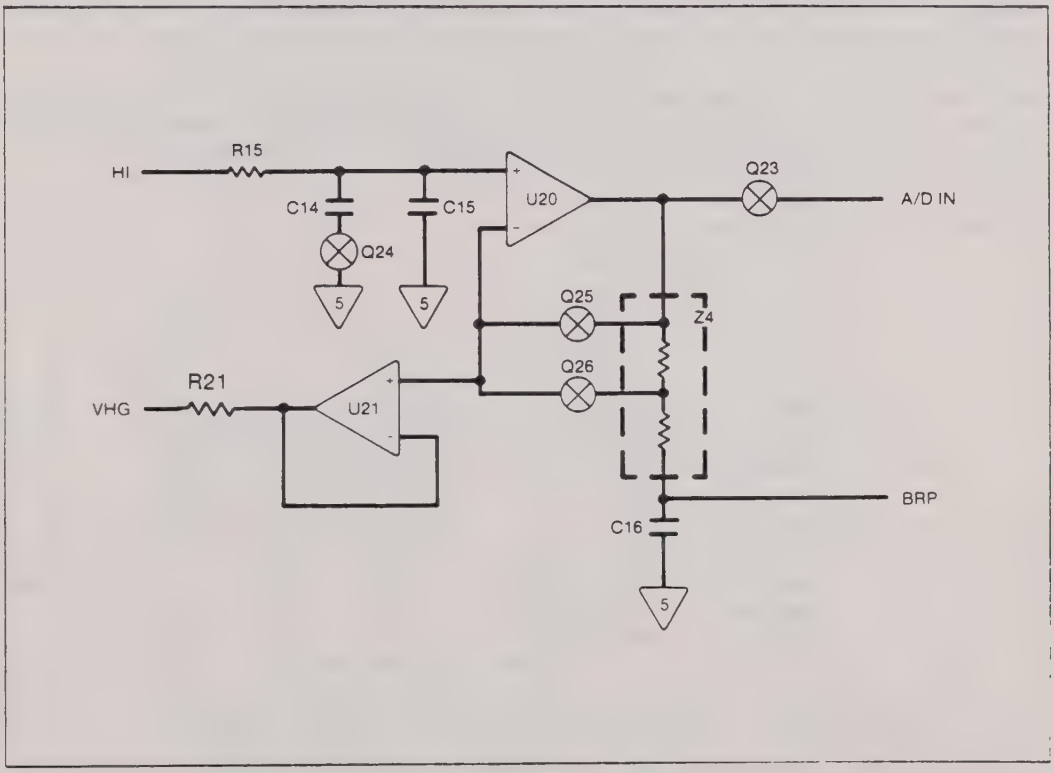


Figure 163-5. Gain Amplifier

CURRENT SOURCE

Two zener-referenced current outputs can be set by the current source circuitry, with one of the two selected at all times. The 256 ohm and 2048 ohm ranges use the 1.0 mA output, and the 64 kohm range uses the 32 uA output. The 32 uA output can be set to another value by changing a precision resistor if a larger full scale value than 64 kohms is desired.

A simplified schematic of the current source is shown in Figure 163-6. As can be seen in the schematic, this circuit is centered around a stable voltage reference and precision resistances. A potential 6.2 volts below the +10 volt rail is generated by the zener reference set composed of VR5, R23, and R24, and this is then divided down to 5.00 volts below the rail by Z4. Range selection is provided by Q20 and Q27 which select R25 for a 1mA current, and Q21 and Q22 which select R19 for a 32 uA (standard) current. U23 compares the voltage across R24 or R19 to the 5 volt reference and enhances the gate of Q19 the necessary amount to bring equilibrium to the circuit. Q19 then passes the current through R9 to the HI EXC reed switches. The VRG amplifier, U22, provides guard drive to traces that prevent leakage out of or into the circuit nodes that sit at the +5 volt potential, while the VSG amplifier, U16, provides guard drive to traces which prevent leakage out of the circuitry at the potential of the drain of Q19. Capacitors C10 and C17 stabilize U16 and U22 respectively in their unity-gain configuration.

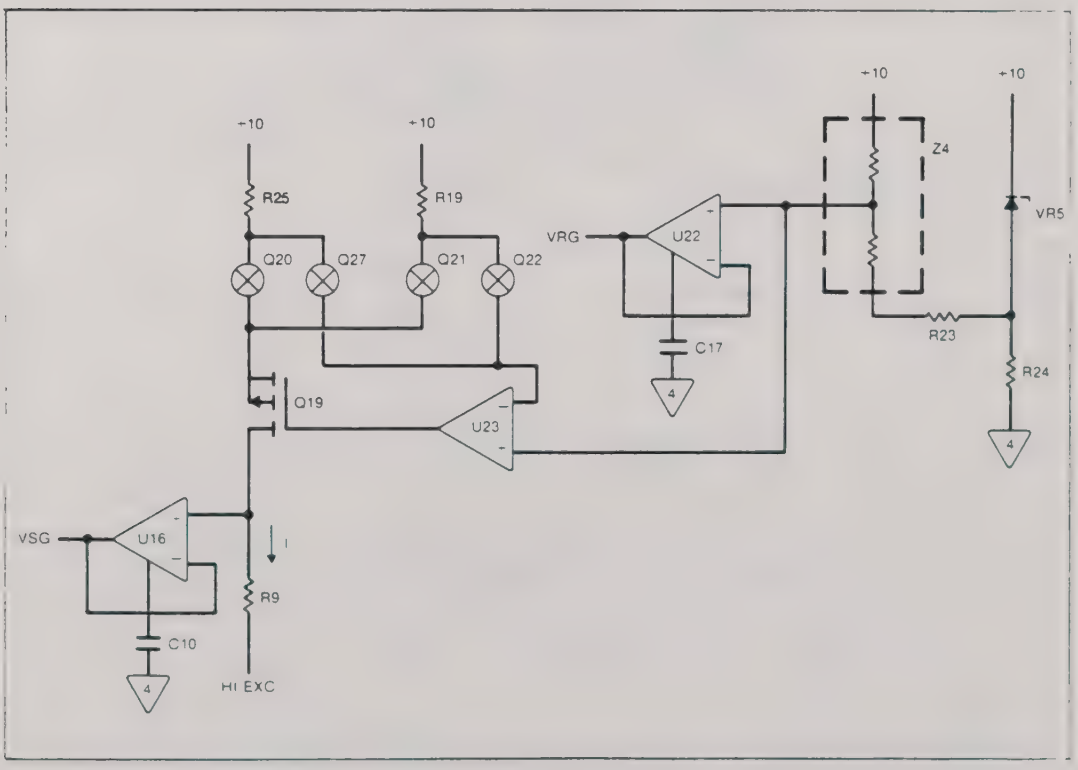


Figure 163-6. Current Source

GROUND SENSE AMPLIFIER

This amplifier sets LO to a potential that allows the A/D to make readings of HI with respect to ground. In 4-wire mode, it compares LO to the analog ground 5, and in 3WA and 3WCM modes it compares the output of the 3-wire compensation amplifier to analog ground. To set LO at the desired voltage level, the amplifier pulls the necessary current through LO EXC in 4-wire and 3WCM modes, or LO COM in the 3WA mode.

Refer to the simplified schematic, Figure 163-7. The ground sense amplifier, as part of the measurement circuit, senses the potential at LO, or the output of U12, and sets it to analog ground 5 potential, thereby allowing the A/D, which does not have a differential input, to make measurements with respect to ground. U11, in response to the inputs, pulls current through R5 and LO EXC or LO COM, depending on the setting of W1. Capacitor C4 in combination with R4 or R30-36, R38, R39, or R41-45 roll off the gain of U11 to reduce out-of-band noise, and C5 reduces the noise sensitivity of U11.

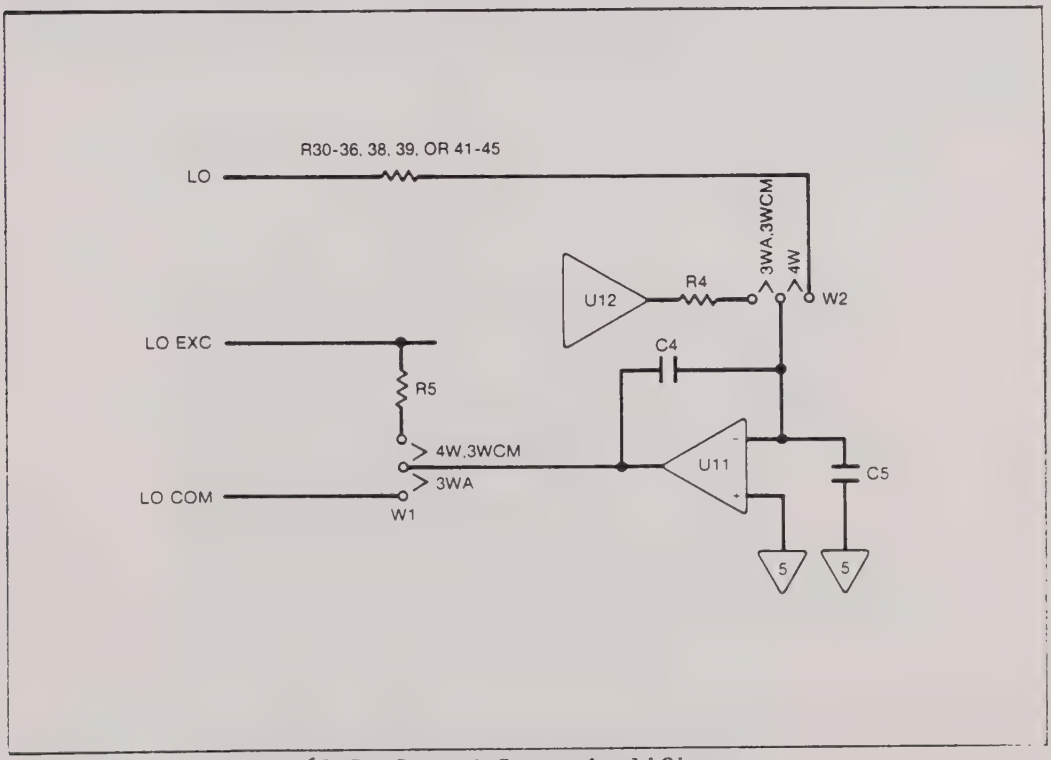


Figure 163-7. Ground Sense Amplifier

3-WIRE COMPENSATION AMPLIFIER

The output of this amplifier is selected when W2 is set to the 3WA and 3WCM position. The voltage difference between LO and LO EXC is measured to determine the lead wire voltage drop, and the output of the compensation amplifier is set to that one lead wire drop above the LO potential. The ground sense amplifier sets the output of the compensation amplifier to ground potential, setting LO to one lead wire voltage drop below ground, and thereby compensating for the HI lead wire drop.

Refer to Figure 163-8, the simplified schematic, for the following discussion. In the two 3-wire modes of operation, U12 measures the lead wire voltage drop between LO and LO EXC (Vrl), with R7 and R6 setting the gain at -1, so that the U12 output is +Vrl, or one lead wire drop, above LO. U11 senses this output, and pulls current through LO COM or LO EXC until the U12 output is set at ground potential, thereby setting LO at -Vrl or one lead wire drop below ground to compensate for the lead wire drop in the HI lead. R4 and C4 stabilize the compensation amplifier loop and roll off the gain for frequencies that are not of interest, and the resistors in the LO path plus C6 and R7 reduce the noise sensitivity of U12.

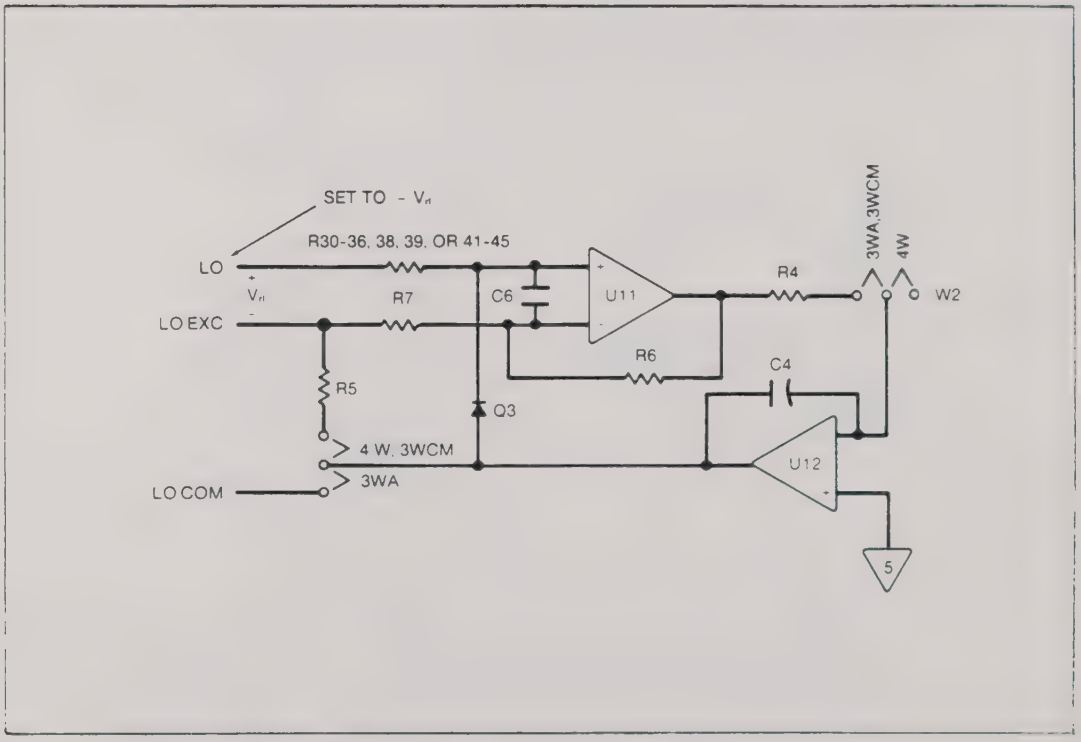


Figure 163-8. 3-Wire Compensation Amplifier

ZERO CIRCUITRY

The zero circuitry, which is enabled by the A/D, configures the scanner so that readings can be made which will allow the A/D to subtract zero errors from all channel measurements. The circuitry is enabled at the start of each scan, giving direct readings of voltage and current offsets on the 256 ohm and 64 kohm ranges. The 2048-ohm range zero reading is calculated by dividing the 256 ohm range zero reading by 8.

Refer to Figure 163-9, the simplified schematic, for the following discussion. To allow the A/D to make zero readings, Q5 and Q7 close the loop around U11 and U12 so that voltage errors appear at the output of U11, and Q6 then connects the U11 output to the gain amplifier, U20. Q4 is turned on to connect the current source to U11 and keep the zero measurements consistent with channel measurements. The resistances of R8 and R10 add to the "on" resistances of Q5 and Q6 to cancel bias current shifts generated by the series resistances present in the HI and LO input lines when making channel readings.

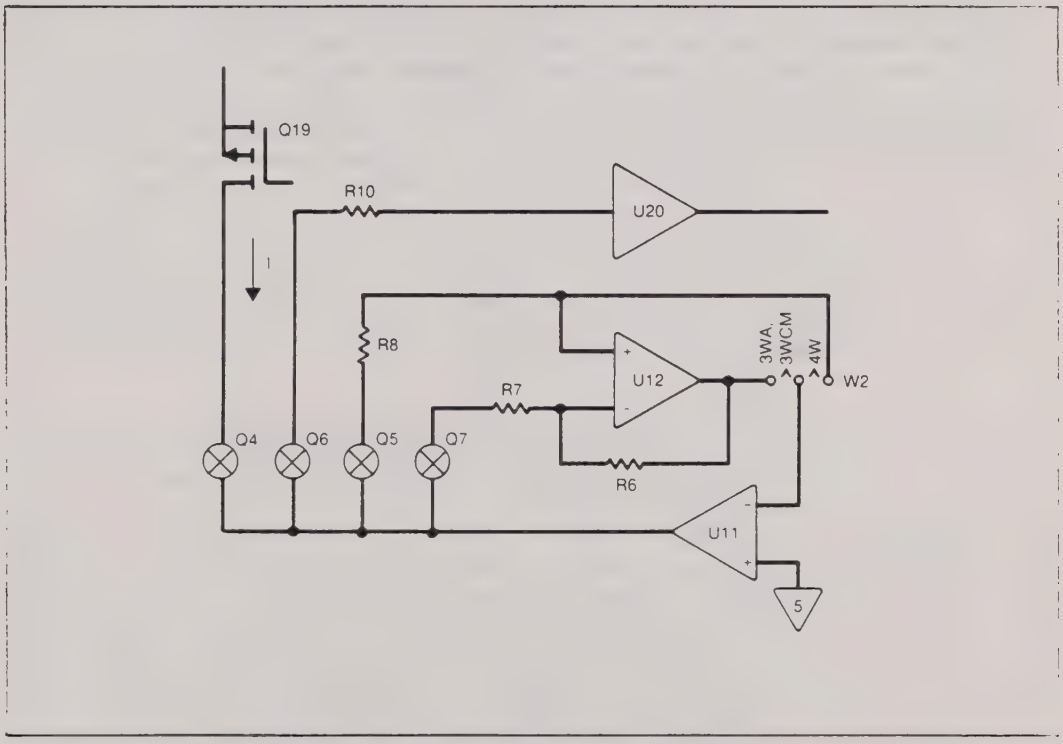


Figure 163-9. Zero Circuitry

The calibrate circuitry is enabled by the A/D once every ten minutes, or on command, and the subsequent calibrate readings are used to calculate gain correction factors used by the A/D when making channel readings. Three precision resistors located on the scanner are measured and used as references for the three ranges. The voltages expected by the 2.048 volt full scale A/D during calibrate are: 1.600 volts on the 256 ohm range, 2.000 volts on the 2048 ohm range, and 1.5872 volts on the 64 kohm range. If a larger full scale than 64 kohms is desired, one of the precision reference resistors must be changed.

Figure 163-10 is a simplified schematic of the calibrate circuitry. To close the loop around U11 and U12 in a way that bias current and offset voltage errors are included in the calibrate readings, Q7 and Q8 are turned on. U11 pulls current through Q7, setting the lower ends of R14, R16, and R18 at the proper potential near ground. During a 256 ohm range calibrate, Q10 supplies current to reference resistor R14, and Q9 switches in the gain amplifier, U20, to make a measurement. During a 2048 ohm range calibrate, Q14 supplies current to R16, and Q13 switches in U20, and during a 64 kohm range calibrate, Q18 supplies R18, with Q17 switching in U20. Resistors R8 and R10 are included to cancel the primary shifts in readings made by U11, U12 and U20 bias currents.

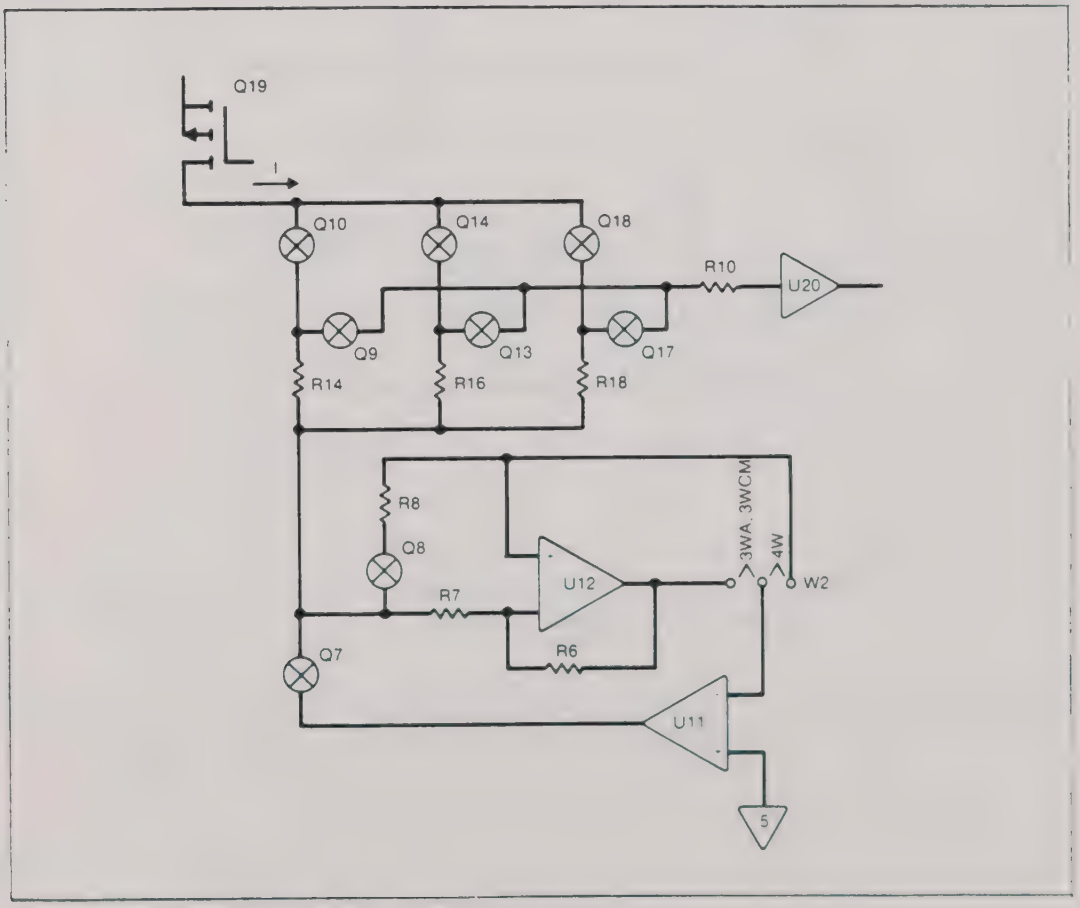


Figure 163-10. Calibrate Circuitry

CONTROL CIRCUITRY

This primarily CMOS and open-collector comparator circuitry decodes the A/D control signals and controls scanner operation. It selects and drives the reed coils, turns on zero and calibrate circuitry, sets the gain of the gain amplifier, and sets the output of the current source when directed by the A/D. It also sends the proper configuration code back to the A/D, asserts RDY (ready), and turns on the scanner output when the scanner is selected.

Figure 163-11 shows a simplified schematic of the scanner control circuitry. The first section of control circuitry asserts the RDY(H) and SCN[0:2](H) lines with U14 whenever SCNS1 is asserted by the A/D. This indicates to the A/D that the scanner is ready to make readings, and that it is an RTD/Ohms scanner.

A second section of control circuitry decodes and provides reed relay coil drive. U5 turns on K20 to connect the A/D Guard whenever the scanner is selected by SCNS1. U1 selects the 4 to 10 decoder needed to match the CHS4 line, and locks out the other decoder by asserting the two high bits of the unneeded one. When the scanner is not selected by SCNS1, the two high bits of both U3 and U6 are asserted, preventing both decoders from enabling any of their output lines. U2 passes either the lockout control lines, or the CHS2 and CHS3 channel select lines to U3 and U6. When U3 is selected, one gate of U9 instructs U8 to pull K21 in, completing the LO COM path for channels 0 through 9, while when U6 is selected, U9 has U8 pull K22 in, completing the LO COM path for channels 10 through 19. When a channel is selected by the SCNS1 and CHS[0:4] lines, U3 or U6 drive the base of an NPN transistor residing in arrays U4, U7, or U10, which switches on, driving the proper reed relay coil, and closing the 4 (A through D) channel reeds.

The third block of scanner control circuitry enables FET transistor switches to select the scanner functions and configurations. Logic ICs U14, U17, and U18 decode 5 control lines from the A/D; ZERO(H), CAL(H), RNG0(L), RNG1(L), and SCNS1(H), plus SCNS1(L) generated by U9. When SCNS1 is de-asserted and the scanner is not selected, zero mode is configured, while the current source range is set by the RNG1 line. Outputs of the logic gates are sent to comparators U13, U15 and U19 where they are compared to a 2.5 volt reference generated by R1 and R2. The Boolean expressions are written above each control line leading to the comparators. The comparator outputs then drive the gates of the FET transistors and perform the specific functions listed. All N-channel JFET transistors are pulled up to VG, a voltage set by CR4 and R13, through 100 kohm pull-up resistors which are not shown. For example, asserting CAL and SCNS1 causes U13 to turn on Q8, helping to place the scanner in a calibrate configuration.

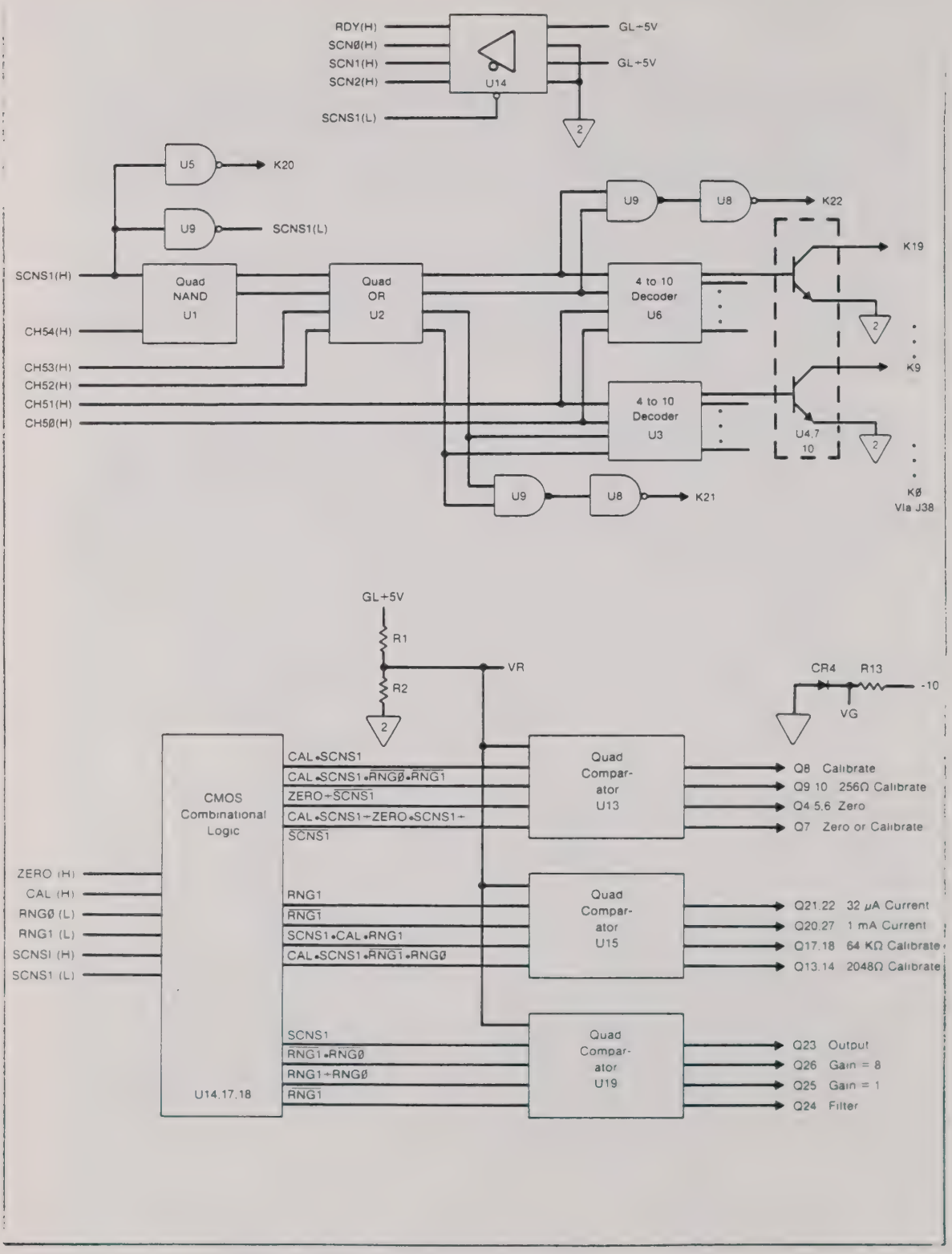


Figure 163-11. Control Circuitry

GENERAL MAINTENANCE

The RTD/Resistance Scanner PCA normally does not require cleaning, but if dirt, dust, or other contamination is visible on the surface, the PCA should be cleaned. Follow PCA cleaning instructions in Section 4.

PERFORMANCE TESTS

The following performance test procedures verify that the RTD/Ohms Scanner is operating properly and meets specifications in all three modes and all three operating ranges. Equipment required to perform the following tests is listed in Table 163-1.

Performance Test Preparation

1. Wire the input connector as shown in Figure 163-12, with all connections to R1, R2, and R3 made to the resistor leads.

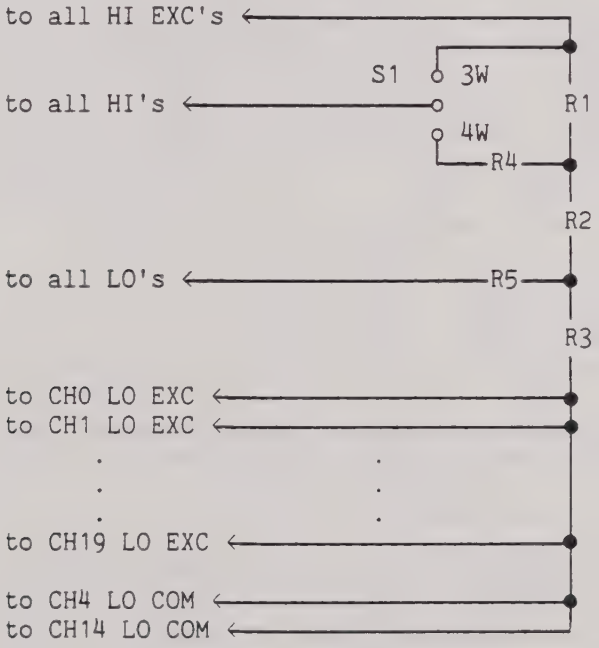


FIGURE 163-12. Test Input Connector Schematic

3. Set the A/D Converter (2280A-161) address selector switch to 3.
4. Install the A/D Converter in the 2280B.
5. Set W1 and W2 of the UUT (2280B-163) for 4W operation.
6. Install the UUT in the slot directly below the A/D Converter.

7. Set S1 of the Test Input Connector to the 4W position.

8. Install the Test Input Connector on the back of the UUT.

Serial Link Communication Test

1. Turn the 2280B keyswitch to the Program position.

2. Ensure that the 2280B Printer ON/OFF switch is ON.

3. Perform a List Configuration as instructed in Table 163-2.

Table 163-2. List Configuration Response Test

STEP	KEYSTROKE(S)	RESULTING DATA LOGGER PROMPT
1	--	MAIN MENU CHOICE <M FOR MENU>? A
2	L	<L> LIST PROGRAM AND CONFIGURATION
3	ENTER	L: LIST MENU CHOICE <A-Z>? E
4	C	L<C> LIST HARDWARE CONFIGURATION
5	ENTER	=> printer will print the list
6	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

4. Verify that the following printout is obtained:

```
BEGINNING CHANNEL NUMBER = 300
TYPE = RTD
BEGINNING CHANNEL NUMBER = 310
TYPE = RTD
```

If a beginning channel number is not obtained, check the A/D (-161)
If the type is not RTD, check the RTD/Ohms scanner (-163)

256-Ohm Range, 4-Wire Mode Test

1. Ensure that the UUT W1 and W2 jumpers are set for 4W operation.

2. Ensure that the Test Input Connector switch S1 is set to 4W.

3. Program the 2280B as shown in Table 163-3.

Table 163-3. 256 Ohm 4-Wire Test

STEP	KEYSTROKE(S)	RESULTING DATA LOGGER PROMPT
1	--	MAIN MENU CHOICE <M FOR MENU>? A
2	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
3	C300..319	CHANNEL NUMBER (OR BLOCK) = C300..319
4	ENTER	PROGRAM COPY DELETE OR LIST (P,C,D,L)? P
5	ENTER	A: CHANNEL FUNCTION <A-Z>? P
6	Z	A<Z> RESISTANCE
7	ENTER	AZ: RESISTANCE RANGE <1-5>? 1
8	3	AZ<3> 256.00 OHMS RTD SCANNER
9	ENTER	AZ: CHANNEL MENU CHOICE <1-5>? 1
10	5	AZ<5> LOGGING FORMAT
11	ENTER	AZ5: LOGGING FORMAT <1-7>? 4
12	4	AZ5<4> NN.NNN
13	ENTER	AZ: CHANNEL MENU CHOICE <1-5>? 1
14	EXIT	A: CHANNEL FUNCTION <A-Z>? Z
15	EXIT	CHANNEL NUMBER (OR BLOCK) = C300..319
16	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

3. Enter Monitor mode as shown in Table 163-4, and read the channels by monitoring each channel.

Table 163-4. Entering Monitor Mode.

STEP	KEYSTROKE(S)	RESULTING DATA LOGGER PROMPT
	--	MAIN MENU CHOICE <M FOR MENU>? A
	MONITOR	MONITOR CHANNEL = C0
	300	MONITOR CHANNEL = 300
	ENTER	=> display shows the measurements for channel 300

4. Press the period <.> to calibrate the A/D Converter.

5. Verify that the reading is between 99.964 and 100.036 ohms.

6. Increment the channel using the up arrow.

7. Repeat steps 5 and 6 until all 20 channels have been checked.

8. Press the MONITOR key to return to the main menu

2048-Ohm Range, 4-Wire Mode Test

1. Ensure proper UUT and Test Connector configuration.

2. Ensure that the UUT W1 and W2 jumpers are set for 4W operation.

3. Ensure that the Test Input Connector switch S1 is set to 4W.

4. Program the 2280B the same as in Table 163-3 with the exception of the two steps listed in Table 163-5.

Table 163-5. 2048 Ohm, 4-Wire Test Step Changes.

STEP	KEYSTROKE(S)	RESULTING DATA LOGGER PROMPT
8	4	AZ<4> 2048.0 OHMS RTD SCANNER
and		
12	5	AZ5<5> NNN.NN

5. To read and monitor each channel:

   a. Enter Monitor mode as in Table 163-4.
   b. Press the period <.> to calibrate the A/D.
   c. Verify that the reading is between 99.93 and 100.07 ohms.
   d. Increment the channel using the up arrow.
   e. Repeat steps c and d until all 20 channels have been checked.
   f. Press the MONITOR key to return to the main menu.

64-Kohm Range, 4-Wire Mode Test

1. Ensure proper UUT and Test Connector configuration.

2. Ensure that the UUT W1 and W2 jumpers are set for 4W operation.

3. Ensure that the Test Input Connector switch S1 is set to 4W.

4. Program the 2280B the same as in Table 163-3 with the exception of the two steps listed in Table 163-6.

Table 163-6. 64 KOhm 4-Wire Test Step Changes.

STEP	KEYSTROKE(S)	RESULTING DATA LOGGER PROMPT
8	5	AZ<5> 64.000 KOHMS RTD SCANNER
and		
12	2	AZ5<2> N.NNNN

3. To read and monitor each channel:

   a. Enter Monitor mode as in Table 163-4.
   b. Press the period <.> to calibrate the A/D.
   c. Verify that the reading is between 0.0987 and 0.1013 kohms.
   d. Increment the channel using the up arrow.
   e. Repeat steps c and d until all 20 channels have been checked.
   f. Press the MONITOR key to return to the main menu.

256-Ohm Range, 3WA-Mode Test

1. To set the jumpers on the UUT:

    a. Switch the 2280B power OFF and remove the UUT.
    b. Set W1 and W2 of the UUT for 3WA operation.
    c. Set S1 of the Test Input Connector to the 3W position.
    d. Re-install the UUT in the slot below the A/D (-161).
    e. Switch the 2280B to the Program position.

2. Program the 2280B the same as in Table 163-3.

3. To read and monitor each channel:

    a. Enter Monitor mode as in Table 163-4.
    b. Press the period <.> to calibrate the A/D.
    c. Verify that the reading is between 99.743 and 100.257 ohms.
    d. Increment the channel using the up arrow.
    e. Repeat steps c and d until all 20 channels have been checked.
    f. Press the MONITOR key to return to the main menu.

256-Ohm Range, 3WCM-Mode Test

1. To set the jumpers on the UUT:

    a. Switch the 2280B power OFF and remove the UUT.
    b. Set W1 and W2 of the UUT for 3WCM operation.
    c. Set S1 of the Test Input Connector to the 3W position.
    d. Re-install the UUT in the slot below the A/D (-161).
    e. Switch the 2280B to the Program position.

2. Program the 2280B the same as in Table 163-3.

3. To read monitor each channel:

    a. Enter Monitor mode as in Table 163-4.
    b. Press the period <.> to calibrate the A/D.
    c. Verify that the reading is between 99.150 and 100.850 ohms.
    d. Increment the channel using the up arrow.
    e. Repeat steps c and d until all 20 channels have been checked.
    f. Press the MONITOR key to return to the main menu.

This completes the 2280B-163 Verification Test.

CALIBRATION

The RTD/Resistance Scanner does not require calibration adjustments.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the RTD/Resistance Scanner is given in Table 163-7. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the RTD/Resistance Scanner is given in Figure 163-13.

TABLE 163-7. 2280B-163 RTD/RESISTANCE SCANNER PCA
(SEE FIGURE 163-13.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOT -E
C 1- 3, 7,		CAP,POLYES,0.22UF,+-10%,50V	696492	89536	696492	7		
C 8, 11, 12			696492					
C 4, 14		CAP,POLYPR,0.047UF,+-10%,100V	446773	89536	446773	2		
C 5, 16		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	2		
C 6		CAP,CER,0.001UF,+-20%,100V,X7R	402966	72982	8121-A100-W5R-102M	1	1	
C 9, 13		CAP,TA,10UF,+-20%,15V	193623	56289	196D106X0015A1	2		
C 10, 17		CAP,CER,100PF,+-2%,100V,COG	512848	51406	RPE121	2		
C 15		CAP,POLYPR,470PF,+-5%,50V	740464	89536	740464	1		
CR 1- 4, 8-	*	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	24	1	
CR 27	*		203323					
H 1		SCREW,MACH,PHP,S STL,4-40X3/4	681973	89536	681973	1		
H 2		NUT,HEX,S.STL,4-40	147611	89536	147611	1		
H 3		WASHER	147603	89536	147603	6		
H 4		WASHER	195354	89536	195354	6		
H 5		WASHER	146225	89536	146225	6		
J 38		CONN,POST,PWB,.025SQ,NON-INSUL,GOLD30	513861	00779	1-87022-7	22		
K 0- 19		RELAY COIL ASSY	605204	89536	605204	20		
K 20- 22		RELAY,REED,1 FORM A,5VDC	520247	71707	UF-40115	3		
L 1		INDUCTOR,0.15 UH,+/-10%,400MHZ,SHLDED	256297	24759	MR0.15	1	1	
MP 2		SPACER,REED	617415	89536	617415	1		
MP 3		SPACER,SWAGED,RND,BRASS,0.125IDX0.187	436675	89536	436675	5		
MP 4		SPACER,SWGD,RND,BRASS,0.150IDX0.125	335075	89536	335075	1		
MP 5		BAG,SHIELDING,TRANSPARENT,12"X16"	680983	89536	680983	1		
MP 6		BOTTOM GUARD	579151	89536	579151	1		
MP 7		PCB RETAINER	579078	89536	579078	2		
MP 8		INSULATOR, BOTTOM	579102	89536	579102	1		
P 38		CONN,PWB,REC,BOARD MOUNT,1/16 THICK	267476	00779	85861-2	22		
Q 1- 18, 23-	*	TRANSISTOR,SI,N-JFET,TO-92	376475	15818	U2810J	22		
Q 26	*		376475					
Q 19- 22, 27	*	TRANSISTOR,SI,P-MOS,ENHANCEMENT,TO-72	741058	89536	741058	5	5	
R 1, 2, 17,		RES,CF,100K,+-5%,0.25W	348920	80031	CR251-4-5P100K	5		
R 21, 25			348920					
R 3		RES,CC,330,+-5%,0.25W	147967	01121	CB3315	1		
R 4, 15, 30-		RES,MF,4.99K,+-1%,0.125W,100PPM	168252	91637	MFF1-84991	16		
R 36, 38, 39,			168252					
R 41- 45			168252					
R 5		RES,CC,100,+-5%,0.25W	147926	01121	CB1015	1		
R 6, 7		RES,MF,10K,+-0.1%,0.125W,25PPM	435065	89536	435065	2		
R 8, 10		RES,MF,4.75K,+-1%,0.125W,100PPM	260679	91637	CMF554751F	2		
R 9		RES,CC,910,+-5%,0.5W	170704	89536	170704	1		
R 11- 13		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	3		
R 14		RESISTOR,WW 200(	653287	89536	653287	1		
R 16		W W RESISTOR	730903	89536	730903	1		
R 18		W W RESISTOR 49.6K	743625	89536	743625	1	1	
R 19		W W RESISTOR 156K	743617	89536	743617	1	1	
R 20		RES,CF,20K,+-5%,0.25W	441477	80031	CR251-4-5P20K	1		
R 24		RES,5.0K(+-.05% 0+-5PPM TC 1/4W BOBB	288647	89536	288647	1	1	
R 37, 40		RES,CC,510,+-5%,0.25W	218032	01121	CB5115	2		
S 10- 79		SWITCH,REED,1 FORM A,10VA,36AT	647578	89536	647578	80		
U 1, 9, 17	*	IC,CMOS,QUAD 2 INPUT NAND GATE	453241	02735	CD4011BE	3	1	
U 2	*	IC,CMOS,QUAD 2 INPUT OR GATE	408393	02735	CD4071BE	1	1	
U 3, 6	*	IC,CMOS,BCD-DEC & BINRY-OCTAL DECODER	650689	89536	650689	2	1	
U 4, 7, 10	*	IC,ARRAY,7 TRANS,NPN,COMMOM EMITTER	407866	49671	CA3081	3	1	
U 5, 8	*	IC,CMOS,DUAL 2 IN NAND DRVR W/OPN DRN	604207	02735	CD40107BE	2	1	
U 11, 12, 20,	*	IC,OP AMP,LO-OFFSET VOLTAGE,LO-NOISE	605980	06665	OP-07DP	4	1	
U 23	*		605980					
U 13, 15, 19	*	IC,COMPARATOR,QUAD,CERAMIC,14 PIN DIP	605584	89536	605584	3	1	
U 14	*	IC,CMOS,HEX BUFFER W/3-STATE OUTPUT	407759	12040	MM80C97N	1	1	
U 16, 22	*	IC,OP AMP,GENERAL PURPOSE,TO-78 CASE	418368	89536	418368	2	1	
U 18	*	IC,CMOS,QUAD 2 INPUT NOR GATE	355172	02735	CD4001AE	1	1	
U 21	*	IC,OP AMP,JFET INPUT,8 PIN DIP	605568	89536	605568	1	1	
VR 1, 2	*	ZENER,UNCOMP, 18.0V, 5%, 7.0MA, 0.4W	327973	04713	1N967B	2	1	
VR 3	*	ZENER,UNCOMP, 5.1V, 5%, 20.0MA, 0.4W	159798	04713	1N751A	1	1	
VR 4	*	ZENER,UNCOMP, 4.7V, 5%, 20.0MA, 0.4W	524058	14552	1N751	1		
VR 5	*	ZENER REFERENCE SET	646539	89536	646539	1	5	
VR 22, 23	*		646539					
W 1, 2		CONN,PWB,HEADER,SIP,0.100,4 PIN	417329	89536	417329	2		
W 3, 4		CONN,PWB,HEADER,SIP,0.100,2 PIN	643916	28213	3469/20	2		
W 5, 6		JUMPER, RECEPTACLE	530253	00079	530153-2	2		
Z 1		RES,NET,SIP,8 PIN,7 RES,100K,+-2%	412908	89536	412908	1		
Z 2, 3		RES,NET,SIP,6 PIN,5 RES,100K,+-2%	412726	89536	412726	2		
Z 4	*	REF DIVIDER RNET ASSY TESTED 2280A	731018	89536	731018	1		

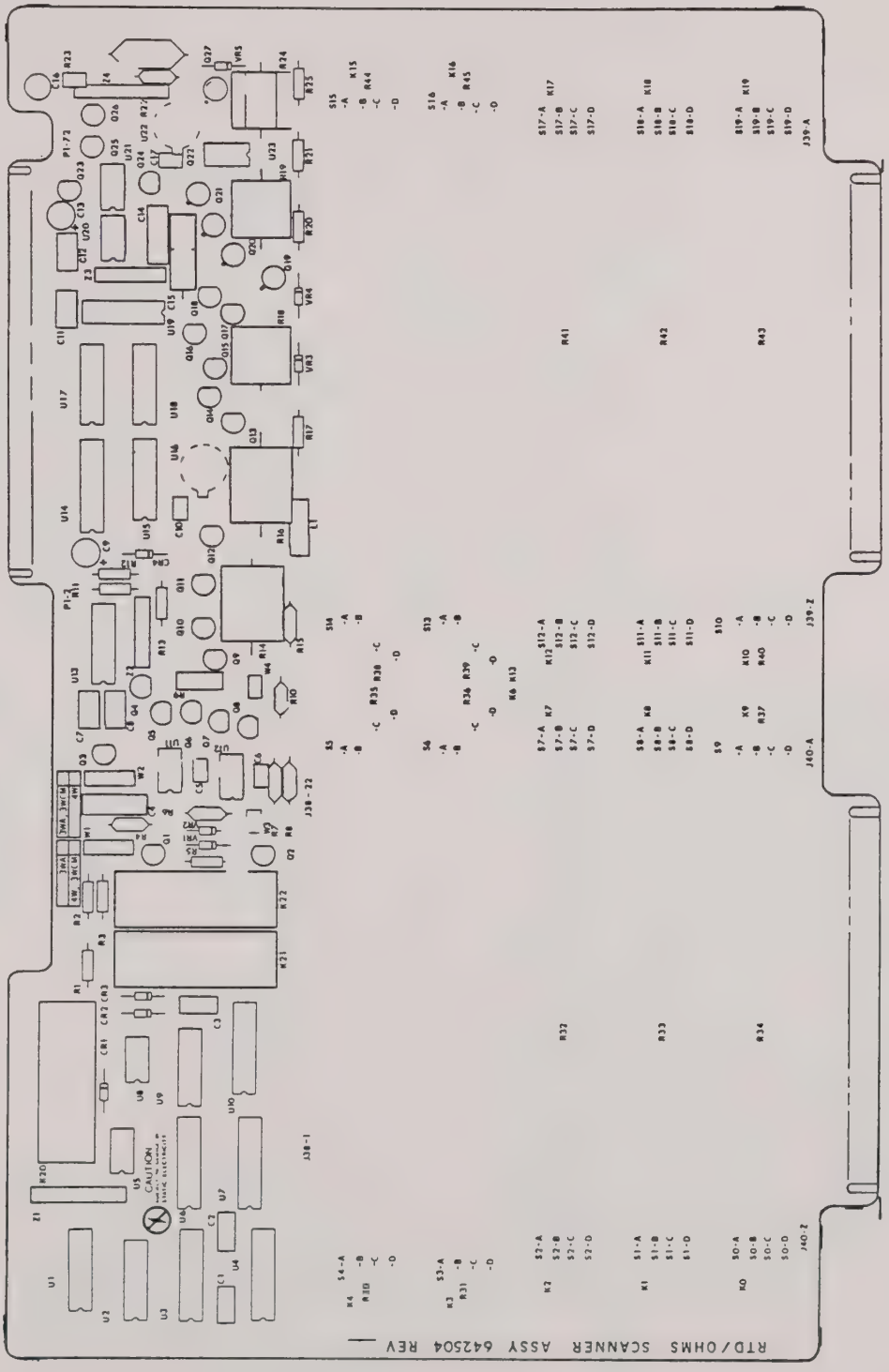
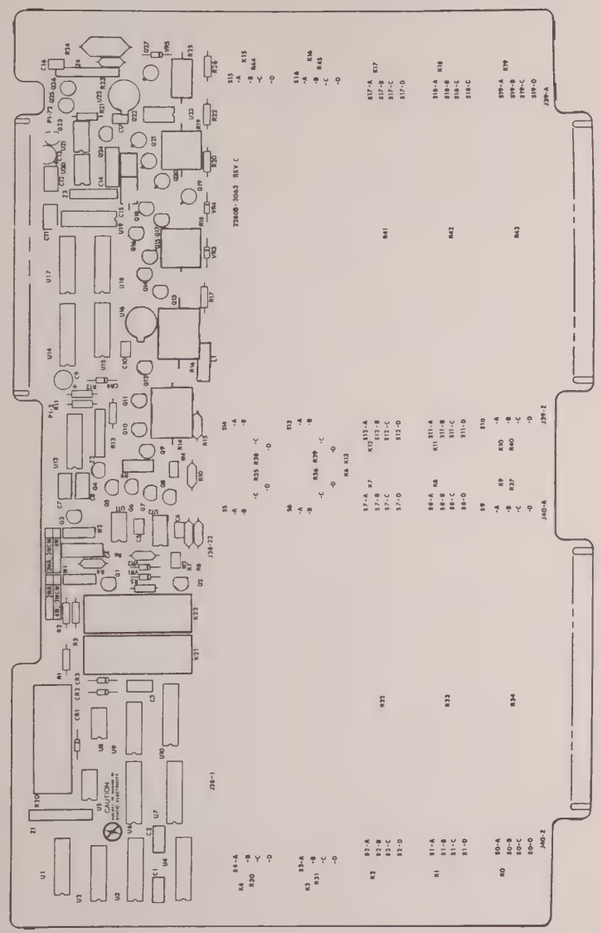


Figure 163-13. 2280B-163 RTD/Resistance Scanner PCA



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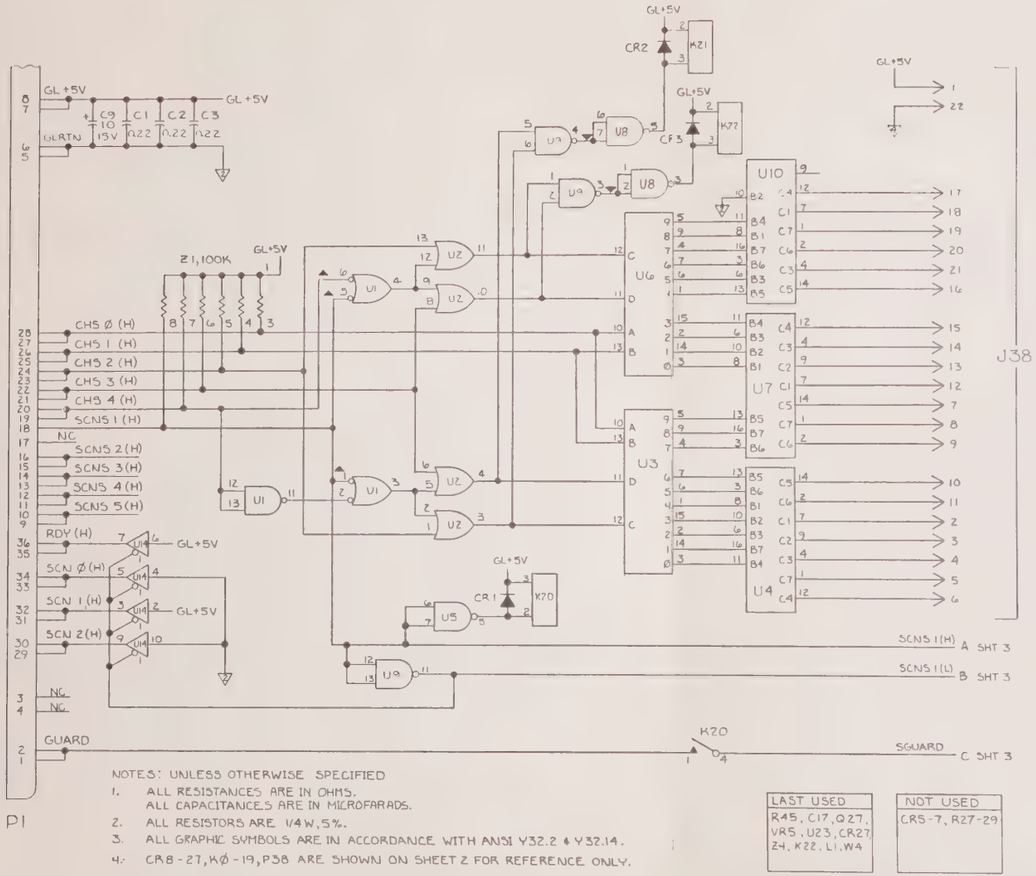


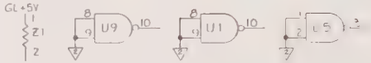
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN MICROFARADS.
2. ALL RESISTORS ARE 1/4W, 5%.
3. ALL GRAPHIC SYMBOLS ARE IN ACCORDANCE WITH ANSI Y32.2 & Y32.14.
4. CR8-27, KØ-19, P38 ARE SHOWN ON SHEET 2 FOR REFERENCE ONLY.

LAST USED
R45, C17, Q27, VR5, U23, CR27, Z4, K22, L1, W4

NOT USED
CR5-7, R27-29

NOT USED



I.C. POWER AND GROUND						
REF DES.	+5V	⏚	+10	-10	VG	DEVICE NAME
U1	14	7				4011B
U2	14	7				4071B
U3	16	8				CD4028B
U4		5,15				CA 3081
U5	8	4				40107
U6	16	8				CD4028B
U7		5,15				CA 3081
U8	8	4				40107
U9	14	7				4011B
U10		5,15				CA 3081
U11			7	4		OP-07
U12			7	4		OP-07
U13			3	12		LM 239
U14	16	8				8097
U15			3	12		LM 239
U16			7	4		LM2Ø8
U17	14	7				4011B
U18	14	7				4001B
U19			3	12		LM [illegible]
U20			7	4		[illegible]
U21			7	4		[illegible]
U22			7	4		[illegible]
U23			7	4		[illegible]
Z1	1					
Z2					1	—
Z3					1	—

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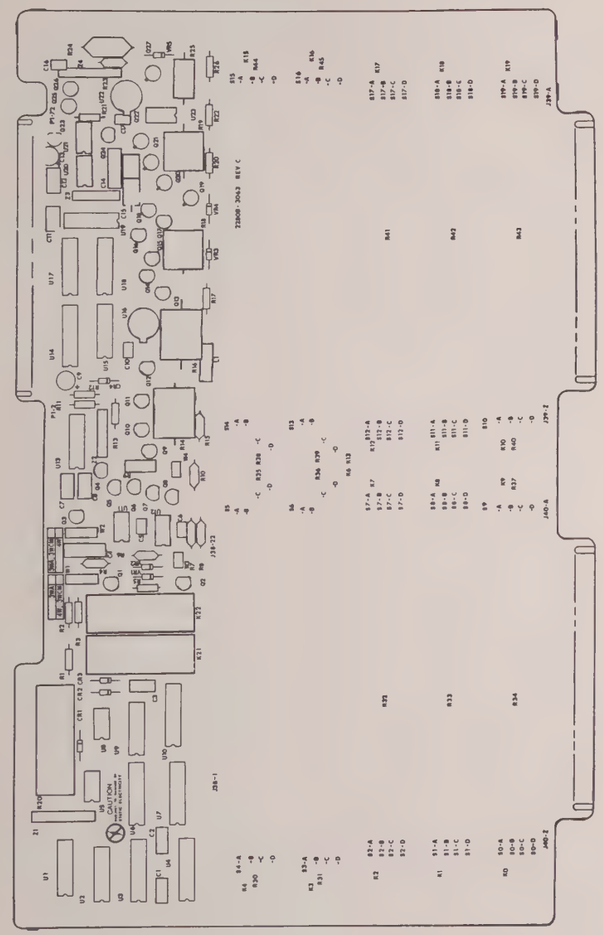
Figure 163-14. RTD-Resistance Scanner Schematic



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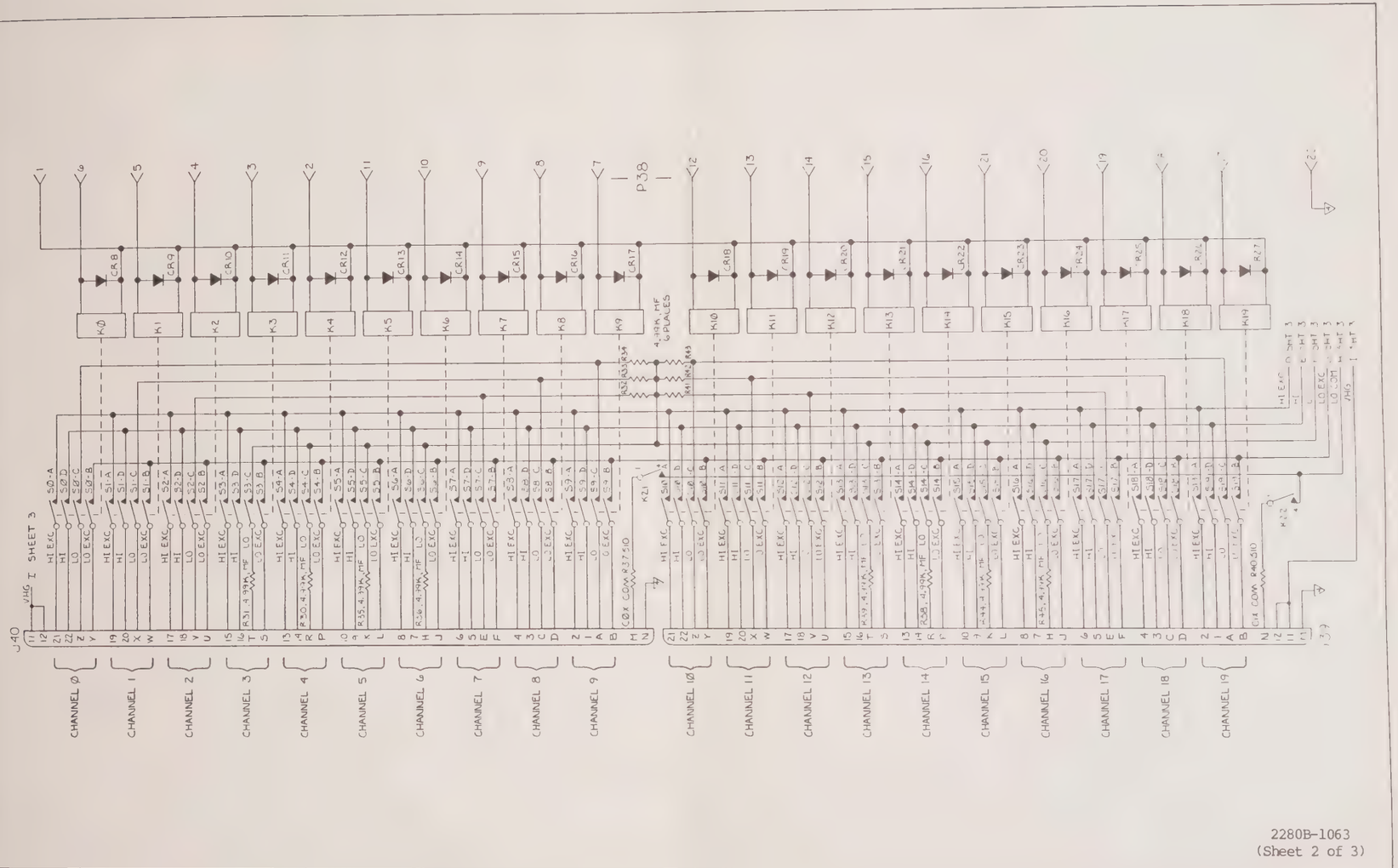

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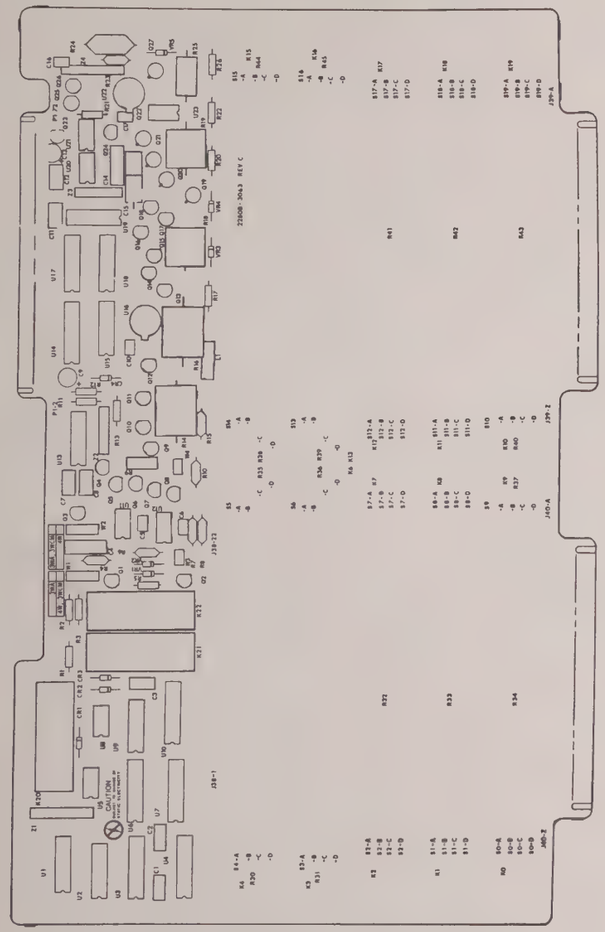
(Sheet 2 of 3)

Figure 163-14. RTD-Resistance Scanner Schematic (cont.)



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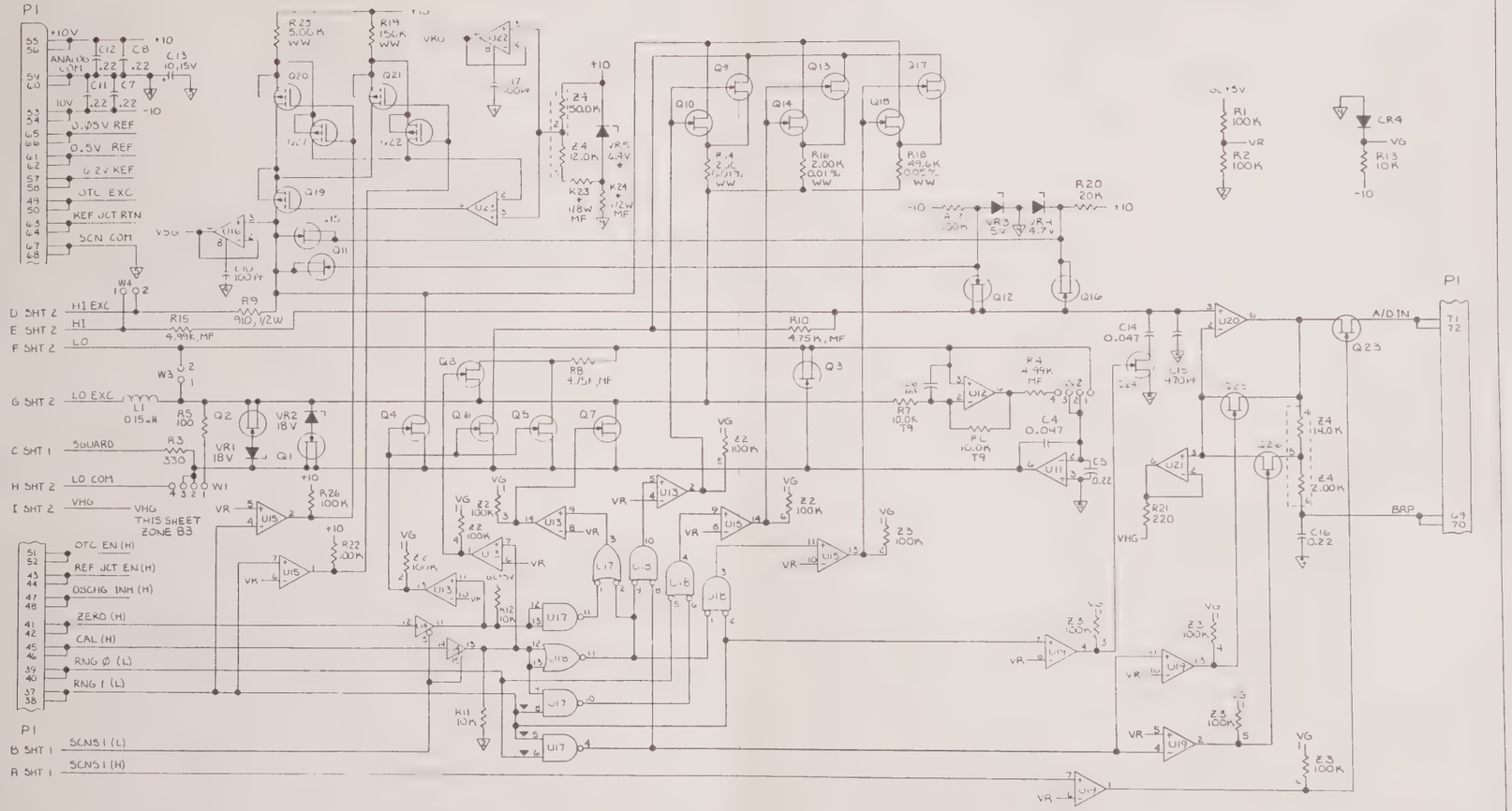

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(Sheet 3 of 3)

Figure 163-14. RTD-Resistance Scanner Schematic (cont.)

Option 2280A-164
Transducer Excitation Module

DESCRIPTION

The Transducer Excitation Module provides excitation conditioning for the measurement of RTD's, low resistances, strain gauges, and strain gauge based transducers. Five precision current sources and one precision voltage source are provided. The 2280 A/D Converter (option 2280A-161), Thermocouple/DC Voltage Scanner (option 2280A-162), and Voltage Input Connector (option 2280A-176) are used to measure the transducers response to the applied excitation.

The excitation currents or voltages are connected to the transducers excitation field wiring on the Transducer Excitation Connector (option 2280A-174). Terminals are also provided on this connector to terminate the transducer sense wiring and in turn connect these signals to the Voltage Input Connector such that the transducers response can be measured.

Excitation is provided for up to 20 measurements. The choice of voltage or current excitation is made in groups of 5 channels using a jumper on the Excitation Input Connector.

WHERE TO FIND FURTHER INFORMATION

In this subsection the Transducer Excitation Module theory of operation, general maintenance, performance tests, calibration procedure, a parts list, and a schematic diagram are given. Installation and system configuration instructions are located in the 2280 Series System Guide, and operating and programming instructions are located in the 2280 Series User Guide. Option specifications can be found in the Appendices to this manual and the System Guide.

The test equipment required to perform this subsection's procedures is listed in Table 164-1. A summary of test equipment required to perform all procedures in this manual is given in Table 1-1 in Section 1 of this manual.

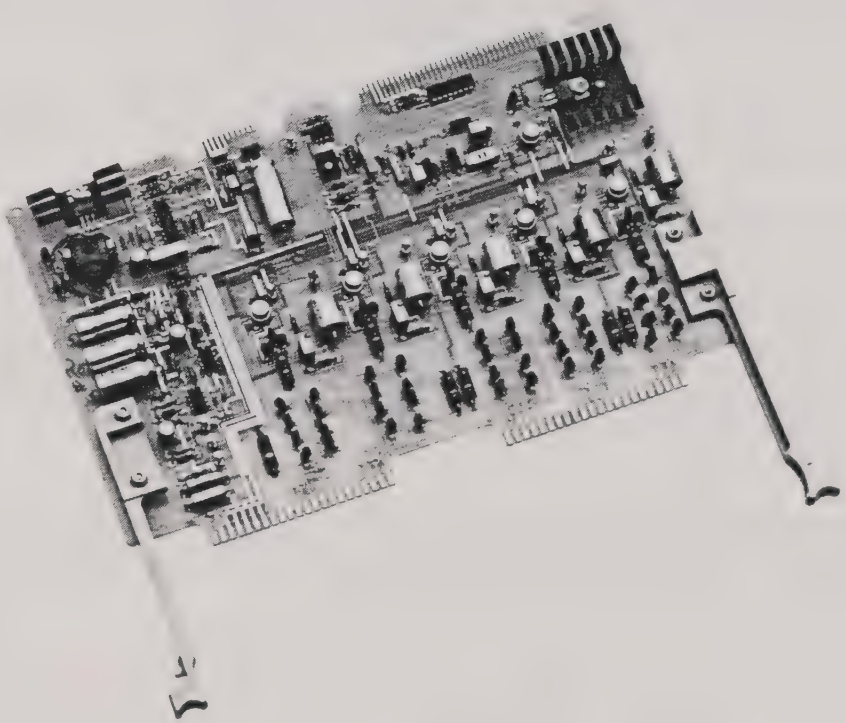


Figure 164-1. Transducer Excitation

Table 164-1. Required Test Equipment

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
Digital Multimeter		Fluke 8505A
Resistance Calibrator		Fluke 5450A
High Performance A/D Converter	.....	Fluke 2280A-161 (no substitute)
Thermocouple/DC Volts Scanner	.....	Fluke 2280A-162 (no substitute)
Voltage Input Connector	.....	Fluke 2280A-176 (no substitute)
Transducer Excitation Connector	.....	Fluke 2280A-174 (no substitute)
Calibration/ Extender Fixture	.....	Fluke Y2056 (no substitute)
Resistor	499 ohms +/- 1%	Fluke Part #_____

THEORY OF OPERATION

The Transducer Excitation Module theory of operation discussion includes an overall functional description of the option and a detailed circuit description that explains the operation of each major circuit block. The schematic diagrams for the Transducer Excitation Module are located at the end of this option subsection.

Overall Functional Description

The Transducer Excitation Module obtains 24V dc power from the serial link and generates stable current and voltage outputs which are made available through the Transducer Excitation Connector (option 2280A-174). The Transducer Excitation Module provides voltage or current excitation for 20 channels. Channels are grouped in 5 groups of 4 channels. One jumper, located on the Transducer Excitation Connector, for each group of channels selects whether the 4 channels are to have voltage or current excitation.

Detailed Circuit Description

POWER SUPPLY

A switching power supply generates the voltages required and provides isolation for the voltage and current output sections of the Transducer

Excitation Module. The power supply is a flyback type composed of T1, U1, one half of U2, U3, and U4. Incoming voltage is applied across the primary winding of T1 for an interval determined by U1, causing the primary current to ramp up to a peak of 1A (when the duty cycle is at a maximum of 50%). Q1 and Q2 are then turned off and the energy stored in T1 is released through CR6, CR7, CR8, and CR10 into C5, C9, C10, and C11. The cycle is repeated at a 32 kHz rate.

The 5.4V nominal voltage on C9 is compared, using U2, with a 2.5V reference voltage from U4. The resulting error signal is relayed to U1 through isolator U3. U1 uses this error information to control the amount of time that Q1 and Q2 are on, thereby maintaining 5.4V across C9 regardless of load or line changes.

The 10V supply is regulated by the linear regulator composed of one half of U2, Q4, and Q3. The 2.5V reference from U4 is compared to the divided-down 10V output by U2, which then uses Q4 to modulate the base current of Q3 and control the output voltage.

VOLTAGE OUTPUT

The voltage output is derived from a precision voltage reference and is driven by a unity-gain buffer amplifier. One of two output values, 2V or 4V, is selected by switch S1 by connecting one of these reference voltages to the input of the buffer amplifier. The buffer amplifier is a high-current, low-output-impedance driver suitable to drive various strain gauge and other transducers.

The buffer amplifier is composed of U5, Q5, and Q6. Transistor Q5 is an n-channel MOSFET used as the series pass element. Transistor Q6 senses the current output and decreases the gate voltage to Q5 if the current exceeds 350 mA, thereby reducing the voltage output to limit the current. The buffer amplifier output voltage is divided in half by a pair of precision wire-wound resistors (R35 and R36). This voltage is made available on the connector for use in bridge completion.

CURRENT SOURCES

Five current sources are provided by the Transducer Excitation Module, with each one set at the factory to output 1 mA. Each current source is designed so that it can provide current for four series-connected RTD's, giving a total of twenty excitation points. If desired, the excitation current can be reduced by placing a resistor in series with the standard current-sense resistors (replacing JR1 typ.).

To provide for fail safe operation, a pair of diode-connected transistors are connected across each RTD or resistance being excited. If a point in the series string of four opens or is left open, then the diodes conduct to ensure that the current will continue to flow through the other points in the string.

Each current source is composed of an amplifier (U6 typ.), a precision voltage reference (VR2), a current-sense resistor (series parallel combination of R45, R50, R55, and R60 typ.), and a p-channel JFET (Q8 typ.). The reference is shared by all five current sources. For each

source, the amplifier maintains a constant voltage across a current sense resistor by controlling the on resistance of a p-channel JFET. Each current source is protected against transient voltage damage by two series resistors (R65 and R70 typ.), which limit current flow, and two JFETs connected as diodes (Q13 and Q18 typ.) which clamp any transient voltages.

COMMUNICATION

The Transducer Excitation Module can be installed in any serial link slot in the Data Logger. In practice, it is usually installed above the scanner used to measure the transducer response to the excitation. When the A/D Converter selects the slot by setting BLCT SCT1 high, the Transducer Excitation Module answers with its type code of 5. Integrated circuit U12 detects the request and responds by turning on its outputs.

GENERAL MAINTENANCE

The Transducer Excitation PCA normally does not require cleaning, but if dirt, dust, or other contamination is visible on the surface, the PCA should be cleaned. Cleaning instructions are located in Section 4 of this manual.

PERFORMANCE TEST

Use the following performance test to verify that the Transducer Excitation Module and Transducer Excitation Connector are operating properly and within specified tolerance.

Two tests are required to verify the proper operation of the assembly; the current excitation test and the voltage excitation test.

Current Excitation Performance Test

1. Turn the 2280 keyswitch to the POWER OFF position. Disconnect the line or battery input power and all other high voltage inputs.

2. Install a High Performance A/D Converter (option 2280A-161) in the uppermost option slot of the 2280. The address switch on the A/D must be set to 0.

3. Install the Transducer Excitation Module to be tested in the slot directly below the A/D. The voltage excitation switch, S1, must be in the 4V position.

4. Install a Thermocouple/DC Volts Scanner (option 2280A-162) in the slot directly below the Transducer Excitation Module. The channels will be measured as channels 20 through 39.

5. Install the 5 jumpers on a Transducer Excitation Connector in the current excitation position.

6. Wire the Transducer Excitation Connector to an Isothermal Input or Voltage Input Connector according to the diagram in Figure 164-2.

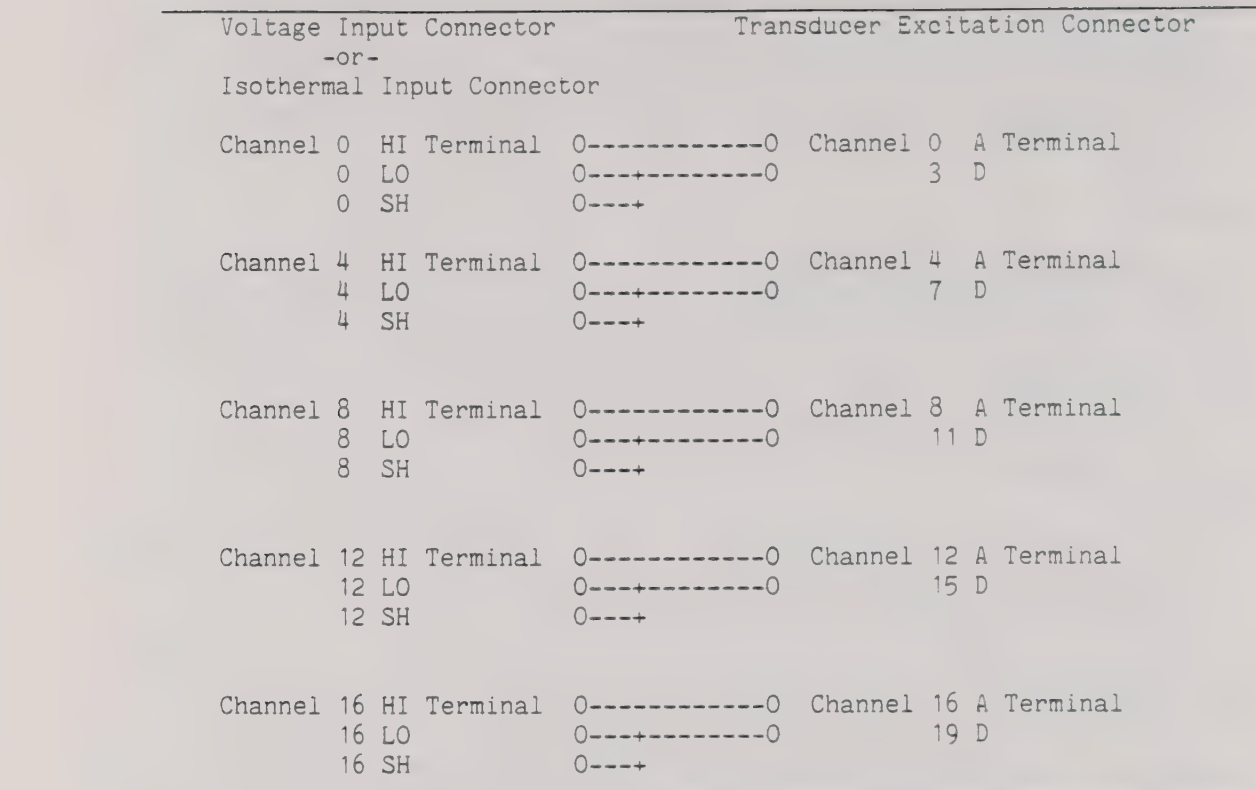


Figure 164-2. Current Excitation Test Wiring Digram 1

7. Install the Transducer Excitation Connector on the Transducer Excitation Module and install the Isothermal or Voltage Input Connector on the Thermocouple/DC Volts Scanner.

8. Program the Data Logger to scan input channels 20 through 39 on the 8V range using the steps in Table 164-2.

9. Press the MONITOR key on the 2280 front panel, then 20 followed by ENTER. Verify that the measurement displayed for channel 20 is between 5.2V and 5.6V. If the measurement is outside this range, then one of the shunt diodes (Q23 through Q30, typ.) is either shorted or open.

10. Press the UPARROW key on the 2280 front panel to read channels 24, 28, 32, and 36 and verify that the measurement on each channel is between 5.2V and 5.6V. If a measurement is outside this range, then one of the shunt diodes is either shorted or open.

11. Power down the 2280 and remove the Transducer Excitation Connector. Rewire the connector as shown below. A 499 ohm +/- 1% resistor must be installed between terminals A and D on channels 0, 4, 8, 12, and 16 of the connector as shown in Figure 164-3.

12. Install the rewired Transducer Excitation Connector on the Transducer Excitation Module. Power up the 2280.

Table 164-2. Current Excitation Performance Test Programming Steps

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
7	20..39	CHANNEL NUMBER (OR BLOCK) = 20..39
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
10	D	A<D> DC VOLTS/CURRENT
11	ENTER	AD: DC RANGE <1-5>? 1
12	2	AD<2> 8.0000 VDC
13	ENTER	AD: CHANNEL MENU CHOICE <1-5>? 1
14	EXIT	A: CHANNEL FUNCTION <A-Z>? D
15	EXIT	CHANNEL NUMBER (OR BLOCK) = C20..39
16	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

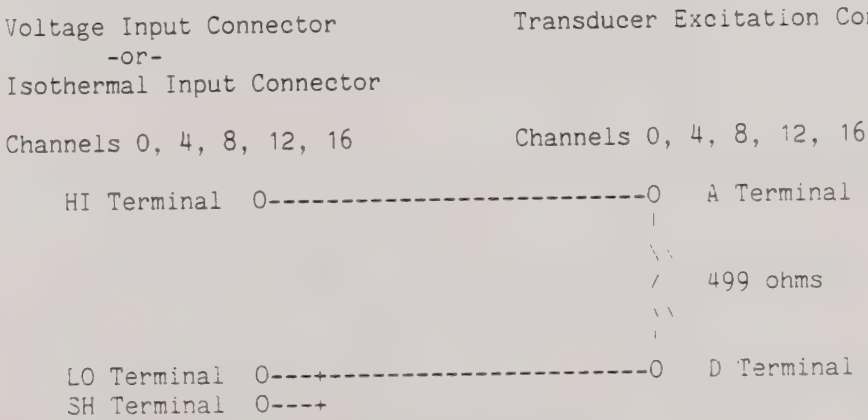


Figure 164-3. Current Excitation Test Wiring Diagram 2

13. Program the 2280 to measure channel 20 through 39 on the 512 mV range using the steps in Table 164-3.

14. Press the MONITOR key on the 2280 front panel, then 20 followed by ENTER. Verify that the measurement displayed for channel 20 is 499 mV, within a tolerance of +/- 5.1mV. This is the voltage drop across the 499 ohm resistor due to the 1mA excitation. If a more accurate measurement of this current is desired, a DMM can be used to measure it directly.

Table 164-3. Current Excitation Performance Test Programming Steps

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
7	20..39	CHANNEL NUMBER (OR BLOCK) = 20..39
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
10	D	A<D> DC VOLTS/CURRENT
11	ENTER	AD: DC RANGE <1-5>? 1
12	3	AD<3> 512.00 MVDC
13	ENTER	AD: CHANNEL MENU CHOICE <1-5>? 1
14	EXIT	A: CHANNEL FUNCTION <A-Z>? D
15	EXIT	CHANNEL NUMBER (OR BLOCK) = C20..39
16	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

15. Press the UPARROW key on the 2280 front panel to read channels 24, 28, 32, and 36 and verify that the measurement on each channel is 499 mV within a tolerance of +/- 5.1mV.

16. This completes the current excitation performance test.

Voltage Excitation Performance Test

1. Perform the current excitation test above.

2. Power down the 2280 and remove the Transducer Excitation Connector. Rewire the connector as shown in Figure 164-4.

3. Move the jumpers on the Transducer Excitation Connector to the voltage excitation position.

4. Install the rewired Transducer Excitation Connector on the Transducer Excitation Module. Power up the 2280.

5. Program the 2280 to measure channels 20 through 39 on the 8V range using the steps in Table 164-2.

6. Press the MONITOR key on the 2280 front panel, then 20 followed by ENTER. Verify that the measurement displayed for channel 20 is 4.0V within a tolerance of +/- 0.004V (4mV).

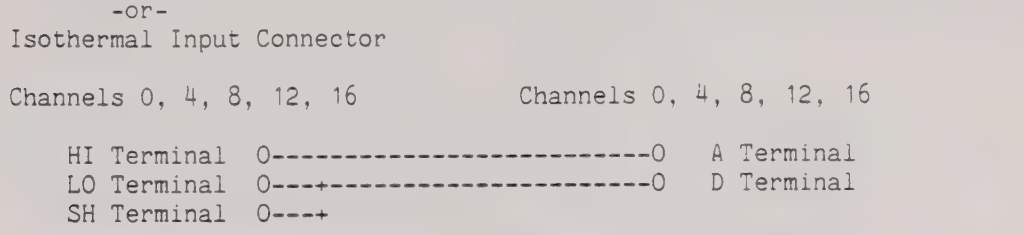


Figure 164-4. Voltage Excitation Test Wiring Diagram

10. Press the UPARROW key on the 2280 front panel to read channels 24, 28, 32, and 36 and verify that the measurement on each channel is 4.0V within a tolerance of +/- 0.004V (4mV).

11. This completes the voltage excitation performance test.

CALIBRATION

The following procedure describes the steps necessary to calibrate the precision voltage and current sources on the Transducer Excitation Module.

Voltage Excitation Calibration

1. Turn the 2280 keyswitch to the POWER OFF position. Disconnect the line or battery input power and all other high voltage inputs.

2. Install a Calibration/Extender Fixture (accessory Y2056) in any option position and install the Transducer Excitation Module on the Fixture. Put slide switch S1 into the 4V position.

3. Reconnect the Data Logger ac line or battery input power.

4. Turn the front panel keyswitch to the PROGRAM position.

5. After the Transducer Excitation Module has warmed up for at least 30 minutes, connect the positive lead of the DMM to test point TP100 and the negative lead to test point TP4.

6. Set the DMM to measure 4V with a resolution of 0.00001V (10uV).

7. Adjust R23 for a DMM reading of 4.00000V within a tolerance of 0.00001V (10uV).

8. Put slide switch S1 in the 2V position. Set the DMM to measure 2V with a resolution of 0.000001V (1uV).

9. Adjust R31 for a DMM reading of 2.000000V within a tolerance of 0.000001V (1uV).

10. Put slide switch S1 in the proper position for your application. This completes the voltage excitation calibration.

Current Excitation Calibration

Note

If a precision resistor of known value is not available, the 8505A may be used with a stable resistor of 250 ohms. Using the DMM in 4-wire mode, measure the resistor on the 100-ohm range. Use the resulting value when preforming the above calibration.

1. Perform the setup steps 1 through 4 from the voltage excitation calibration procedure given above.

2. Again, make sure the Transducer Excitation Module has warmed up for at least 30 minutes, then connect the DMM high lead to test point TP21 and the low lead to test point TP101.

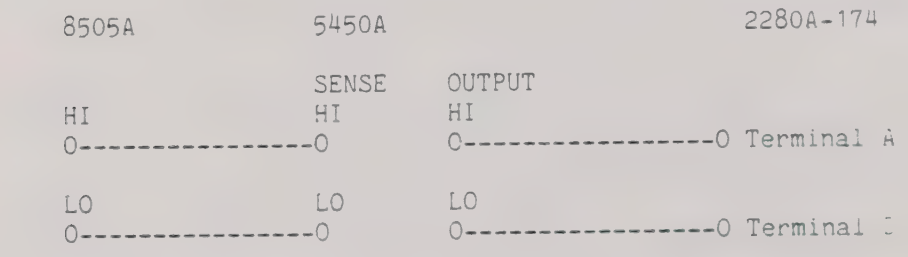
3. Set the DMM to measure on the 10V range with a resolution of 0.0001V (100uV).

4. Adjust R42 for 6.2000V within a tolerance of 0.0002V (200uV).

5. Power down the 2280 and install a Transducer Excitation Connector assembly (option 2280A-174) onto the Transducer Excitation Module.

6. Put the programming jumpers on the Transducer Excitation Connector in the current output position.

7. Connect the DMM, the Resistance Calibrator and the Transducer Excitation as follows, where Terminal A and D on the 2280A-174 are those of channel 0.



4. Set the Resistance Calibrator to the 190 nominal

5. Set the DMM to measure on the 1V range with 1uV resolution, with the average mode enabled. The DMM must have been calibrated within 90 days and also have been "software calibrated" within the last 24 hours.

6. To calibrate the current source for channels 0, 1, 2, and 3, adjust R55, such that the reading on the DMM equals the displayed value of the resistance output on the Resistance Calibrator.

7. Repeat the current calibration procedure for the channel 4, 5, 6, and 7 current source moving the Terminal A and D connections from channel 0 to channel 4 and adjusting R56 such that the reading on the DMM equals the displayed value of the resistance output on the Resistance Calibrator.

8. Repeat the current calibration procedure for the channel 8, 9, 10, and 11 current source moving the Terminal A and D connections from channel 4 to channel 8 and adjusting R57 such that the reading on the DMM equals the displayed value of the resistance output on the Resistance Calibrator.

9. Repeat the current calibration procedure for the channel 12, 13, 14, and 15 current source moving the Terminal A and D connections from channel 8 to channel 12 and adjusting R58 such that the reading on the DMM equals the displayed value of the resistance output on the Resistance Calibrator.

10. Repeat the current calibration procedure for the channel 16, 17, 18, and 19 current source moving the Terminal A and D connections from channel 12 to channel 16 and adjusting R59 such that the reading on the DMM equals the displayed value of the resistance output on the Resistance Calibrator.

11. The calibration of the Transducer Excitation Module is complete. Power down the 2280. Remove the Transducer Excitation Module from the Calibration/Extender Fixture. Remove the Fixture from the 2280. Install the Transducer Excitation Module for use within your 2280 system.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the Transducer Excitation Module is given in Table 164-4. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the Transducer Excitation Module is given in Figure 164-5.

TABLE 164-4. 2280A-164 TRANSDUCER EXCITATION PCA
(SEE FIGURE 164-5.)

REFERENCE DESIGNATOR A->NUMERICS---)	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOTE -E
C 1, 20- 25		CAP,POLYES,0.1UF,+-10%,50V	696484	89536	696484	7		
C 2		CAP,AL,330UF,+100-10%,25V	614404	89536	614404	1		
C 3		CAP,CER,1000PF,+-5%,50V,COG	528539	51406	RPE113	1		
C 4		CAP,POLYES,0.47UF,+-10%,100V	369124	89536	369124	1		
C 5, 12, 13		CAP,AL,47UF,+-20%,16V	643304	89536	643304	3		
C 6		CAP,CER,1000PF,+-10%,500V,X5S	357806	56289	C016B102G102K	1		
C 7		CAP,CER,1.0UF,+-20%,50V,Z5U	436782	72982	8131-050-601-105M	1		
C 8		CAP,CER,0.0012UF,+-10%,500V,Z5R	106732	71590	CF122	1		
C 9		CAP,AL,470UF,+100-10%,12V	602649	89536	602649	1		
C 10, 11		CAP,AL,270UF,+100-10%,20V	602656	89536	602656	2		
C 14- 19		CAP,CER,33PF,+-2%,100V,COG	513226	51406	RPE121	6		
CR 1, 3- 6,	*	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	6		
CR 11	*		203323					
CR 7	*	DIODE,SI, 20 PIV, 1.0 AMP	507731	83003	VSK120	1	2	
CR 8, 10	*	DIODE,SI, 50 PIV, 1.0 AMP	379412	04713	1N4933	2	1	
F 1		FUSE,1/4 X 1-1/4,FAST,0.5A,250V	153858	71400	AGC1-2	1		
H 1		STUD,THREADED,PENN KFH,4-40,.500	494682	89536	494682	2	5	
H 2		BROACHING TYPE, L=.750 DASH#12,4-40	614636	89536	614636	2		
H 3		WASHER,LOCK,SPLIT,STEEL,#4	110395	89536	110395	4		
H 4		NUT,MACH,HEX,STL,4-40	110635	89536	110635	4		
H 5		WASHER,FLAT,BRASS,#4,0.025	110775	89536	110775	4		
H 6		SCREW,MACH,PHP,STL,6-32X3/8	152165	89536	152165	2		
H 7		WASHER,FLAT,BRASS,#6,0.012 THK	111054	89536	111054	2		
H 8		WASHER,LOCK,SPLIT,STEEL,#6	110692	89536	110692	2		
H 9		NUT,HEX,MINI,S.STL,6-32	110569	89536	110569	2		
L 1, 2		CHOKE,6TURN	320911	89536	320911	2		
MP 1		RETAINER,P.C.B.	579078	89536	579078	2		
MP 2		HEAT SINK, XISTOR THERMALLOY 6072B	473686	89536	473686	1		
MP 3		FUSE HLDR,CLIP,PCB,1/4 DIA FUSE	485219	91833	3529	2		
MP 4		SPACER,RND,ALUM,0.156IDX0.250	153155	89536	153155	2		
MP 5		BAG,SHIELDING,TRANSPARENT,12"X16"	680983	89536	680983	1		
MP 6		HEATSINK, INNER, U1	473660	13103	6070B	1	1	
Q 1	*	TRANSISTOR,SI,NPN,HI-VOLTAGE	370684	04713	MPS A 42	1	1	
Q 2	*	SILICON, NPN, FAST SWITCHING D44H11	535542	89536	535542	1	1	
Q 3, 7	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	340026	04713	MPS6563	2	1	
Q 4, 23- 62	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	41	1	
Q 5	*	TRANSISTOR,SI,N-MOS,POWER,TO-220AB	586107	89536	586107	1	9	
Q 6	*	TRANSISTOR,SI,NPN,SELECTD,TEMP SENSOR	640862	89536	640862	1	1	
Q 8- 17	*	TRANSISTOR,SI,P-JFET,TO-92	413690	89536	413690	10	1	
Q 18- 22	*	TRANSISTOR,SI,N-JFET,REMOTE CUTOFF	429977	89536	429977	5	2	
R 1- 4		RES,MF,10K,+-1%,0.125W,100PPM	168260	91637	CMF551002F	4		
R 5		RES,MF,15.8K,+-1%,0.125W,100PPM	293688	91637	CMF551582F	1		
R 6		RES,MF,39.2K,+-1%,0.125W,100PPM	236414	91637	CMF553922F	1		
R 7		RES,CF,1K,+-5%,0.25W	343426	80031	CR251-4-5P1K	1		
R 8		RES,CF,1.8K,+-5%,0.25W	441444	80031	CR251-4-5P1K8	1		
R 9, 18		RES,CF,510,+-5%,0.25W	441600	80031	CR251-4-5P510E	2		
R 10		RES,CF,1.5K,+-5%,0.25W	343418	80031	CR251-4-5P1K5	1		
R 11, 16, 75		RES,CF,330,+-5%,0.25W	368720	80031	CR251-4-5P330E	3		
R 12		RES,CF,430,+-5%,0.25W	441568	80031	CR251-4-5P430E	1		
R 13		RES,MF,121,+-1%,0.125W,100PPM	343160	91637	CMF551210F	1		
R 14, 32, 37,		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	6		
R 43, 44, 77			348839					
R 15		RES,MF,100,+-1%,0.125W,100PPM	168195	91637	CMF551000F	1		
R 17		RES,MF,10.7K,+-1%,0.125W,25PPM	423681	91637	CMF551072F	1		
R 19		RES,MF,3.57K,+-1%,0.125W,25PPM	376905	89536	376905	1		
R 20		RES,CF,51,+-5%,0.25W	414540	80031	CR251-4-5P51E	1		
R 23, 31, 55-		RES,VAR,CERM,1K,+-10%,0.5W	393728	32997	3299W-CR2-102	7		
R 59			393728					
R 24		RES,MF,3.92K,+-1%,0.125W,100PPM	294801	91637	CMF553921F	1		
R 25		RES,MF,7.5K,+-1%,0.125W,25PPM	484881	89536	484881	1		
R 26		RES,WW,23.7K,+-0.1%,0.15W	385609	89536	385609	1		
R 27, 29		RES,WW,20K,+-0.1%,0.125W	271395	89536	271395	2	1	
R 28		RES,MF,53.6,+-1%,0.125W,100PPM	339861	91637	CMF5553R6F	1	1	
R 30		RES,MF,287K,+-1%,0.125W,25PPM	257543	89536	257543	1		
R 33		RES,CF,13K,+-5%,0.25W	441402	80031	CR251-4-5P13K	1		
R 34		RES,CF,1.5,+-5%,0.25W	442020	89536	442020	1		
R 35, 36		W W RESISTOR	719377	89536	719377	2		
R 40		RES,WW,60.75K,+-0.1%,0.15W	385625	89536	385625	1	1	
R 41		RES,MF,750,+-1%,0.125W,25PPM	448035	89536	448035	1	1	
R 42		RES,VAR,CERM,500,+-10%,0.5W	325613	89536	325613	1		
R 45- 49		W W RESISTOR	719344	89536	719344	5		
R 50- 54		RES,CF,5.6M,+-5%,0.25W	543371	80031	CR251-4-5P5M6	5	1	
R 60- 64		RES,MF,10.5,+-1%,0.125W,100PPM	494492	89536	494492	5		
R 65- 74		RES,WW,FUSIBLE,1K,+-10%,2W	474080	89536	474080	10		

TABLE 164-4. 2280A-164 TRANSDUCER EXCITATION PCA
(SEE FIGURE 164-5.)

REFERENCE DESIGNATOR A-)NUMERICS---)	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
R 76		RES,CF,100K,+-5%,0.25W	348920	80031	CR251-4-5P100K	1		
S 1		SWITCH,SLIDE,SPDT	453365	34828	G1-116-0001-G20-52	1		
T 1		INVERTER TRANSFORMER	580407	89536	580407	1		
U 1	*	IC,REGULATING PULSE WIDTH MODULATOR	454678	01295	SG3524N	1	1	
U 2	*	IC,OP AMP,DUAL,INDUSTRIAL TEMP RANGE	605550	01295	LM258JG	1	1	
U 3	*	ISOLATOR,OPTO,HI-SPEED,8 PIN DIP	354746	89536	354746	1	1	
U 4	*	IC, 2.5 V,40 PPM T.C.,BANDGAP REF	472845	04713	MC1403V	1	1	
U 5- 10	*	IC,OP AMP,GENERAL PURPOSE,TO-78 CASE	418368	89536	418368	6	1	
U 11	*	IC,OP AMP,MOSFET INPUT,8 PIN DIP	507426	89536	507426	1	2	
U 12	*	IC,CMOS,HEX BUFFER W/3-STATE OUTPUT	407759	12040	MM80C97N	1	1	
VR 1, 2	*	ZENER REFERENCE SET	646539	89536	646539	2		1
VR 3	*	ZENER,UNCOMP, 10.0V, 5%, 25.0MA, 1.0W	340695	12969	UZ8710	1	1	
VR 4	*	ZENER,UNCOMP, 6.2V, 5%, 20.0MA. 0.4W	325811	07910	1N753A	1	1	
XQ 13- 17		TERMINAL, FEED-THRU/TEFLON	529297	98291	011-6812-00-0-206	5		

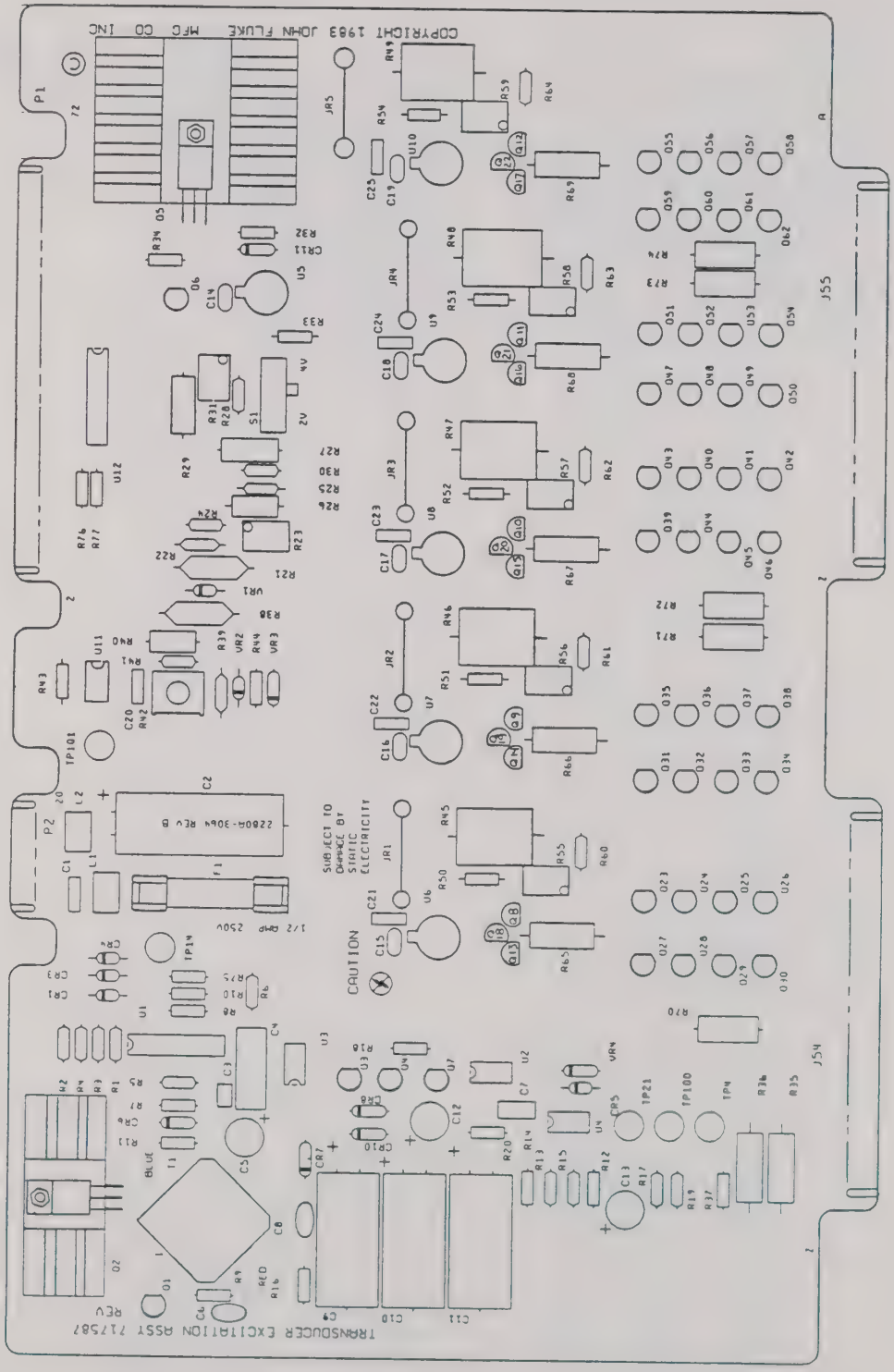
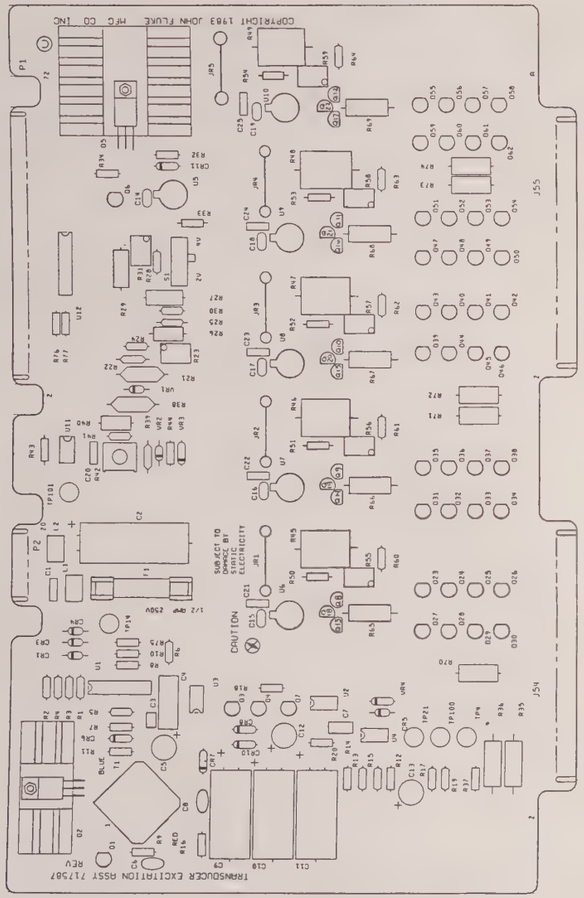
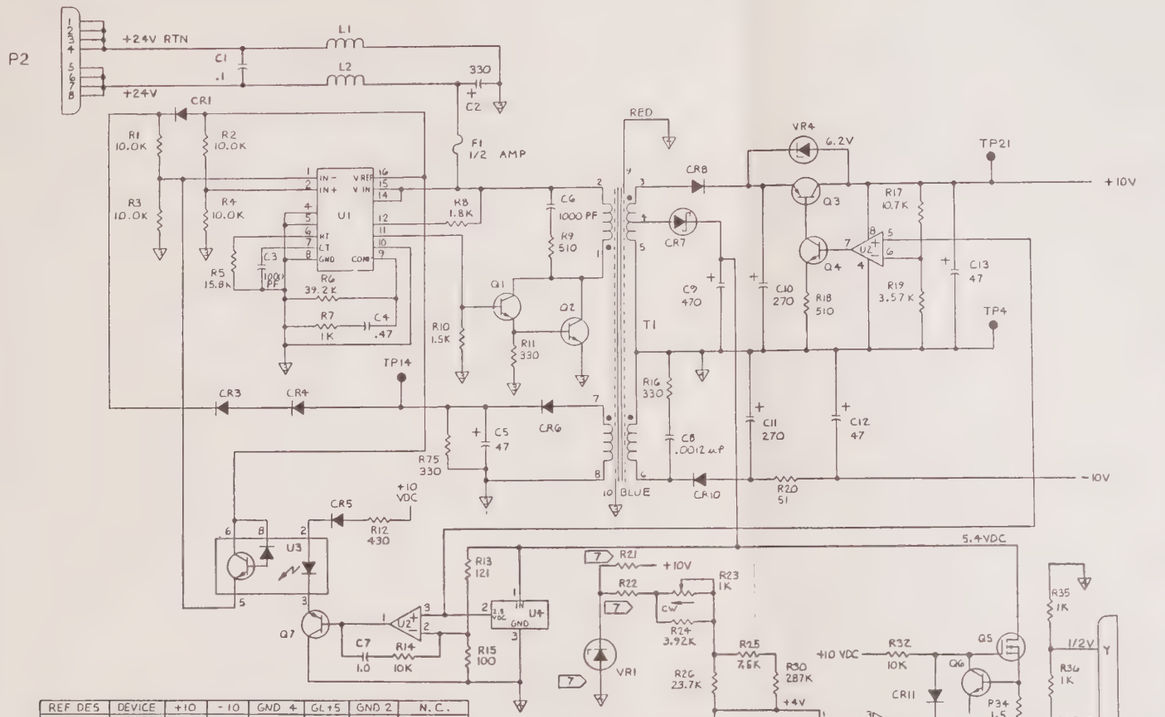


Figure 164-5. 2280A-164 Transducer Excitation PCA



2280A-1664



REF DES	DEVICE	+10	-10	GND 4	GL+5	GND 2	N.C.
U1	SG3524	—	—	—	—	—	3, 13
U2	LM258	—	—	—	—	—	—
U3	GN135	—	—	—	—	—	1, 4, 7
U4	MC1403	—	—	—	—	—	4, 5, 6, 7, 8
U5	LM208	7	4	—	—	—	5
U6	LM208	7	4	—	—	—	5
U7	LM208	7	4	—	—	—	5
U8	LM208	7	4	—	—	—	5
U9	LM208	7	4	—	—	—	5
U10	LM208	7	4	—	—	—	5
U11	3140E	7	—	4	—	—	1, 5, 8
U12	80C97	—	—	—	16	8	—

NOTES: UNLESS OTHERWISE SPECIFIED

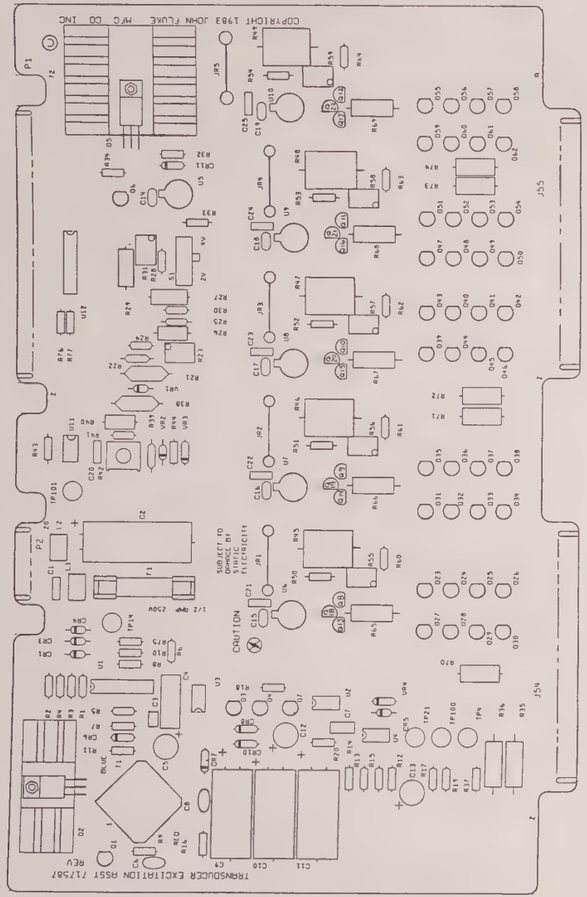
1. ALL RESISTANCE IS IN OHMS.
2. ALL CAPACITANCE IS IN MICROFARADS.
3. ALL GRAPHIC SYMBOLS ARE IN ACCORDANCE WITH ANSI Y32.2 AND Y32.14.

6. R38, R39, AND VR2 IS A MATCHED REFERENCE SET.

7. R21, R22, AND VR1 IS A MATCHED REFERENCE SET.

2280A-1064

Figure 164-5. Transducer Excitation Module Schematic Diagram



2280A-1664

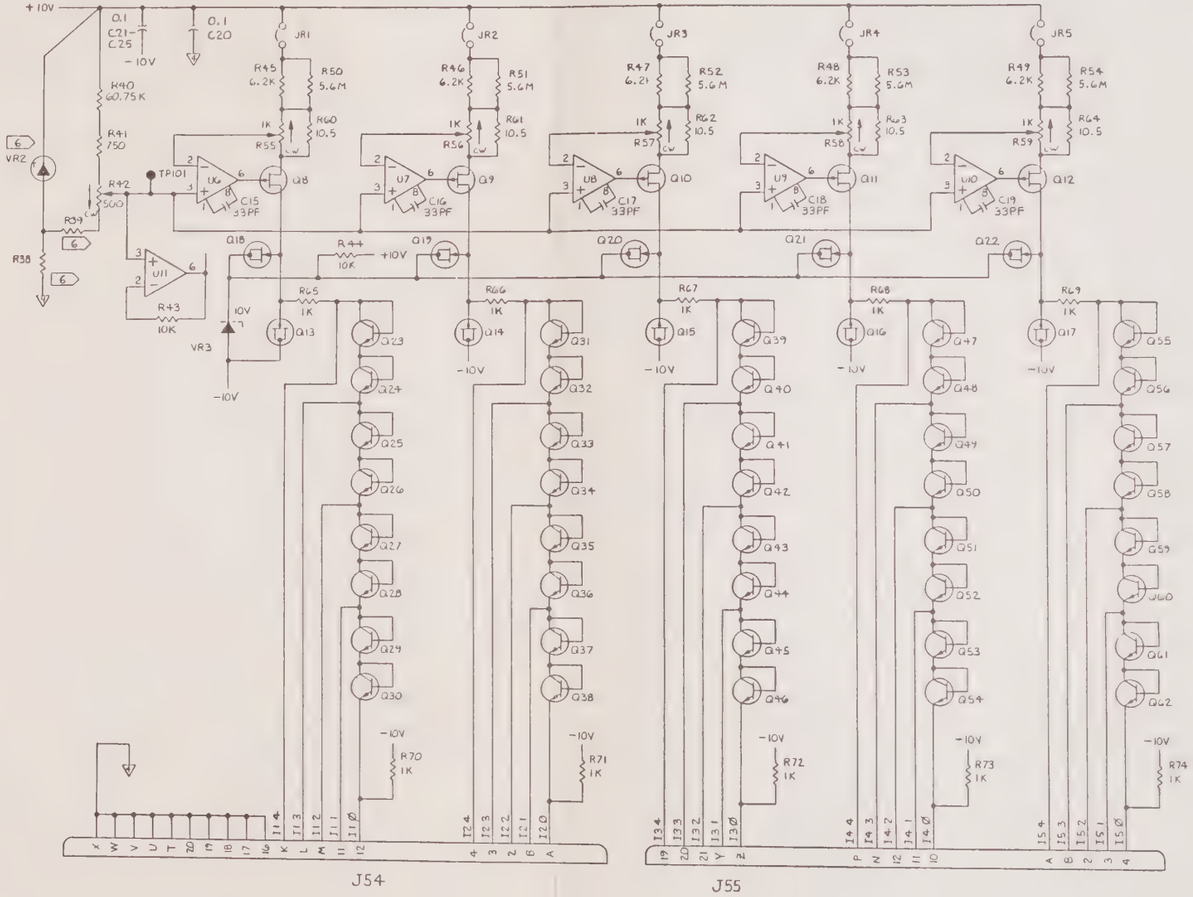
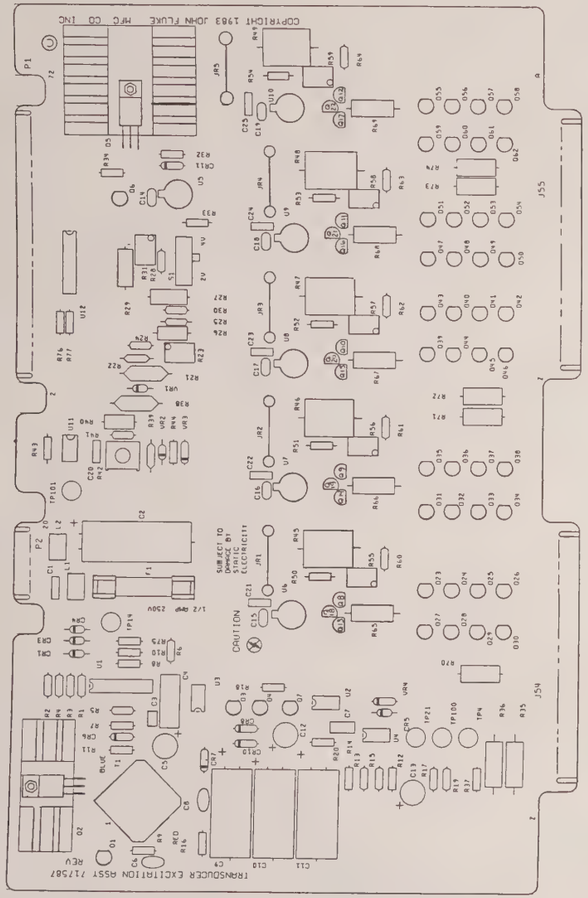
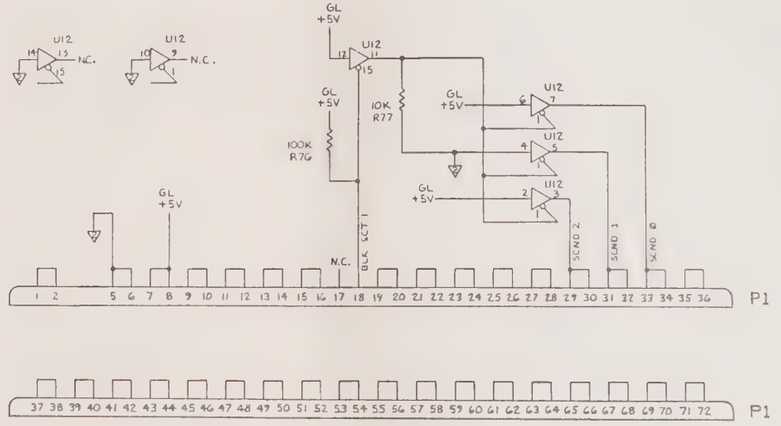


Figure 164-5. Transducer Excitation Module Schematic Diagram (cont.)



2280A-1664



2280A-1064

Figure 164-5. Transducer Excitation Module Schematic Diagram (cont.)

Option 2280A-168
Digital I/O Assembly

DESCRIPTION

The Digital I/O Assembly, illustrated in Figure 168-1, allows the Data Logger to receive and transmit digital information. The input connector used with the Digital I/O and the way the connector is wired determines whether the assembly is used by the 2280 to transmit or receive information. When used for output, a single channel (or single bit) can be changed at a time. When used for input, the 2280 can read a single bit at a time or parallel words in a binary or binary-coded-decimal (BCD) format.

Two connector options are available for use with the Digital I/O Assembly. For output, the Status Output Connector (option 2280A-169) is used. Inputing requires use of the Digital/Status Input Connector (option 2280A-179). Signals originating on the chosen connector inform the Digital I/O assembly whether is being used for input or output.

The Digital I/O Assembly supports 20 input or output channels. If the Digital I/O Assembly is used to input data to the Data Logger, two additional input lines are used to determine which information type (BCD, binary, or status) the assembly is to measure. Refer to the appropriate connector option section in the 2280 Series System Guide for configuration instructions.

WHERE TO FIND FURTHER INFORMATION

In this subsection are Digital I/O Assembly theory of operation, general maintenance, performance tests, calibration procedure, a parts list, and a schematic diagram. Installation and system configuration instructions are in the 2280 Series System Guide, and operating and programming instructions are in the 2280 Series User Guide. Option specifications are in the Appendices in this manual and the System Guide.

Test equipment required to perform the procedures in this subsection is listed in Table 168-1. A summary of test equipment required for all procedures in this manual is given in Table 1-1 in Section 1 of this manual.

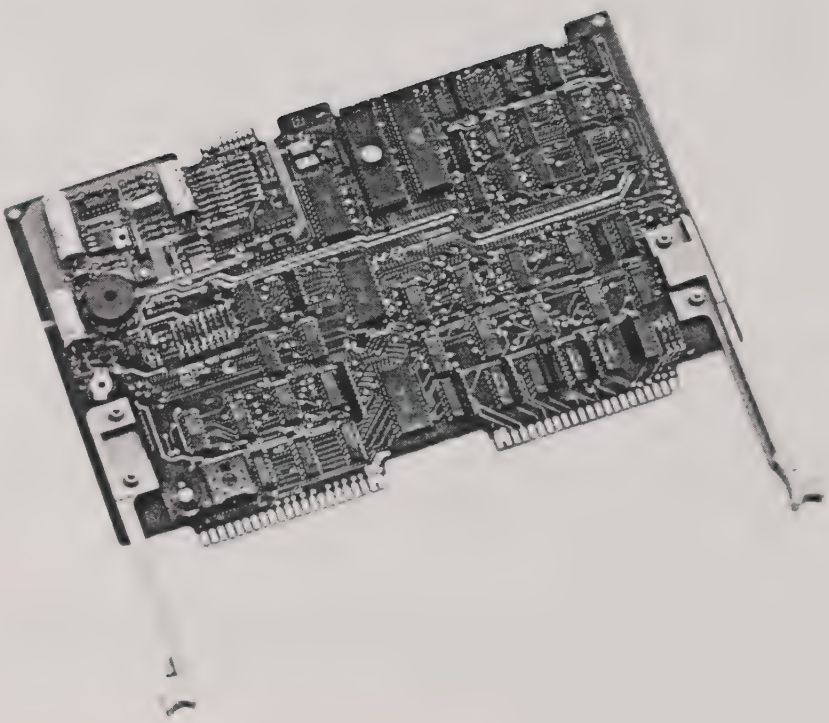


Figure 168-1. Digital I/O Assembly

Table 168-1. Required Test Equipment

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
Digital Multimeter	+/- 10V, +/- 0.06V	Fluke 8505A
Calibration/ Extender Fixture	.....	Fluke Accessory Y2056 (no substitute)
Digital/Status Input Connector	.....	Fluke Option 2280A-179 (no substitute)
Status Output Connector	.....	Fluke Option 2280A-169 (no substitute)

THEORY OF OPERATION

The following theory of operation discussion includes a functional description of the Digital I/O Assembly, followed by a block diagram analysis which describes how each major circuit block on the Digital I/O Assembly works. Circuit analysis of each block described in the block diagram analysis concludes the theory of operation discussion. Where necessary, block diagrams and simplified schematics are included with the text. Schematic diagrams for the Digital I/O Assembly are at the end of this option subsection.

Overall Functional Description

The Digital I/O Assembly provides the data logger with the ability to output single bit alarm or status information and the ability to input information in any of three formats: single-bit alarm or status , BCD formated digital, and binary formated digital information.

Block Diagram Analysis

Six major circuit blocks perform the necessary functions: the power supply, address select, the serial link interface, the microcomputer, the handshake logic, and the parallel input and output interfaces. Figure 168-2 illustrates the Digital I/O Assembly in block diagram form. The following paragraphs discuss the function of each of the blocks in the diagram.

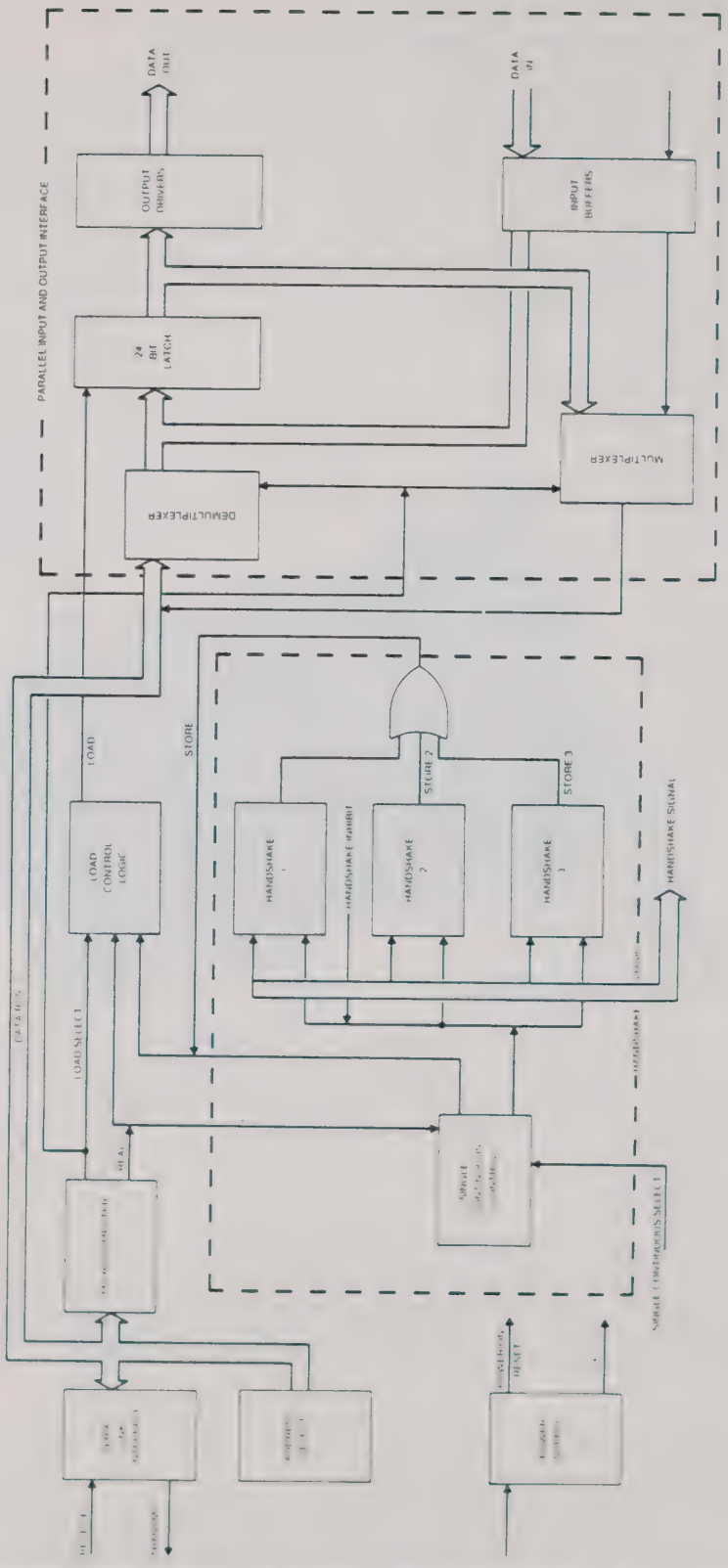


Figure 168-2. Digital I/O Assembly Block Diagram

POWER SUPPLY

The power supply converts incoming dc power from the serial link into isolated +5V dc for the Digital I/O circuitry and +5V dc for the serial link. The power supply circuitry also generates a reset signal that is used to start up the the microcomputer and the handshake logic properly.

SERIAL LINK

The Serial Link allows the Digital I/O Assembly to exchange commands and measurement data with the Data Logger mainframe controller. In this block, the bi-directional serial transmissions are electrically isolated, buffered, and converted to signals that the microcomputer can use. The serial link circuitry sends an interrupt signal and data to the microcomputer while the microcomputer returns data and a transmitter enable signal.

ADDRESS SELECT

Two thumbwheel switches on the Digital I/O Assembly are used to select the channel range for the assembly. The switches select the starting channel number of a block of 20 contiguous channels for the assembly. The switch that selects the most significant digit has a valid range of 0 to 14 (position 15 not used), and the switch that selects the second-most significant digit has a range of 0 to 9.

MICROCOMPUTER

The Digital I/O Option uses an NMOS 8748, 8 bit microcomputer to control all interaction between the 2280 mainframe controller and the input/output interface.

HANDSHAKE LOGIC

When the Digital I/O board is used to read parallel words in either a BCD or binary format, the user may select one of three different handshake schemes through which the data may be entered. In addition, the user may select either noninverted or inverted polarity for each of the handshakes and may choose between a single or continuous update mode.

In the continuous update mode, data may be continuously loaded between transfers to the mainframe controller, thereby ensuring that only the most recent data is measured. In the single update mode, the data may be loaded only once between transfers; any further loads are inhibited until the data has been retrieved by the mainframe controller.

PARALLEL INPUT AND OUTPUT INTERFACE

This circuit block consists of data storage latches, tri-state buffers to read from and write to the latches, and input and output buffers. The latches are used to store the data output when the Digital I/O is used for status output, and they are used to store the parallel BCD or binary input data when used as a digital input.

Detailed Circuit Description

POWER SUPPLY

Dc-Dc Converter

Isolation of the Digital I/O circuitry is provided by T1 which is also the core of the dc-dc converter. In the dc-dc converter, T1, U1, Q1, and Q2 comprise a "flyback" type of switching regulator converter. Incoming dc power from 10V dc to 25V dc is applied to the primary of T1 for an interval generated by U1, causing the primary current to ramp up to approximately 1 ampere peak before Q1 and Q2 are turned off. The energy stored in T1 is then released through CR10 and CR12, into C5 and C20 respectively. The voltage on C5 is sampled by R9, R10, and R11, and a feedback error signal is generated and relayed to U1. The duty cycle of Q1 and Q2 is then adjusted by U1 to maintain C5 at 5.0V despite load changes.

The voltage on C20 is used to supply all isolated circuitry on the assembly. The voltage on C5 is used to power the serial link interface circuits.

Adjustment potentiometer R11 is used to set the isolated 5V dc supply voltage (GL +5) to 5V. This can be measured between test points TP2 and TP20.

Reset Generator

When power is first applied to the Digital I/O, Q6 is turned on by R36, and the power-on reset signal (POR(L)) to the controller is held low. U24 compares the voltage on C22 to a 1.22V reference provided through VR3 to determine whether the +5V supply is within tolerance. Once the supply voltage has stabilized, C21 is allowed to charge through R28 and R33, generating a delay of approximately 50 ms before C21 charges to 1.22V. This causes U24 to remove the drive to Q6, allowing POR(L) to be pulled high by R37.

SERIAL LINK

There are three major components in the serial link interface: a Universal Asynchronous Receiver and Transmitter (UART) (U8), a bidirectional optical interface (U4 and U5), and a differential driver (U2) and receiver (U3).

To improve system operation in an electrically noisy environment, differential line drivers in U2 and receivers in U3 transmit and receive information through transient suppression networks consisting of resistors R12, R13, R14, R15, R18, R19, R20 and R21 and diodes CR1 through CR8 in conjunction with VR2.

When data is transmitted from the Digital I/O Assembly to the system controller, the processor places the eight-bit word on the Digital I/O Assembly internal data bus accompanied by a WRITE STROBE. The UART accepts each of the parallel eight-bit words from the processor and converts them to a serial data stream. The serialized data is then sent

through the optical coupler (U4, pins 3, 4, 5, and 6) and driver (U2) onto the serial link. Because there may be a number of different devices on the link, the drivers are placed in a high-impedance state when they are not actively involved in transferring data. Driver tri-stating is accomplished by the signal from microcomputer port 1, bit 5, which is transferred through an optical coupler (U4, pins 1, 2, 5, and 7).

Incoming data from the 2280 mainframe controller assembly is fed into the UART (U8) through optical coupler U5. Upon receipt of a data byte, the UART interrupts the microcomputer (U7).

The clock for the UART is provided by the Address Latch Enable (ALE(H)) signal from the microprocessor. Clock frequency is 16 times the 25 kbaud bit rate of the serial link.

ADDRESS SELECT

Two thumbwheel switches, S1 and S2, on the Digital I/O Assembly are used to select the address range for that assembly. The microcomputer reads the current switch settings through buffers in U27 and U28 when they are enabled by setting port 1 bit 6 low.

Each time a command is received from the mainframe controller, the state of the address switches is checked. If the address within the command falls within the address block selected through the switches, the remainder of the message is decoded and executed. If the address does not match, the command from the mainframe controller is ignored.

MICROCOMPUTER

The microcomputer on the Digital I/O Assembly (U7) has 1024 bytes of internal EPROM memory and 64 bytes of internal RAM. There is no external memory on the Digital I/O Assembly. A 6MHz crystal (Y1) provides the frequency reference for the clock generated within the microcomputer. The microcomputer, in turn, generates the 400K Address Latch Enable (ALE(H)) signal used as the clock for the remainder of the subsystem.

The microcomputer has two 4-bit input/output ports which are used to develop a number of control signals throughout the Digital I/O board. In addition, there is an 8-bit data bus used for data transfer within the Digital I/O Assembly.

HANDSHAKE LOGIC

Five subcircuits comprise the handshake logic: the three handshake circuits, the single/continuous control circuit, and the load control circuit. Handshake logic provides three alternate means by which data may be entered. In response to an external load signal, the selected handshake circuit generates the appropriate acknowledge and a store signal to the load control circuit.

The three independent handshake circuits are discussed in the following paragraphs. All signals in the accompanying illustrations are shown in the noninverted polarity.

Handshake Type One Circuit

Counter U34, flip-flops U20 (labeled F and G), and gates U12, U13, U15, U16, and U18 comprise the type one handshake circuit. Refer to Figure 168-3. Immediately following power on, the circuit is in its initial state with both flip-flops reset. One clock pulse after the counter output (P) transitions to a logical one, flip-flop G sets, generating the leading edge of the ACK1 output pulse. Approximately 32 uS later, P returns to the logical zero state, then flop-flop F is set and the trailing edge of ACK1 is generated.

After the ACK1 output pulse is generated, the circuit is ready to accept the LOAD 1 input pulse from the user's circuitry. When LOAD 1 transitions to a logic zero, the G flip-flop resets and the leading edge of the STORE command is sent to the Load Control circuit. The incoming data is stored. When the LOAD 1 command returns to the logic 1 state, flip-flop F resets and the sequence is complete.

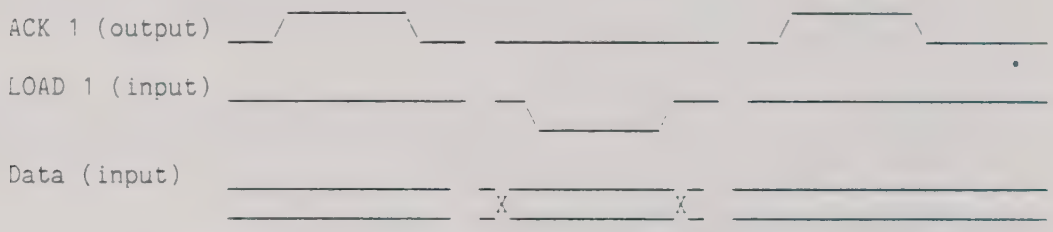


Figure 168-3. Handshake Type One Timing Diagram

Handshake Type Two Circuit

Flip-flops U21 (labeled D and E) and gates U12, U13, and U16 implement the circuit for the type two handshake. Refer to Figure 168-4. Immediately following power up, flip-flops D and E are in the reset state, from which flip-flop E transitions to the logic 1 state to generate the leading edge of the ACK 2 output signal. The external device may now generate the leading edge of the LOAD 2 input signal. In response to the LOAD 2 zero-to-one transition, the external data is stored and flip-flop E is reset, thus, generating the trailing edge of the ACK 2 signal. When LOAD 2 returns to the logic zero state, ending the handshake, flip-flop D is reset.

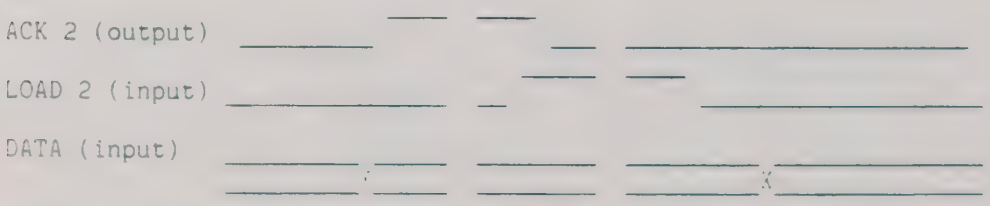


Figure 168-4. Handshake Type Two Timing Diagram

Handshake Type Three Circuit

The final handshake circuit consists of gates U12 and U15. Data may be loaded into the data storage register using this method any time that the BUSY output is in the logic zero state. The LOAD 3 input command is accepted by the Digital I/O Assembly and is passed on immediately to the Load Control circuit. Refer to Figure 168-5.

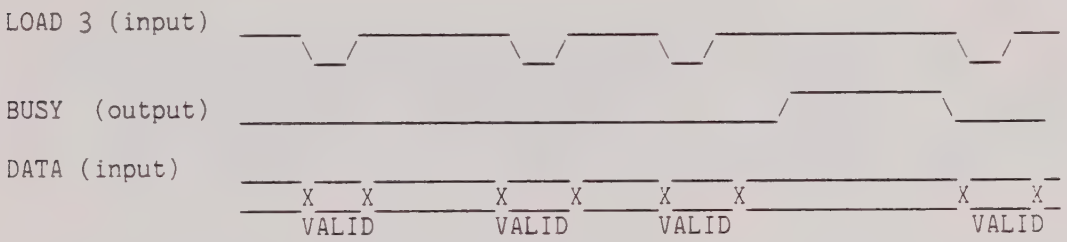


Figure 168-5. Handshake Three Timing Diagram

Load Control Logic

The load control circuit accepts the STORE signal from any of the three handshake circuits and develops a LOAD pulse to the data storage register to strobe in the external data. The load control circuit also prevents loading during a read cycle.

Three flip-flops within U22, and gates U16 and U17 comprise the load control logic. The load control logic is a sequential circuit that accepts a STORE signal from the handshake circuits and a READ signal from the microcomputer and generates a LOAD signal to the data storage register.

Upon initialization, flip-flops A, B, and C are in the reset state. One clock pulse later, C becomes set and arms gate U16 in anticipation of a STORE command. When the STORE command occurs, flip-flops A and B are set, and they remain set until the command is terminated. The Q outputs of flip-flops A and B are ANDed through U17 which, in turn, forms the D input to flip-flop C and generates the leading edge of the load strobe to the data storage register. Flip-flop C, with its D input at a logic zero, is reset on the clock pulse and therefore generates the trailing edge of the load strobe.

When the LOAD command terminates, the sequential machine returns to the quiescent state where it waits for the next command. When the READ signal is received, flip-flops A and B are prevented from changing state, therefore a load strobe can not be generated.

Single/Continuous Control Circuit

The single/continuous control circuit determines whether data is loaded either continuously, or only once between reads by the system controller. The single/continuous logic consists of flip-flop U25 and several gates in U14 and U23. If the board is in the continuous mode, the flip-flop is held in the reset state and does not effect the board operation.

If, however, the single mode has been selected, the flip-flop is set upon receipt of the first load command from an external device. When the flip-flop is set, the signal HANDSHAKE ENABLE becomes false, and the three handshake circuits are held in the reset state until the latched data is read. Following the read, the flip-flop is reset and the process may repeat.

PARALLEL INPUT AND OUTPUT INTERFACE

A temporary data storage register comprised of three 8-bit latches (U6, U29, and U40) is the focal point for all parallel data transfer between the Digital I/O Assembly and external devices. Since parallel data transfer operations are different for each of the operating modes (status input, status output, and digital input), the interface circuit will be discussed in terms of the selected operating mode.

Because the Digital I/O Assembly may be user-configured to perform three different functions, the microcomputer must determine which function has been selected. Upon power-up, or when the system controller requests configuration, microcomputer port 2, bit 6, goes to logic zero which gates the three most significant bits of the parallel input word onto the internal data bus. A READ strobe is then issued to accept the data, and port 2, bit 6, returns to the logic one state.

If the assembly is used for status input (with a Digital/Status Input connector, 2280A-179), then it must fetch the user input data when commanded. The first step is to gate the external data, buffered through U41, U42, U43, and U44, to the inputs of the set of latches, U6, U29, and U40. Gating is accomplished by placing port 2, bit 6, in the logic zero state to place the input data on the inputs of the three latches. Next, port 2, bit 7, is pulsed from high to low and back to high to strobe the data into the latches. Port 2, bits 0 through 2, are then sequentially placed in the logic zero state and returned to the logic one state. At the same time, a READ strobe is issued and the data is brought into the processor through buffers U36, U37, U38, and U39.

If the assembly is used for status output (with a Status Output Connector, 228A-179), operation is directly analogous to the status input configuration. In the status output configuration, port 2, bits 6 and 7, are placed in the logic one state and port 2, bits 0 through 2, are sequentially placed in the logic zero state then returned to the logic one state. While each port bit is in the logic zero state, a WRITE strobe is issued to clock the output data from the processor into the appropriate latch through buffers U30, U31, U32, and U33.

The digital input configuration operates exactly like the status input configuration except that there is no need to store the data in the on-board latches since it has already been stored there through the action of the handshake sequence.

Outputs from the Digital I/O assembly are buffered to the external circuitry though buffers U46, U47, and U48. Data inputs to the assembly are buffered through U41, U42, U43, and U44.

GENERAL MAINTENANCE

The Digital I/O PCA normally requires no cleaning, but if dirt, dust, or other contamination is visible on the surface, the PCA should be cleaned. Follow PCA cleaning instructions in Section 4 of this manual.

PERFORMANCE TESTS

The following performance tests verify proper operation of the Digital I/O Assembly. There are two tests; each is related to one of the two possible input connectors that may be used with the Digital I/O Assembly. Both tests (with both connectors) are necessary to fully test the Digital I/O Assembly under all conditions, but either test may be performed independently for a partial performance evaluation. The two performance tests are:

- Output Test

  The Output Test verifies operation of the Digital I/O Assembly's output capability. This test requires the use of Option 2280A-169 Status Output Connector.

- Input Test

  The Input Test verifies operation of the Digital I/O Assembly's input capability. This test requires the use of Option 2280A-179 Digital/Status Input Connector.

Output Test

1. Turn the 2280 front panel keyswitch to the POWER OFF position. Disconnect the Data Logger power input and all other high voltage inputs.

2. Install a Calibration/Extender Fixture in the uppermost Data Logger option slot.

3. Set the Digital I/O channel decade switches to 0, then install the Digital I/O Assembly on the Calibration/Extender Fixture.

4. Install the Status Output Connector on the Digital I/O Assembly.

5. Reconnect the Data Logger power input.

6. Turn the keyswitch to the PROGRAM position.

7. Program the Data Logger to initialize the system and toggle all channels of the status output using single scan by performing the steps given in Table 168-2.

Table 168-2. Output Test Programming Steps

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
.		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
7	C0..19	CHANNEL NUMBER (OR BLOCK) = C0..19
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
10	S	A(S) STATUS OUTPUT
11	ENTER	ZERO RESULT LABEL <14 CHRS MAX>= ZERO
12	ENTER	NON-ZERO RESULT LABEL <14 CHRS MAX>= ONE
13	ENTER	AS: CHANNEL MENU CHOICE <1-5>? 1
14	3	AS<3> CHANNEL PROCEDURE
15	ENTER	CP:
16	CX=1-CX	CP: CX=1-CX
17	ENTER	CP:
18	ENTER	AS: CHANNEL MENU CHOICE <1-5>? 4
19	EXIT	A: CHANNEL FUNCTION <A-Z>? S
20	EXIT	CHANNEL NUMBER (OR BLOCK)= C0..19
21	EXIT	MAIN MENU CHOICE <M FOR MENU>? A
22	K	<K> PROGRAM A SCAN GROUP
23	ENTER	SCAN GROUP NUMBER= 0
24	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
25	ENTER	K: SCAN GROUP MENU CHOICE <1-5>?
26	2	K<2> SCAN GROUP CHANNEL LIST
27	ENTER	CL:
28	C0..19	CL: C0..19
29	ENTER	CL:
30	ENTER	K: SCAN GROUP MENU CHOICE <1-5>? 3
31	ENTER	K3: TRIGGER MODE <1-5>? 1
32	ENTER	K: SCAN GROUP MENU CHOICE <1-5>? 4
33	ENTER	K4: DEVICE <1-5>? 1
34	2	K4<2> PRINTER
35	ENTER	K42: TYPE OF DATA <1-4>? 1
36	2	K42<2> ALL DATA
37	ENTER	K4: DEVICE <1-5>? 3
38	EXIT	K: SCAN GROUP MENU CHOICE <1-5>? 5
39	EXIT	SCAN GROUP NUMBER= 0
40	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

8. Connect the DMM leads to channel 0 on the output connector. Set the DMM to a diode-checking range. Read the resistance across the terminals, and record the reading.

9. Press SINGLE SCAN, then 0, then ENTER.

10. Verify that the resistance reading on the DMM is lower than the resistance reading taken in step 8.

12. Press SINGLE SCAN, then 0, then ENTER.

13. Verify a DMM reading close to the one taken in step 8.

14. Repeat steps 8 through 13 for each channel (channels 1 through 19).

15. The Digital I/O Assembly output test is complete.

Input Test

1. Turn the 2280 front panel keyswitch to the POWER OFF position. Disconnect the Data Logger power input and all other high voltage inputs.

2. Install a Calibration/Extender Fixture in the uppermost option slot of the Data Logger.

3. Install the Digital I/O Assembly on the Calibration/Extender Fixture.

4. Short signal to return on terminal 21 of the Digital/Status Input Connector. Remove all other connections. Install the input connector on the Digital I/O Assembly.

5. Reconnect the Data Logger power input.

6. Turn the keyswitch to the PROGRAM position.

7. Program the Data Logger to scan the status input channels using the steps given in Table 168-3.

Table 168-3. Input Test Programming Steps

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>?
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
7	0..19	CHANNEL NUMBER (OR BLOCK) = C0..19
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
10	I	A<I> STATUS INPUT
11	ENTER	ZERO RESULT LABEL <14 CHRS MAX> = ZERO
12	ENTER	NON-ZERO RESULT LABEL <14 CHRS MAX> = ONE
13	ENTER	AI: CHANNEL MENU CHOICE <1-5>? 1
14	EXIT	A: CHANNEL FUNCTION <A-Z>? I
15	EXIT	CHANNEL NUMBER (OR BLOCK) = C0..19
16	EXIT	MAIN MENU CHOICE <M FOR MENU>? A
17	K	<K> PROGRAM A SCAN GROUP
18	ENTER	SCAN GROUP NUMBER = 0
19	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
20	ENTER	K: SCAN GROUP MENU CHOICE <1-5>? 1
21	2	K<2> SCAN GROUP CHANNEL LIST
22	ENTER	CL:
23	C0..19	CL: C0..19
24	ENTER	CL:
25	ENTER	K: SCAN GROUP MENU CHOICE <1-5>? 3
26	ENTER	K3: TRIGGER MODE <1-5>? 1
27	3	<K3> CONTINUOUS SCAN
28	ENTER	K: SCAN GROUP MENU CHOICE <1-5>? 4
29	ENTER	K4: DEVICE <1-5>?1
30	2	K4<2> PRINTER
31	ENTER	K42: TYPE OF DATA <1-4>? '
32	2	K42<2> ALL DATA
33	ENTER	K4: DEVICE <1-5>? 3
34	EXIT	K: SCAN GROUP MENU CHOICE <1-5>? 5
35	EXIT	SCAN GROUP NUMBER =0
36	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

8. Press SCAN. The Data Logger should continuously print the status of the 20 input channels.

9. On the input connector, sequentially short the SIGNAL terminal to the RETURN terminal for each channel (0 through 19). Verify the the value returned for each channel with the two terminals shorted is 0.

10. The input test is complete.

CALIBRATION

The Digital I/O Assembly requires no calibration.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the Digital I/O Assembly is given in Table 168-4. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the Digital I/O Assembly is given in Figure 168-6.

TABLE 168-4. 2280A-168 DIGITAL I/O PCA
(SEE FIGURE 168-6.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q
C 1		CAP,AL,330UF,+100-10%,25V	614404	89536	614404	1	
C 2, 3		CAP,CER,1000PF,+-10%,500V,X5S	357806	56289	C016B102G102K	2	
C 4		CAP,POLYES,0.22UF,+-10%,100V	436113	73445	C280MAH1A220K	1	
C 5		CAP,AL,270UF,+100-10%,20V	602656	89536	602656	1	
C 8- 19, 22-		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	25	
C 31, 33- 35			519157				
C 20		CAP,AL,470UF,+100-10%,12V	602649	89536	602649	1	
C 21		CAP,TA,0.47UF,+-20%,35V	161349	56349	196D474X0035HA1	1	
C 32		CAP,TA,10UF,+-20%,20V	330662	56289	196D106X0020KA1	1	
C 36		CAP,CER,0.01UF,+-20%,100V,X7R	407361	72982	8121-A100-W5R-103M	1	
CR 1- 8	*	DIODE,SI, 50 PIV, 1.0 AMP	379412	04713	1N4933	8	
CR 9, 11, 13	*	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	3	2
CR 10, 12	*	DIODE,SI, 20 PIV, 1.0 AMP	507731	83003	VSK120	2	1
F 1		FUSE,PICO,FAST,0.5A,125V	603274	71400	GFA	1	1
H 1		NUT,MACH,HEX,STL,4-40	110635	89536	110635	4	
H 2		WASHER,LOCK,SPLIT,STEEL,#4	110395	89536	110395	4	
H 3		WASHER,FLAT,STEEL,#5,0.032 THK	195909	89536	195909	4	
H 4		STUD,THREADED,PENN KFH,4-40,.500	494682	89536	494682	2	
H 5		BROACHING TYPE, L=.750 DASH#12,4-40	614636	89536	614636	2	
H 6		NYLON, STEM:OD=.093", L=.115"	658450	89536	658450	1	
L 2		CHOKE 550UH	645721	89536	645721	1	
MP 1		RETAINER,P.C.B.	579078	89536	579078	2	
MP 2		SPACER,RND,ALUM,0.156IDX0.250	153155	89536	153155	2	
MP 3		SPACER,MOUNT,NYLON,	175125	89536	175125	1	
MP 4		BAG,SHIELDING,TRANSPARENT,12"X16"	680983	89536	680983	1	
Q 1	*	SILICON, NPN, FAST SWITCHING D44H11	535542	89536	535542	1	1
Q 2	*	TRANSISTOR,SI,NPN,HI-VOLTAGE	370684	04713	MPS A 42	1	1
Q 3- 5	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	195974	64713	2N3906	3	1
Q 6	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	1	1
R 1		RES,CF,1.8K,+-5%,0.25W	441444	80031	CR251-4-5P1K8	1	
R 2		RES,CF,1.5K,+-5%,0.25W	343418	80031	CR251-4-5P1K5	1	
R 3		RES,CF,330,+-5%,0.25W	368720	80031	CR251-4-5P330E	1	
R 4		RES,CF,510,+-5%,0.25W	441600	80031	CR251-4-5P510E	1	
R 5, 6, 9,		RES,MF,4.99K,+-1%,0.125W,100PPM	168252	91637	MFF1-84991	4	
R 10			168252				
R 7		RES,MF,16.9K,+-1%,0.125W,100PPM	267146	91637	CMF551692F	1	
R 8, 24- 26		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	4	
R 11		RES,VAR,CERM,1K,+-10%,0.5W	275750	11236	360T-102A	1	
R 12, 13, 18,		RES,CF,51,+-5%,0.25W	414540	80031	CR251-4-5P51E	4	
R 19			414540				
R 14, 15, 22,		RES,CF,270,+-5%,0.25W	348789	80031	CR251-4-5P270E	5	
R 38, 39			348789				
R 16, 17, 23,		RES,CF,5.6K,+-5%,0.25W	442350	80031	CR251-4-5P5K6	4	
R 27			442350				
R 20, 21		RES,CF,30,+-5%,0.25W	442228	80031	CR251-4-5P30E	2	
R 28		RES,MF,154K,+-1%,0.125W,100PPM	289447	91637	CMF551543F	1	
R 29, 35		RES,CF,1M,+-5%,0.25W	348987	80031	CR251-4-5P1M	2	
R 30, 34, 36		RES,MF,10K,+-1%,0.125W,100PPM	168260	91637	CMF551002F	3	
R 31		RES,MF,26.7K,+-1%,0.125W,100PPM	245779	91637	CMF552672F	1	
R 32		RES,CF,2K,+-5%,0.25W	441469	80031	CR251-4-5P2K	1	
R 33		RES,MF,332K,+-1%,0.125W,100PPM	289504	91637	CMF553323F	1	
R 37		RES,CF,20K,+-5%,0.25W	441477	80031	CR251-4-5P20K	1	
R 40- 42		RES,CF,82,+-5%,0.25W	442277	80031	CR251-4-5P82E	3	
S 1		SWITCH,ROTARY,1 POLE,16 POS,1 THUMB	615096	97527	1A-21-60-33-G-F	1	1
S 2		SWITCH,ROTARY,1 POLE,10 POS,1 THUMB	602888	97527	1A-21-60-02-G-F	1	
T 1		INVERTER TRANSFORMER	617803	89536	617803	1	
TP 1, 2, 20,		CONN,TAB,FASTON,PRESS-IN,0.110 WIDE	512889	02660	62395	12	
TP 23, 24, 30-			512889				
TP 32, 50, 58,			512889				
TP 82, 83			512889				
U 1	*	IC,REGULATING PULSE WIDTH MODULATOR	454678	01295	SG3524N	1	1
U 2	*	IC,BPLR,DUAL DIFF LINE DRVR W/3-STATE	586081	12040	DS1692J	1	1
U 3	*	IC,BPLR,DIFFERENTIAL LINE RECEIVER	586073	01295	SN55182J	1	1
U 4	*	ISOLATOR,OPTO,HI-SPEED,DUAL	429894	28480	5082-4355	1	1
U 5	*	ISOLATOR,OPTO,HI-SPEED,8 PIN DIP	354746	89536	354746	1	1
U 6, 29, 40	*	IC,CMOS,DUAL 4BIT LTCH W/STROBE&RESET	605261	04713	MC14508BCP	3	1
U 7		IC,NMOS 8-BIT UCOMP W/PROG. EPROM	655563	89536	655563	1	
U 8	*	IC,CMOS,UNIV ASYNC RECEIVR/TRANSMITER	453464	32293	1M6402CPL	1	1
U 9	*	IC,LSTTL,QUAD 2 INPUT NOR GATE	642884	01295	SN54LS02J	1	
U 10	*	IC,LSTTL,QUAD 2 INPUT OR GATE	605618	01295	SN54LS32J	1	1
U 11	*	IC,LSTTL,QUAD 2 INPUT NAND GATE	605600	01295	SN54LS00J	1	1
U 12, 19	*	IC,CMOS,HEX INVERTER	404681	02735	CD4069BE	2	1
U 13	*	IC,CMOS,TRIPLE 3 INPUT NAND GATE	375147	02735	CD4023UBE	1	1
U 14, 26	*	IC,CMOS,QUAD 2 INPUT OR GATE	408393	02735	CD4071BE	2	1

TABLE 168-4. 2280A-168 DIGITAL I/O PCA
(SEE FIGURE 168-6.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q
U 15, 16	*	IC,CMOS,QUAD 2 INPUT NOR GATE	355172	02735	CD4001AE	2	1
U 17	*	IC,CMOS,QUAD 2 INPUT NAND GATE	453241	02735	CD4011BE	1	1
U 18, 23	*	IC,CMOS,TRIPLE 3 INPUT NOR GATE	355180	02735	CD4025AE	2	1
U 20, 21, 25	*	IC,CMOS,DUAL JK F/F,+EDG TRIG	355230	02735	CD4027AE	3	1
U 22	*	IC,CMOS,QUAD D F/F,+EDG TRG	536292	04713	MC14175B	1	1
U 24	*	IC,COMPARATOR,DUAL,LO-PWR,8 PIN DIP	478354	12040	LM393N	1	1
U 27, 28, 30-	*	IC,CMOS,HEX BUFFER W/3-STATE OUTPUT	407759	12040	MM80C97N	14	1
U 33, 36- 39,	*		407759				
U 41- 44	*		407759				
U 34	*	IC,CMOS,7STAGE RIPPLE CARRY BIN CNTR	412965	86684	CD4024AE	1	3
U 35, 45	*	IC,CMOS,QUAD XOR GATE	355222	02735	CD4030AE	2	1
U 46- 48	*	IC,ARRAY,7 TRANS,NPN,DARLINGTON PAIRS	454116	01295	ULN2003	3	1
VR 1	*	ZENER,UNCOMP, 24.0V, 5%, 5.2MA, 0.4W	267807	04713	1N970B	1	1
VR 2	*	ZENER,UNCOMP,6V TRANSIENT SUPPRESSOR	508655	24444	1N5908	1	1
VR 3	*	IC, 1.22V,100 PPM T.C.,BANDGAP REF	452771	89536	452771	1	1
XU 7, 8		SOCKET,DIP,0.100 CTR,40 PIN	429282	09922	DILB40P-108	2	
Y 1	*	CRYSTAL,6MHZ,+-0.01%,HC-18/U	461665	89536	461665	1	5
Z 1- 3		RES,NET,SIP,8 PIN,7 RES,10K,+-2%	412924	80031	95081002CL	3	
Z 4, 5		RES,NET,SIP,10 PIN,9 RES,10K,+-2%	414003	80031	95081002CL	2	
Z 7, 9, 11,		RES,NET,DIP,14 PIN,7 RES,100K,+-5%	516930	89536	516930	6	
Z 14, 16, 18			516930				
Z 8, 10, 12,		RES,NET,SIP,8 PIN,7 RES,47K,+-2%	413286	89536	413286	6	
Z 13, 15, 17			413286				

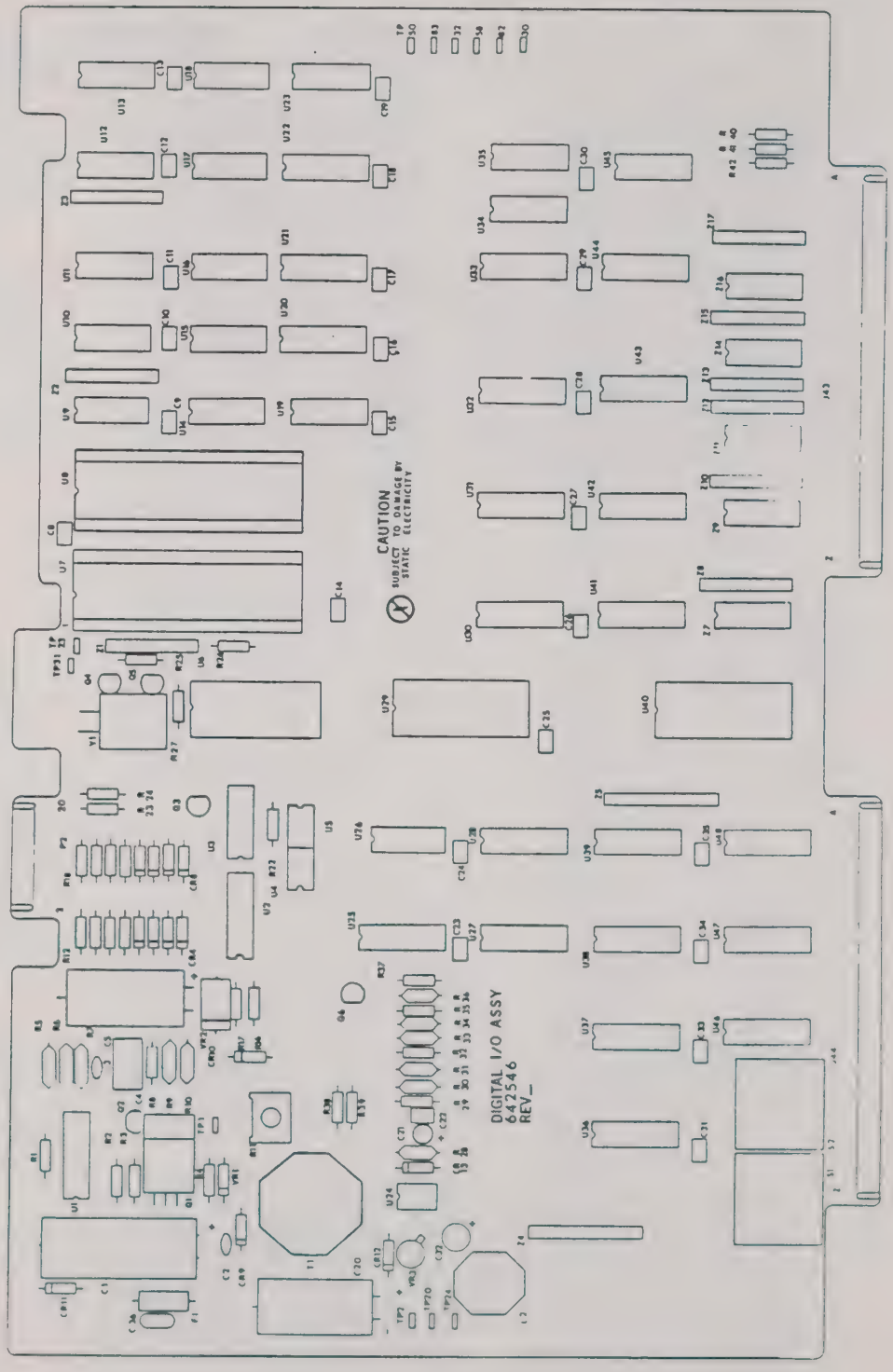
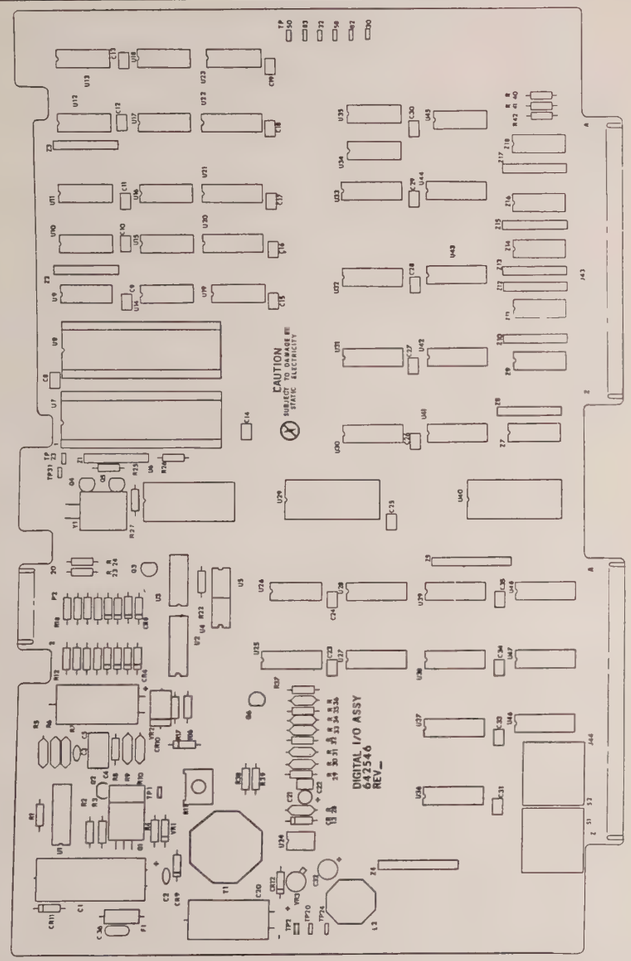


Figure 168-6. 2280A-168 Digital I/O PCA



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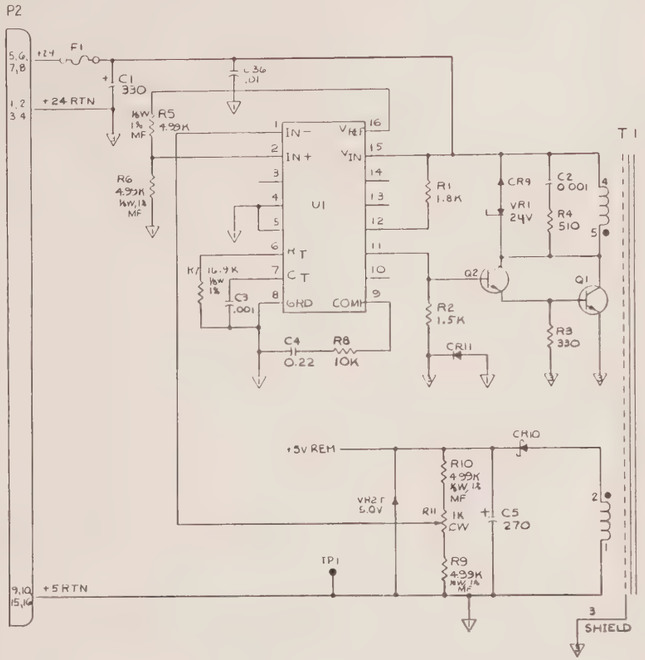
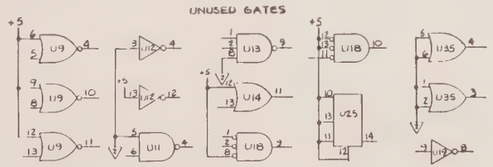
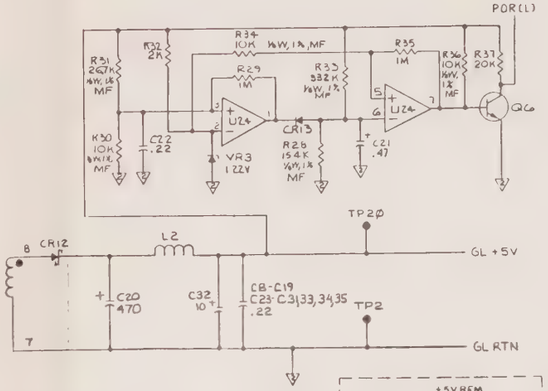
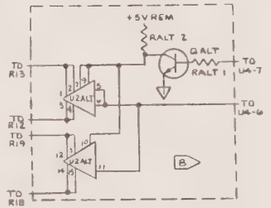






NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4W, 5% AND ALL RESISTANCE ARE IN OHMS.
2. ALL CAPACITANCE IS IN MICROFARADS.
3. ALL GRAPHIC SYMBOLS ARE IN ACCORDANCE WITH ANSI Y32.2 AND Y32.14.



PWR & GND				
I C	Ø +5V			+5V REM
U1		8 4 5		1
U2		8 1 5		
U3		1 3 7		
U4		5		
U5	8		5	
U6	24		12 Ø	
U7	26 40		20 7	
U8	37 38 39 1		6 Ø	
U9	14 6 9 12		7	
U10	14		74	
U11	14		75	
U12	13 14		37	
U13	14		7 8	
U14	12 14		7	
U15	14		7	
U16	14		7	
U17	14		7	
U18	12 13 14 6		7	
U19	9 6		7	
U20	16		7 8 9	
U21	16		7 8 9	
U22	16		8	
U23	14		7	
U24	8		4	
U25	10 11 12 13 14		7 8	
U26	14		7	
U27	16		8 Ø	
U28	10 12 16		8 12	
U29	24		3 12 6	
U30	16		2 4 8	
U31	16		8	
U32	16		8	
U33	16		8	
U34	14		8	
U35	14		14 5 6 3	
U36	6 16		8	
U37	16		8	
U38	16		8	
U39	24		3 12 15	
U40	16		8	
U41	16		8	
U42	16		8	
U43	16		8	
U44	16		8	
U45	14		7	
U46			1 8	
U47			8	
U48			8	
U49	16			

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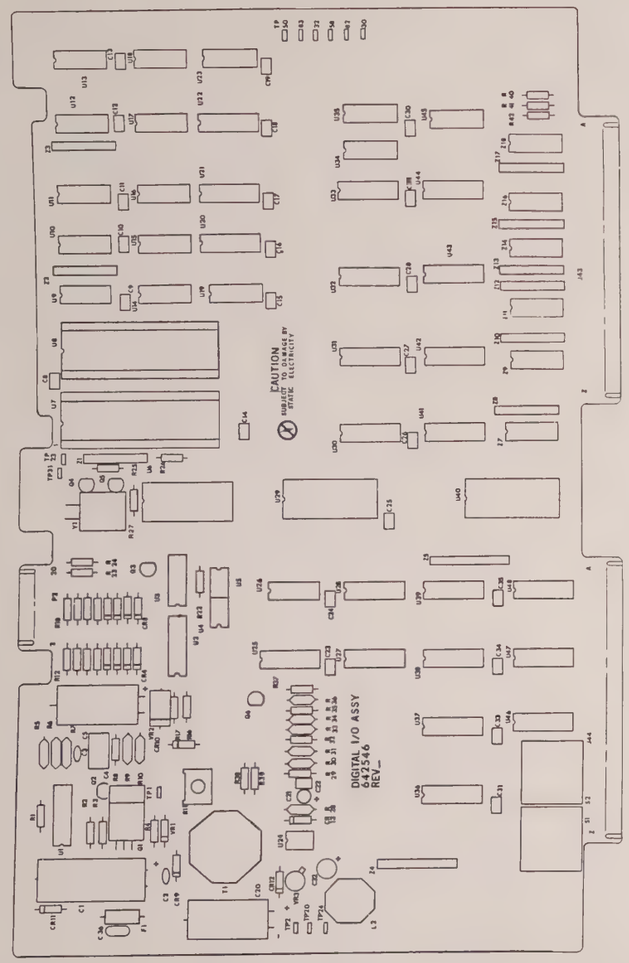
Figure 168-6. Digital I/O Assembly Schematic Diagram



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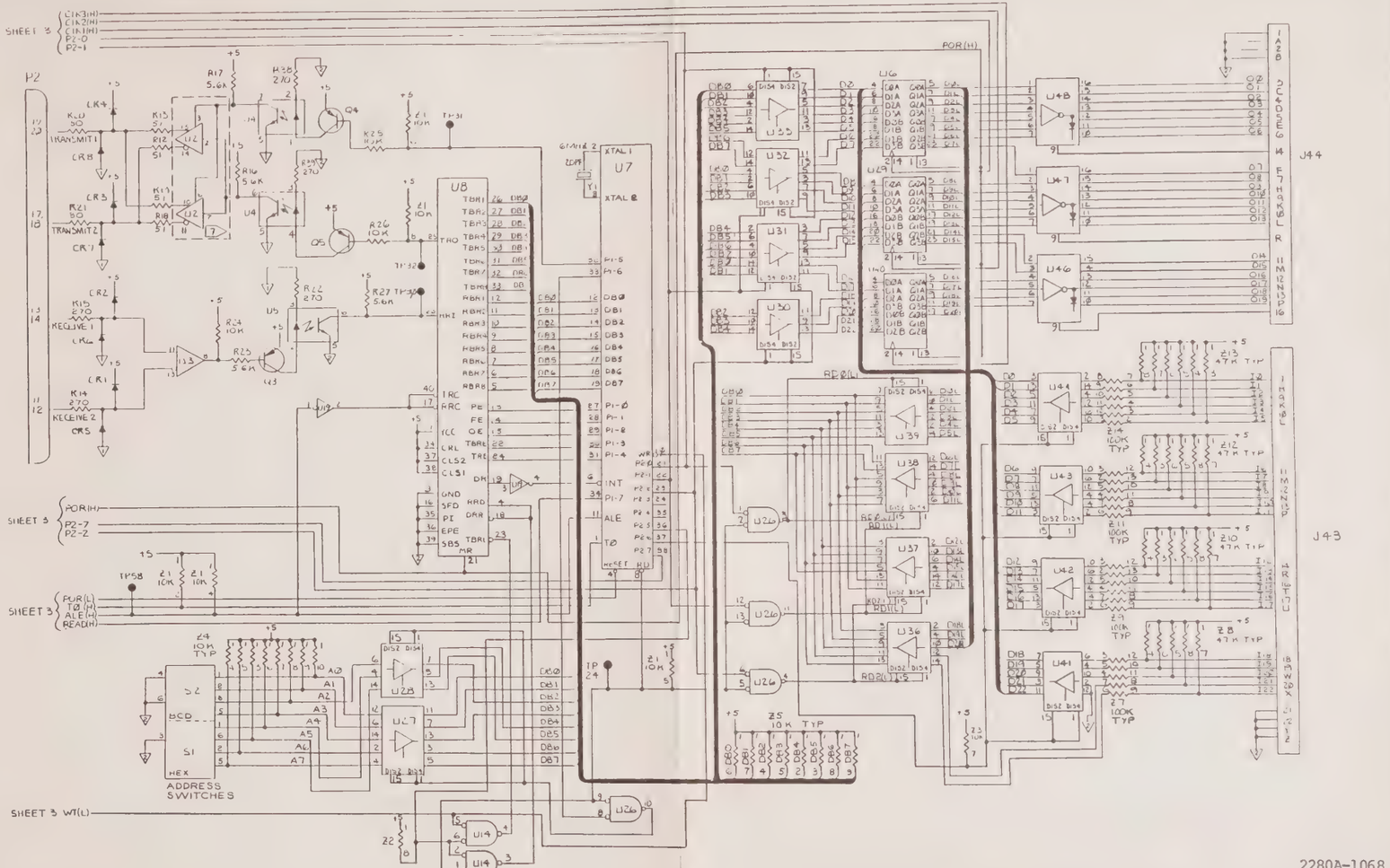

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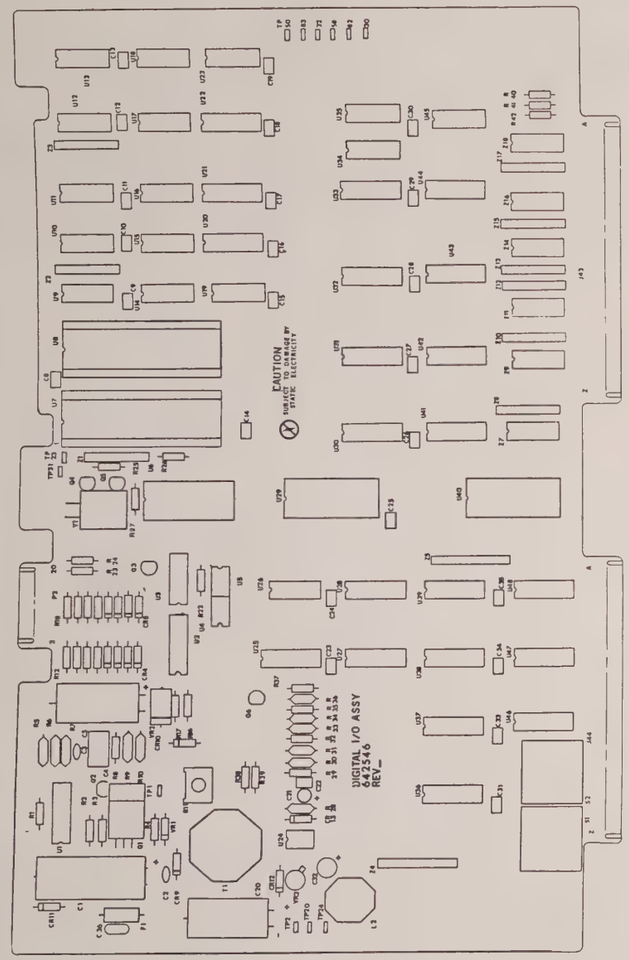
Figure 168-6. Digital I/O Assembly Schematic Diagram (cont.)



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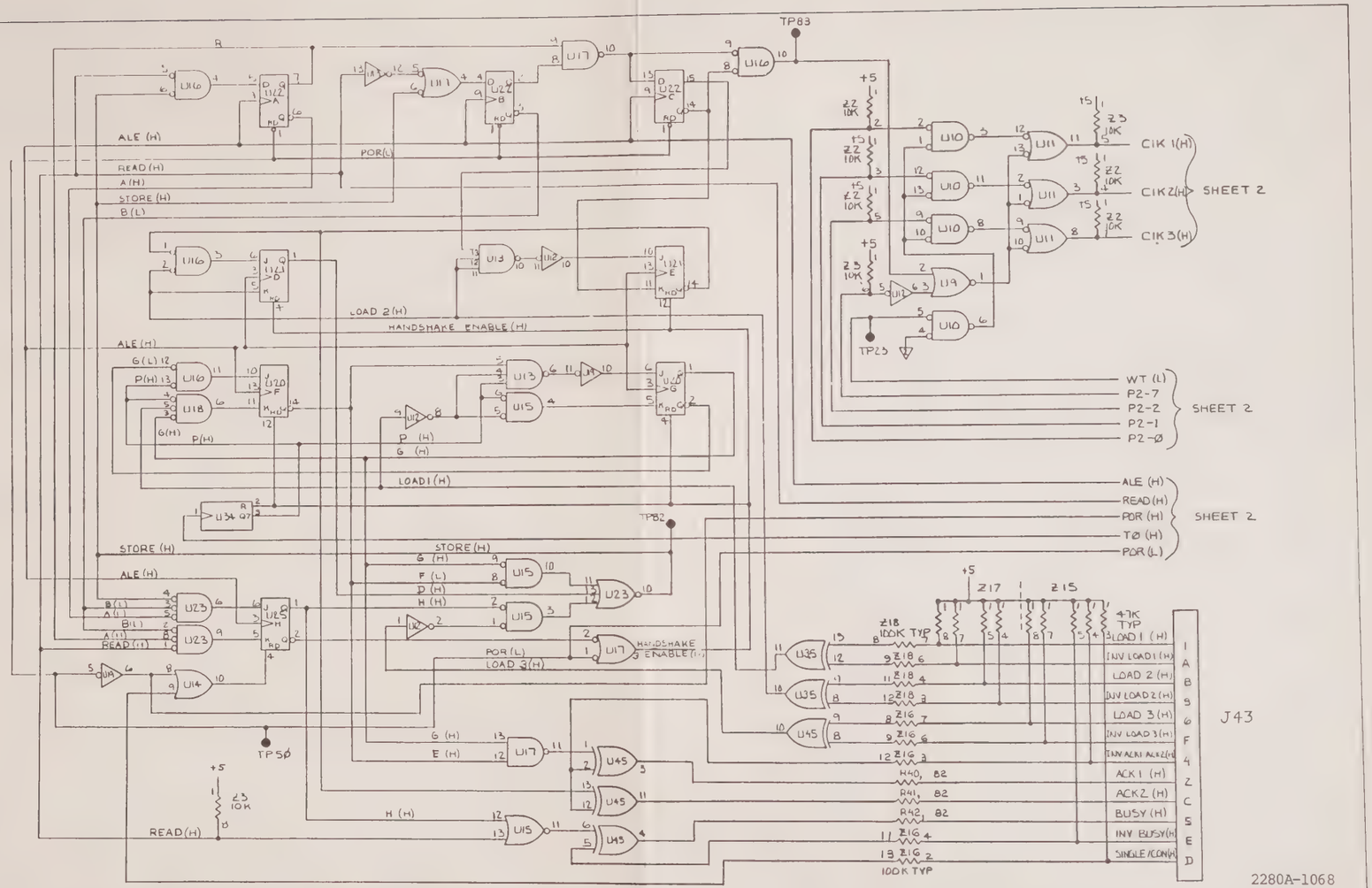

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Figure 168-6. Digital I/O Assembly Schematic Diagram (cont.)

Option 2280A-169
Status Output Connector

DESCRIPTION

The Status Output Connector provides connection for 20 single-bit output signals from the Digital I/O Assembly (Option 2280A-168) to external points. Each output channel is individually selectable by the Data Logger and can be used to drive lamps or relays, or to change logic levels. Figure 169-1 shows the Status Output Connector.

The Status Output Connector plugs onto the 44-pin card-edge connector on the left side of the rear edge of the Digital I/O Assembly. The connector assembly is enclosed in a plastic housing that protects the terminals and provides strain relief for the external wiring. Retaining screws on each side of the housing fasten the connector assembly to the rear of the data logger.

WHERE TO FIND FURTHER INFORMATION

The Status Output Connector theory of operation, general maintenance, performance test, calibration procedure, parts list, and schematic diagram are located in this subsection. Installation and system configuration instructions are located in the 2280 Series System Guide.

THEORY OF OPERATION

The Status Output Connector theory of operation consists only of a short functional description of the Status Output Connector. The schematic diagram at the end of this option subsection provides a circuit reference and should answer most questions.

Overall Functional Description

The connector provides terminals for connecting wiring to equipment that is to be controlled by data logger status outputs. Output, return, and flyback diode clamp terminals are provided on the connector.

GENERAL MAINTENANCE

The Status Output Connector PCA normally does not require cleaning unless dirt, dust, or other contamination is visible on the surface. To clean the pcb, follow the cleaning instructions in Section 4 of this manual.

PERFORMANCE TEST

The Status Output Connector is tested using the 2280A-168 Digital I O Assembly output mode performance test located in the 2280A-168. Digital I/O Assembly subsection of this manual.

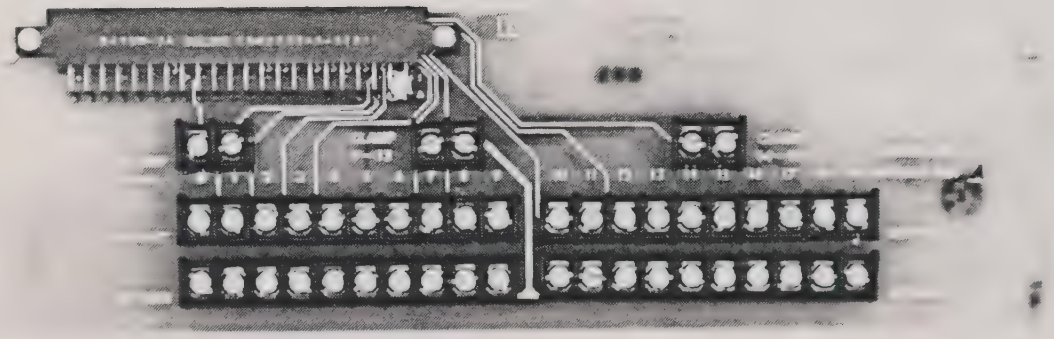


Figure 169-1. Status Output Connector

CALIBRATION

The Status Output Connector does not require calibration adjustment.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the Status Output Assembly is given in Table 169-1. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the Status Output Assembly is given in Figure 169-2.

TABLE 169-1. 2280A-169 STATUS OUTPUT CONNECTOR
(SEE FIGURE 169-2.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	RS -Q	NOT -E
H 1		STEEL,CAD.PLATED,.125X .500	276493	89536	276493	2		
H 2		WASHER,FLAT,STEEL,#4,0.030 THK	147728	89536	147728	2		
MP 1		CONNECTOR HOUSING TOP	578971	89536	578971	1		
MP 2		CONNECTOR HOUSING BOTTOM	656876	89536	656876	1		
MP 3		DECAL, STATUS OUTPUT CONNECTOR	634568	89536	634568	1		
MP 4		DECAL, OPTION -169	634485	89536	634485	1		
MP 5		TAPE, FOAM, PVC, 1/4W 3/8 THK	603134	89536	603134	1		
P 44		CONN,PWB EDGE,REC,90,0.156 CTR,44 POS	614313	89536	614313	1		
TB 1- 4		SINGLE ROW, .325 CENTERS, 10 POSITION	615328	89536	615328	4		
TB 5- 7		SINGLE ROW, .325 CENT., PCB MOUNT,	643858	89536	643858	3		

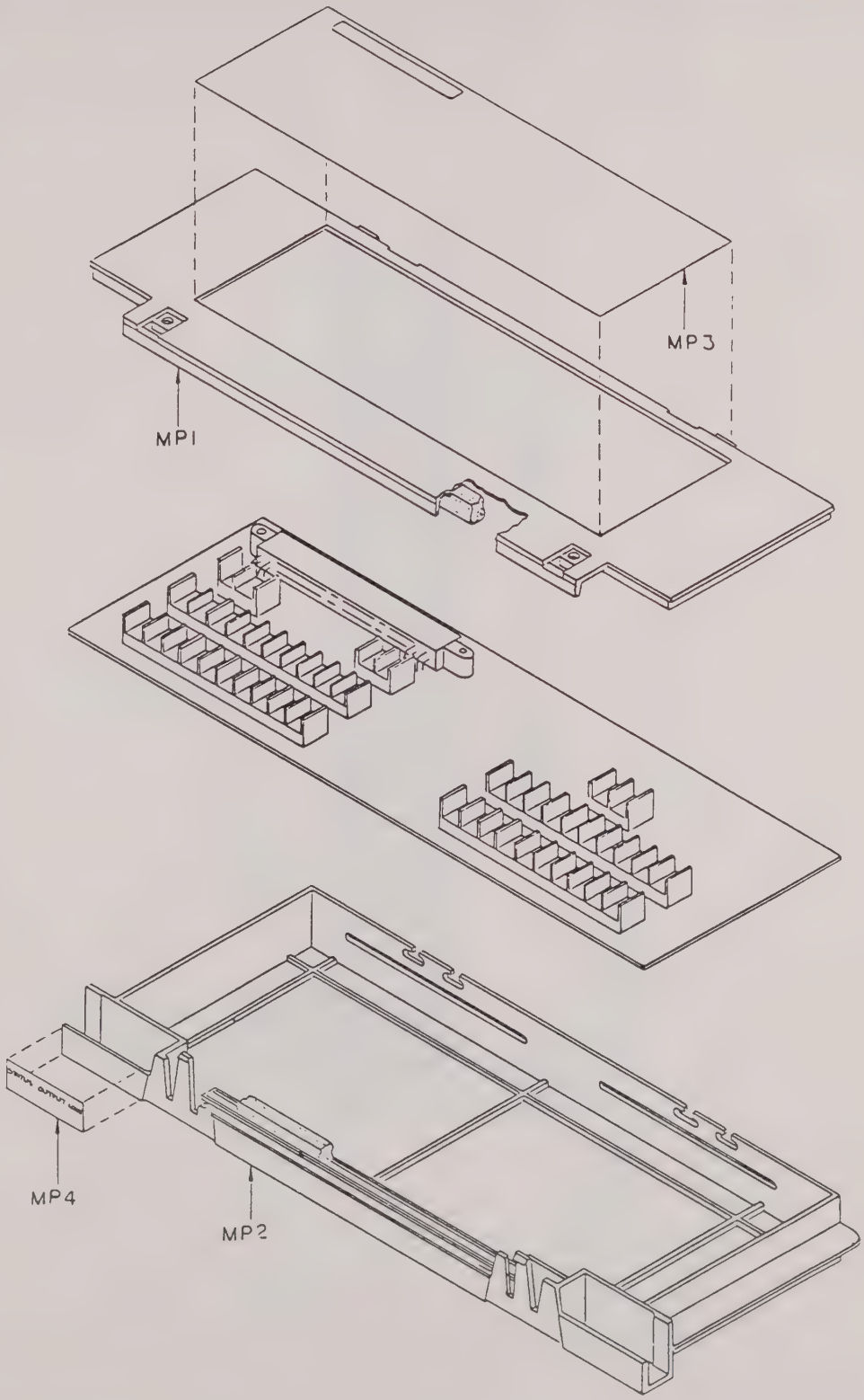


Figure 169-2. 2280A-169 Status Output Connector

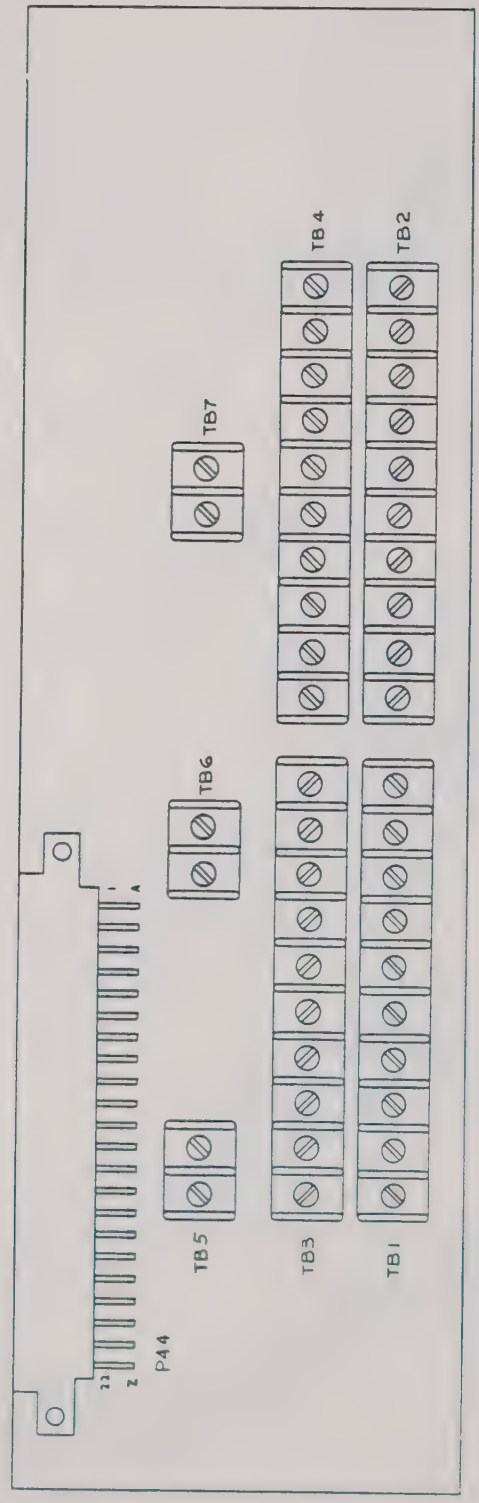
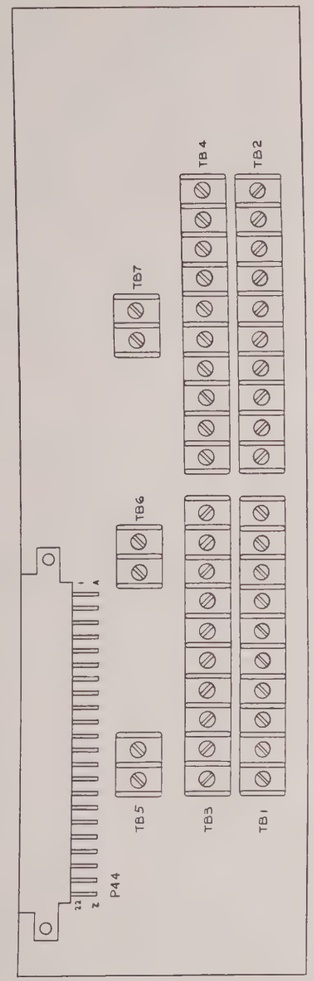


Figure 169-2. 2280A-169 Status Output Connector (cont.)



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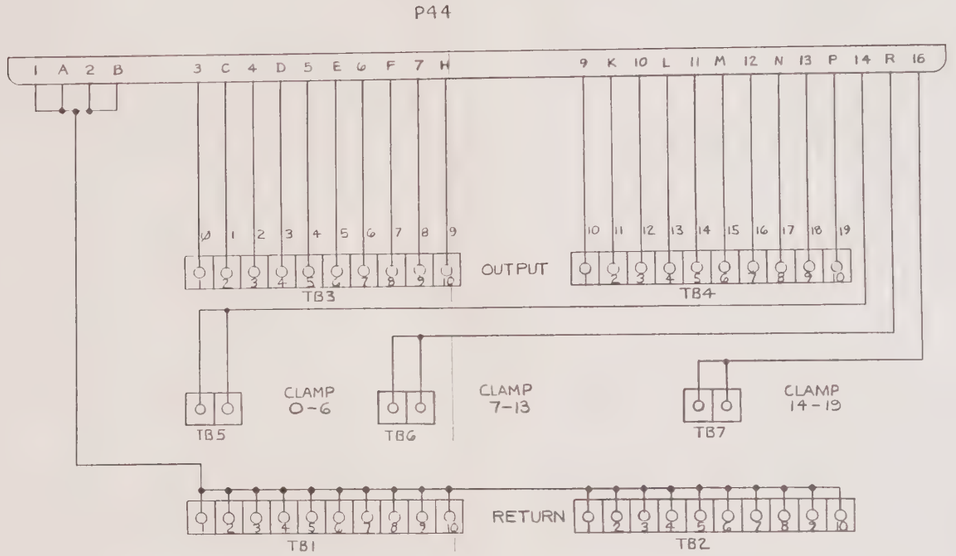

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Figure 169-2. Status Output Connector Schematic Diagram

SECTION 9

OPTIONS -170 THROUGH -179

CONTENTS

Option 2280B-170 Analog Output 170-1
Option 2280A-171 Current Input Connector 171-1
Option 2280A-174 Transducer Excitation Connector 174-1
Option 2280A-175 Isothermal Input Connector 175-1
Option 2280A-176 Voltage Input Connector 176-1
Option 2280B-177 RTD/Resistance Input Connector 177-1
Option 2280A-179 Digital/Status Input Connector 179-1

DESCRIPTION

Analog outputs are available from the mainframe through the Analog Output option, illustrated in Figure 170-1. The analog outputs provide voltage and current signals for use in driving chart recorders or other equipment that requires an analog input. There are four output channels on each board. All four output channels are electrically isolated from chassis ground, but not from each other. The four outputs share common returns and voltage references. Each channel will supply 0 to +10V, -5 to +5V, and 4 to 20 mA. Only one type of output is allowed per channel at a given time.

WHERE TO FIND ADDITIONAL INFORMATION

In this subsection, the Analog Output Option theory of operation, general maintenance, performance tests, calibration procedure, a parts list, and a schematic diagram are given. Installation and system configuration instructions are given in the 2280 Series System Guide, and operating and programming instructions are given in the 2280 Series User Guide.

Test equipment required to perform the procedures in this subsection is listed in Table 170-1. A summary of test equipment required to perform all procedures in this manual is given in Table 1-1 in Section 1 of this manual.

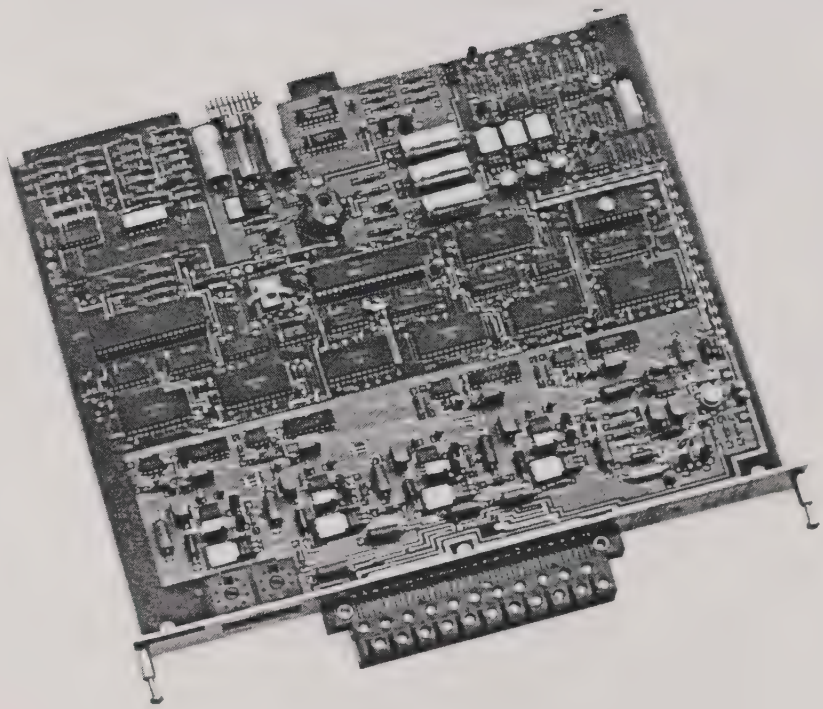


Figure 170-1. Analog Output Option

Table 170-1. Required Test Equipment

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
Digital Multimeter	+/- 10V +/- 0.0001V	Fluke 8505A
Calibration and Extender Fixture	.....	Fluke Y2056

THEORY OF OPERATION

The Analog Output Option theory of operation includes a functional description, a block diagram description, and a detailed circuit description. The schematic diagram for this assembly is given at the end of this option subsection.

Functional Description

The analog output consists of four primary sections; a power supply, serial link communication, digital control, and digital to analog conversion circuitry. Figure 170-2 is a block diagram showing the interrelationship between these sections. The communication circuitry is responsible for receiving and transmitting information to the mainframe via the serial link. The digital control circuitry directs the serial link communications and delivers a 12 bit data word received from the mainframe to the selected analog output circuitry. The analog circuitry converts this digital word to its corresponding voltage and current output.

Block Diagram Description

Communication circuitry includes: a serial link driver and receiver, three optical couplers, and a UART. Information is received from the serial link by a receiver chip. The information is then transferred, using optical coupler isolation, to the UART in serial form. The UART converts the serial data to eight bit data words to be read by the uP. When a data word is ready, the UART interrupts the microprocessor. The microprocessor then reads the data supplied by the UART from the data bus, while checking for errors. To transmit data, the microprocessor loads information from the data bus into the UART and enables the transmit circuitry. When the transmit circuitry is enabled, the data is transferred, through an optical coupler, to the driver and onto the serial link.

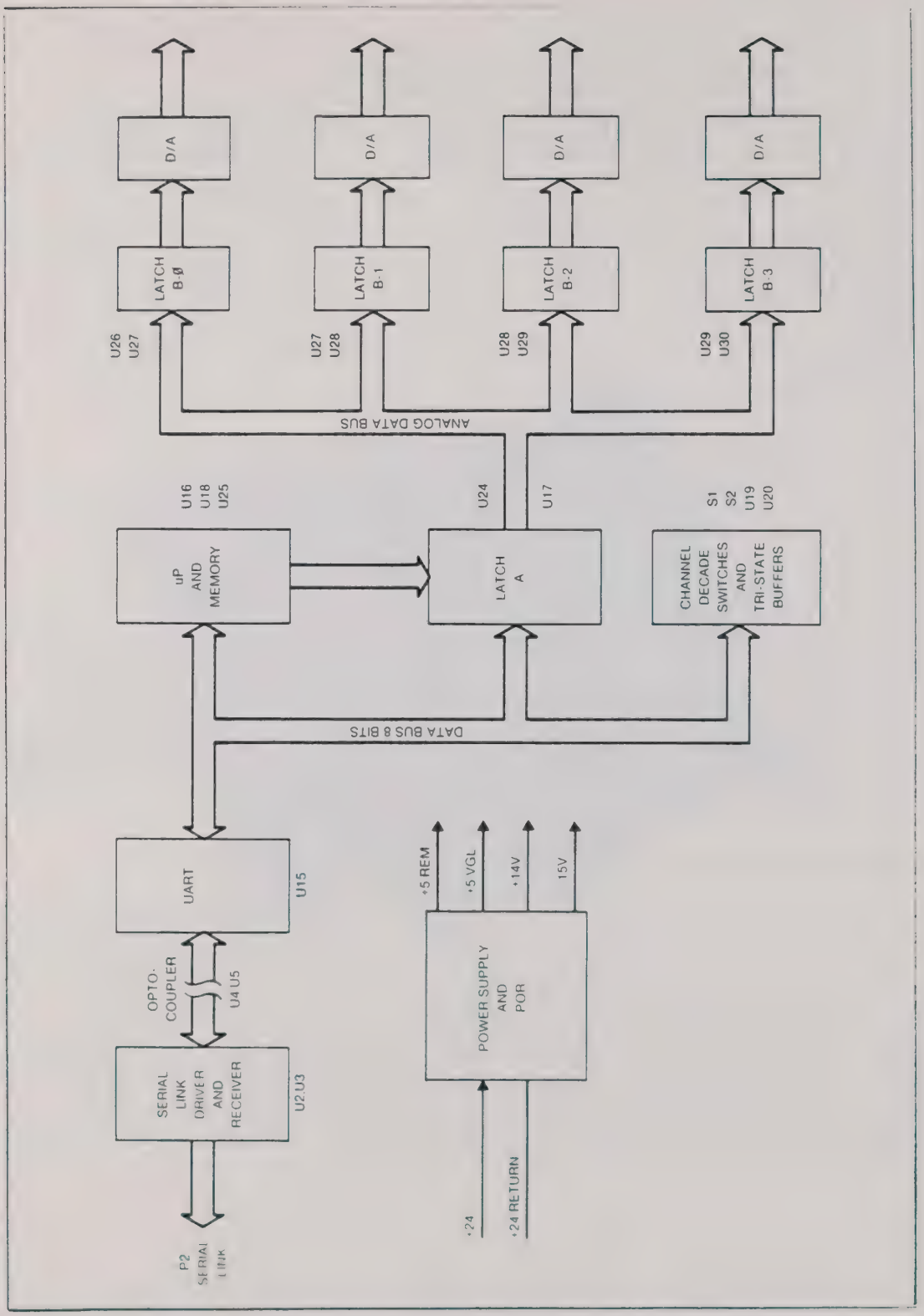


Figure 170-2. Analog Output Option Block Diagram

Digital control circuitry consists of a microprocessor, decade switches with tri-state buffers, and latches to assemble and hold the 12 bit word for the digital to analog converters (DAC). The microprocessor directs the activities of the control circuitry. It oversees the UART communications with the mainframe controller assembly. Addresses received over the serial link are compared with the address selected through the decade switches to determine if the data is intended for this Analog Output assembly. The 12-bit data word for an output is loaded into intermediate latches and then passed to the latch associated with the intended output channel.

The digital to analog section consists of a 0 to +10 volt output, a 5 volt offset, and a voltage to current converter. The 5 volt offset, when used with the 0 to +10 volt output, provides a bi-polar output of -5 to +5 volts. The voltage to current converter uses the 0 to +10 volt output to provide 4 to 20 mA.

Detailed Circuit Description

POWER SUPPLY

The power supply is a fly-back converter. It will accept an input voltage of 10 to 25 volts from the serial link. Voltages supplied by the converter are the 5V REM for remote serial link, 5VGL for the digital circuitry, and +14/-15 volts for the analog circuitry. The 5VGL, +14V, and -15V supplies have post linear regulators to provide additional regulation.

The Inverter Section

A simplified schematic of the power supply is shown in Figure 170-3. Isolation is provided by T1. When the transistor, Q4, is turned on, the rectifying diodes are off allowing the current in the primary of T1 to ramp up. Q4 is then turned off, causing the energy stored in T1 to be released into the secondaries through the diodes. The voltage on C15 is sampled by U10 and its supporting circuitry. If the voltage is above or below the nominal 5.4V, an error signal is generated. This error signal is relayed through the optical coupler to the control circuitry. The control circuitry varies the ratio of the time Q4 is on to the time Q4 is off to control the output voltage. The ratio of the on time to the off time is called the duty cycle. If the voltage sampled on C15 is lower than 5.4V the control circuitry increases the duty cycle. If the sampled voltage is greater than 5.4V the duty cycle is decreased. The voltages on C13, C14, and C15 are further regulated by post linear regulators.

The Control Section

The control section directs the overall activities of the analog output card. It controls the UART in serial link communications, retrieves the card address from the decade switches, and delivers the binary number to the DACs. The major components of the control section are a microprocessor (U16), a ROM (U18) that contains the program for the microprocessor, a crystal (Y1) to drive the microprocessor's clock, and a latch (U25). The address to the ROM consists of eight bits from the latch (U25) and three bits directly from the microprocessor. The latch is gated by the address latch enable (ALE) signal from the microprocessor.

The Power-On Reset Circuit

The power-on reset circuit enables the digital circuitry 50 mS or more after power has been established. It also disables the microprocessor immediately if the 5VGL decreases below operating level.

The power-on reset circuit is shown in Figure 170-4. Stage 1 of the power-on reset circuit is the sensing circuit, used to determine if the output voltage is sufficient for operation. During turn-on, the sensing circuit releases the RC circuit in the second stage when the power supply is within tolerance, allowing the RC to charge slowly. If the voltage across the RC circuit is sufficient, it trips the comparator in stage 2. When the comparator trips, the POR signal goes high. If on the other hand, the voltage dips, the output of the comparator in stage 1 will go low, pulling the voltage across the RC circuit low very quickly. Low voltage across the RC circuit causes the comparator to set the POR reset signal low.

Communication Circuitry

The communication circuitry is shown in Figure 170-5. Information is received from the serial link by U3, the serial link receiver, and transmitted onto the serial link by U2, the serial link driver. When a data word is received by the UART the DR (data ready) is set, interrupting the microprocessor. The microprocessor reads the UART by enabling the RD signal with port 1, bit 1. By checking port 1, bit 0, the microprocessor checks for three different kinds of errors: overrun error, frame error, and parity errors.

To transmit, the serial link driver is enabled by port 1, bit 3. The microprocessor loads a data word to be transmitted over the serial link by enabling the WR (write) signal to the TBRL (transmit buffer register load). The UART then serially transmits the 8 bit word just loaded from the data bus. The serial link driver is then disabled to allow other boards to use the serial link.

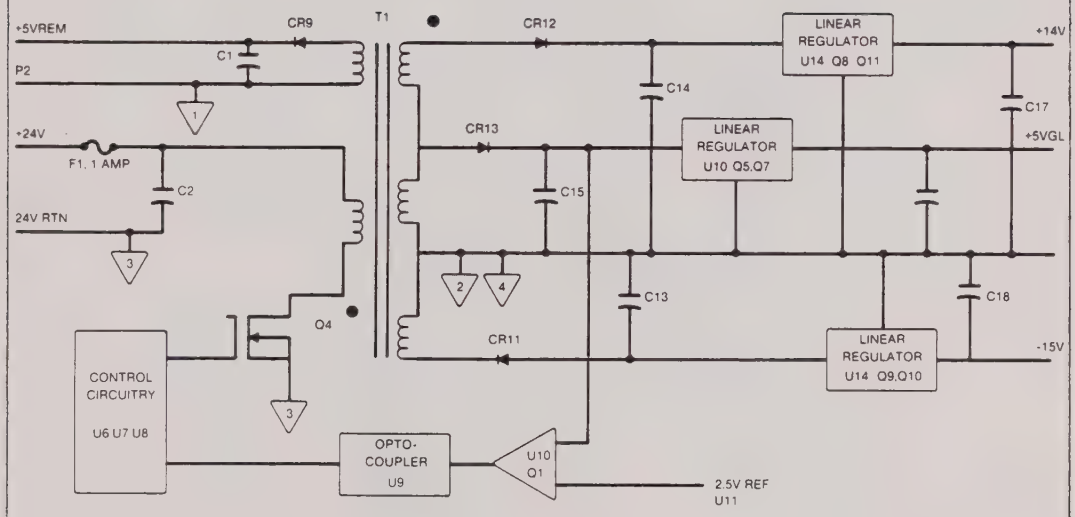


Figure 170-3. Power Supply Simplified Schematic

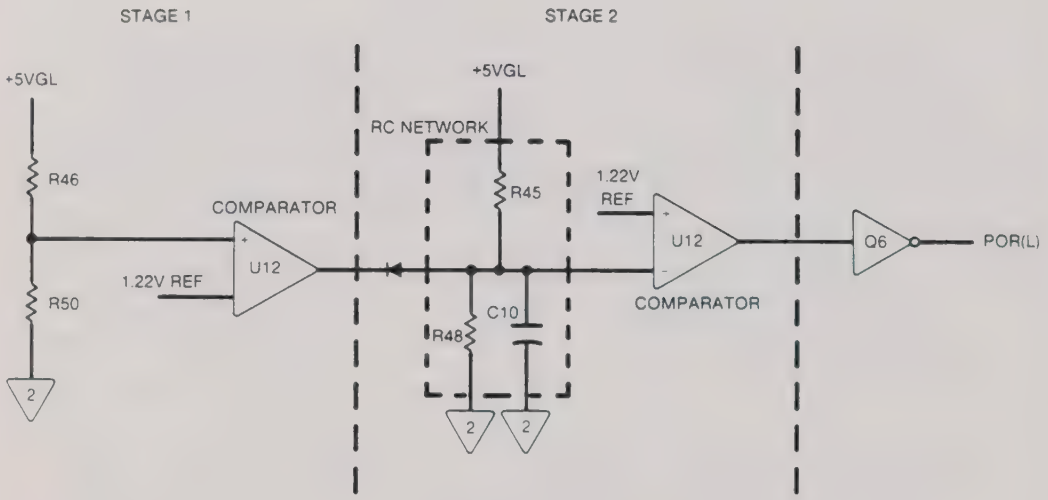


Figure 170-4. Power-On-Reset Simplified Schematic

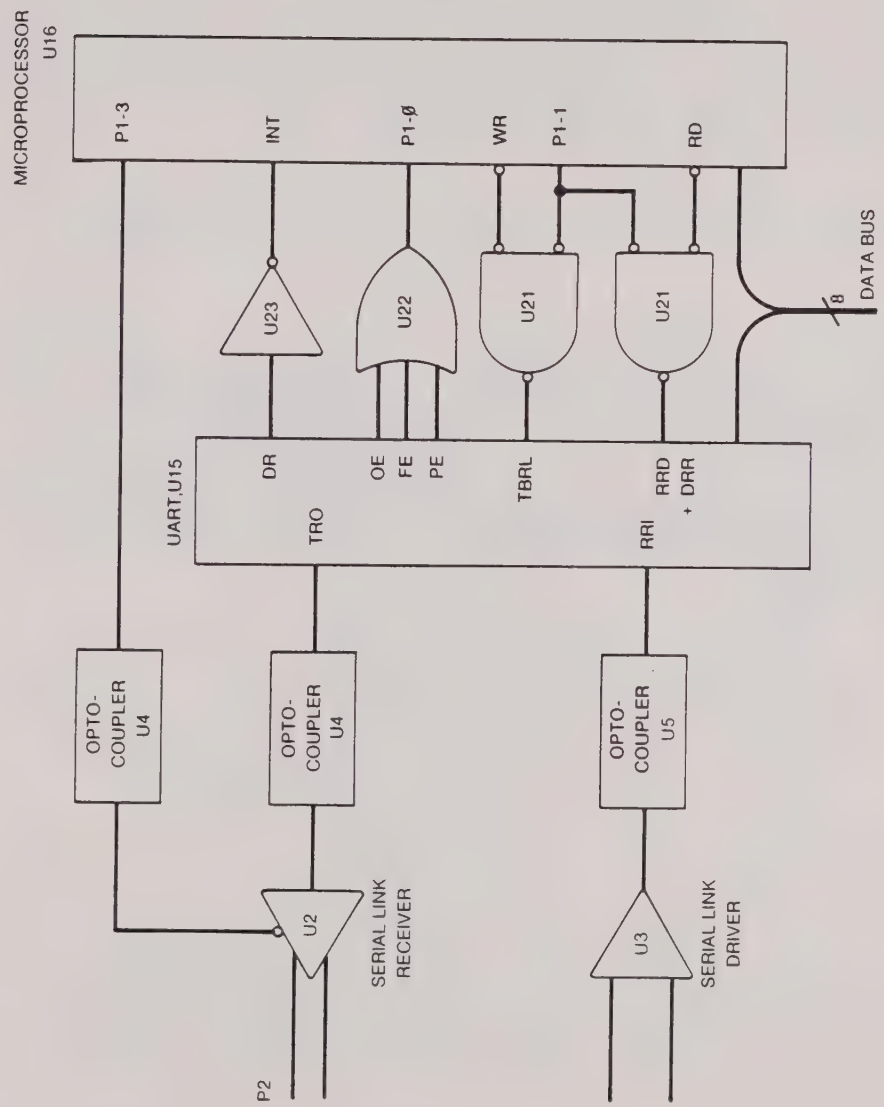


Figure 170-5. Communication Circuitry

The Decade Switches

The analog output address is determined by the position of the decade switches. The decade switches are physically located on the left hand side of the board. The value of the decade switch is enabled onto the data bus by the tri-state buffers U19 and U20. The tri-state buffers are controlled by the RD signal from the microprocessor. The RD signal to the buffers is enabled by setting port 1, bit 5, low. Figure 170-6 is a simplified schematic of the interface between the microprocessor and the decade switch. The address read from the decade switch is compared to the address received over the serial link.

Note that when checking the address lines for the correct signals, a value of 1 (true) is indicated by a low voltage on the corresponding line.

Latch Control

The digital to analog converters (DACs) convert a 12-bit digital word to an analog output. The 12-bit word is built in two steps using latch A, shown in Figure 170-7. First, an 8-bit data word is latched into U17 from the data bus. Then 4 bits are latched into U24 from the lower 4 bits of port 2. This 12-bit word is then presented to the output channel selected by port 2, bits 4 through 7, which clock the 12-bit data word into the appropriate B latch. Table 170-2 lists the port bit that is used for each channel.

Table 170-2. Channel Port Pins (U16)

port 2, bit 7	pin 38	channel 0
port 2, bit 6	pin 37	channel 1
port 2, bit 5	pin 36	channel 2
port 2, bit 4	pin 35	channel 3

The output of all four channels is reset to 0% of full scale when port 2, bit 7, is set high. Port 2, bit 7, is high initially when the Analog Output is powered on. This control line is also used to reset the outputs when an initialize or reset command is received from the mainframe.

THE ANALOG SECTION

The core of the analog section is a voltage reference and DAC with an amplifier. This circuitry is all that is needed for the 0 to 10 volt output. The bipolar output +5V to -5V is achieved with the addition of a 5V offset. The current source converts the 0 to 10 volt output and -10 volt reference to establish the 4 to 20 mA output. The digital to analog circuitry is shown in Figure 170-8.

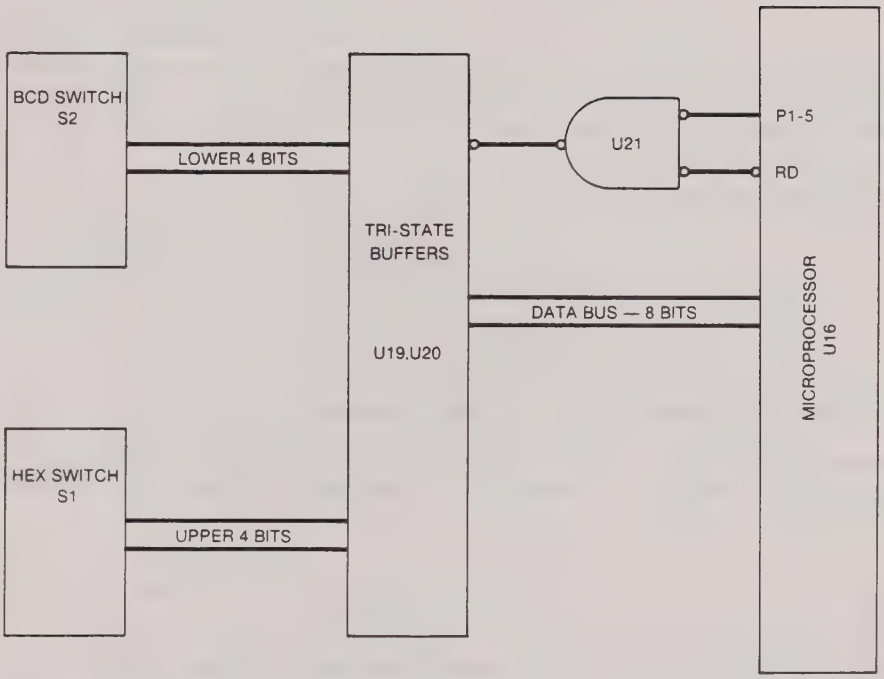


Figure 170-6. Decade Switches To Microprocessor Interface

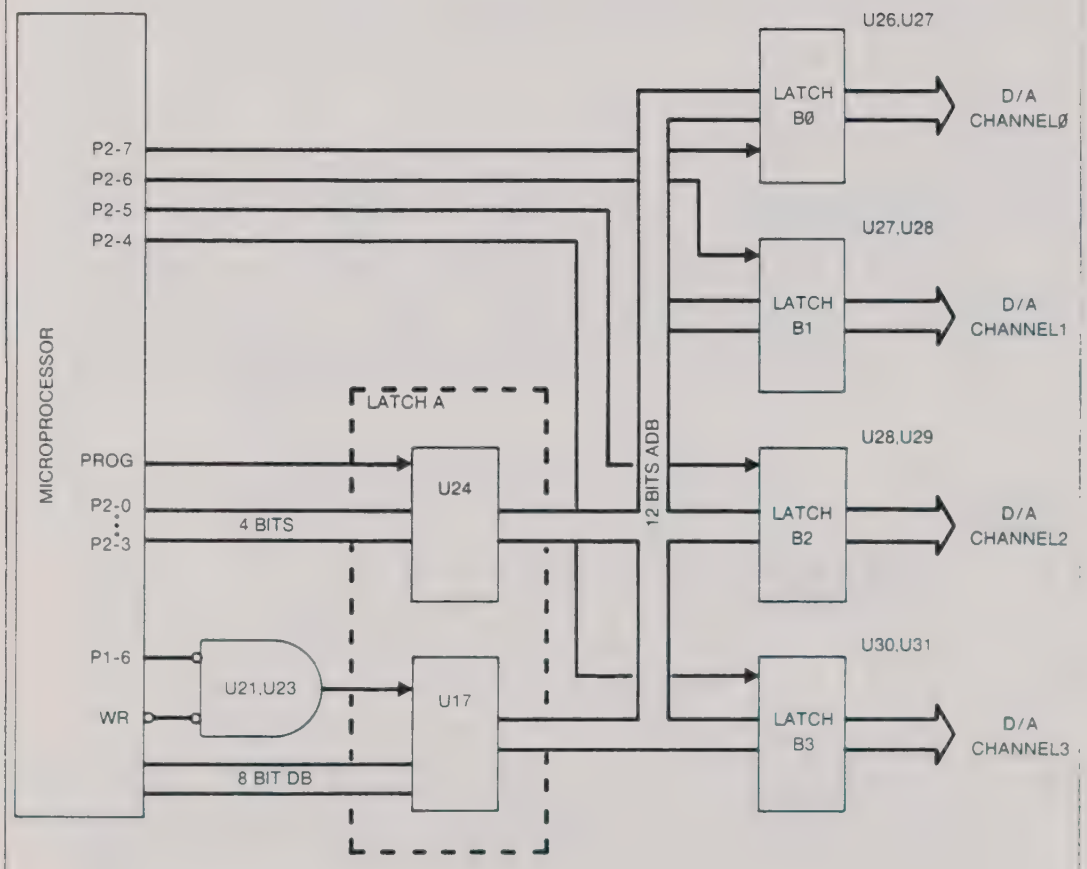
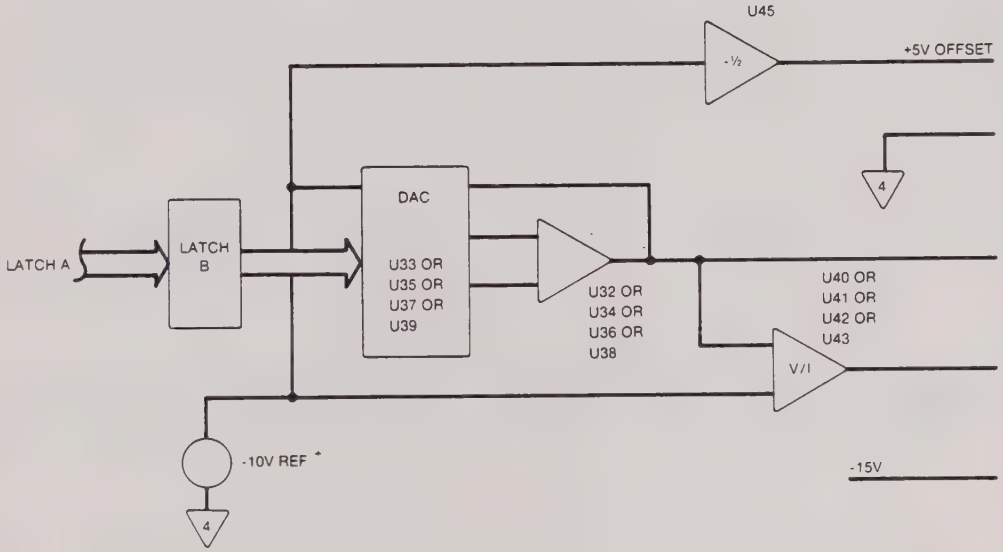


Figure 170-7. Control Circuitry


U45
-½
+5V OFFSET
4
DAC
LATCH A
LATCH B
U33 OR
U35 OR
U37 OR
U39
U32 OR
U34 OR
U36 OR
U38
U40 OR
U41 OR
U42 OR
U43
V/I
-10V REF
4
-15V

The -10V Reference

The -10V reference is the main reference for the analog output. The primary components are VR3 and U44. The zener diode is part of a selected set containing VR3, R98, and R106. The resistors are chosen so the voltage on pin 3 of U44 is between -6.2 and -6.45 volts. This voltage is amplified to -10 volts by U44, which is configured in a non-inverting mode with a nominal gain of 1.61. Potentiometer R99 adjusts the gain (the -10 volt reference).

The 5V offset

The 5 volt offset is used as the return for the voltage source when the bi-polar, -5 to +5 volt, is desired. This offset is common to all four channels.

The primary active components are U45, Q27, and Q26. The -10 volt reference is used to drive an inverting amplifier with a gain of -0.5. Q27 and Q26 provide the additional drive necessary to support all four outputs. The potentiometer R100 adjusts the 5 volt offset.

The DAC and Amplifier

The DAC and its amplifier for each channel are shown in Table 170-3. The potentiometer shown adjusts the voltage output of the channel.

Table 170-3. DAC Amplifier Potentiometers

CHANNEL	DAC	AMPLIFIER	POTENTIOMETER
0	U33	U32	R61
1	U35	U34	R64
2	U37	U36	R67
3	U39	U38	R70

The Current Source

Figure 170-9 shows the current source. Output current flows through the 100 ohm resistor and the drive transistors to the load. The voltage drop across the 100 ohm sense resistor, and hence, the output current, is set by the output voltage of the operational amplifier. The potential at the inverting node of the amplifier is the result of the 0-10 volt output and the voltage drop across the 100 ohm sense resistor. The amplifier output voltage is set so that the voltage at the non-inverting node is equal to the voltage at the inverting node. This node is offset from ground by the offset circuitry to create the drive for the 4 mA offset.

In normal operation, Q14 (Q17, Q20, Q23) is turned off. The voltage drop across the 2 kilohm resistor located between the base of the drive transistors and the output of the amplifier is a few millivolts. When the load resistance is such that the voltage drop across the load exceeds the compliance range (10 V) of the current source, the current flowing from the base of the drive transistors becomes excessive, which causes a voltage drop that approaches one volt. The voltage drop creates enough drive to turn Q14 (Q17, Q20, Q23) on, thus connecting the output of the operational amplifier to the inverting node. The voltage output of the amplifier is forced to the offset voltage on the non-inverting node of the amplifier.

GENERAL MAINTENANCE

The Analog Output Option PCA normally does not require cleaning unless dirt, dust, or other contamination is visible on the surface. Follow PCA cleaning instructions in Section 4 of this manual.

PERFORMANCE TESTS

There are two performance tests for the 2280A-170 Analog Output. The first test is the Address Response test. This test verifies that the mainframe controller assembly can communicate properly with the Analog Output with the address switch set to positions that test all address switch signals. The second test is the accuracy verification test. This ensures that all analog outputs on the assembly are within specifications.

The performance tests verify that the Analog Output performs properly and meets it's specified accuracy tolerances. If it is determined that calibration of the assembly is required, refer to the Calibration section that immediately follows the performance tests in this section.

Address Response Performance Test

WARNING

THE DATA LOGGER CONTAINS HIGH VOLTAGES WHICH CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE EQUIPMENT. TURN OFF THE DATA LOGGER AND REMOVE ALL POWER SOURCES BEFORE PERFORMING THE FOLLOWING PROCEDURE.&

1. Turn the 2280 keyswitch to the POWER OFF position. Disconnect the line power or battery input power and all other high voltage inputs.

2. Remove all A/D Converters (2280A-161), Digital I/O (2280A-168), Analog Outputs (2280B-170), Counter/Totalizers (2280B-167) options from the Data Logger.

3. Install the Analog Output to be tested in the uppermost option slot of the Data Logger.

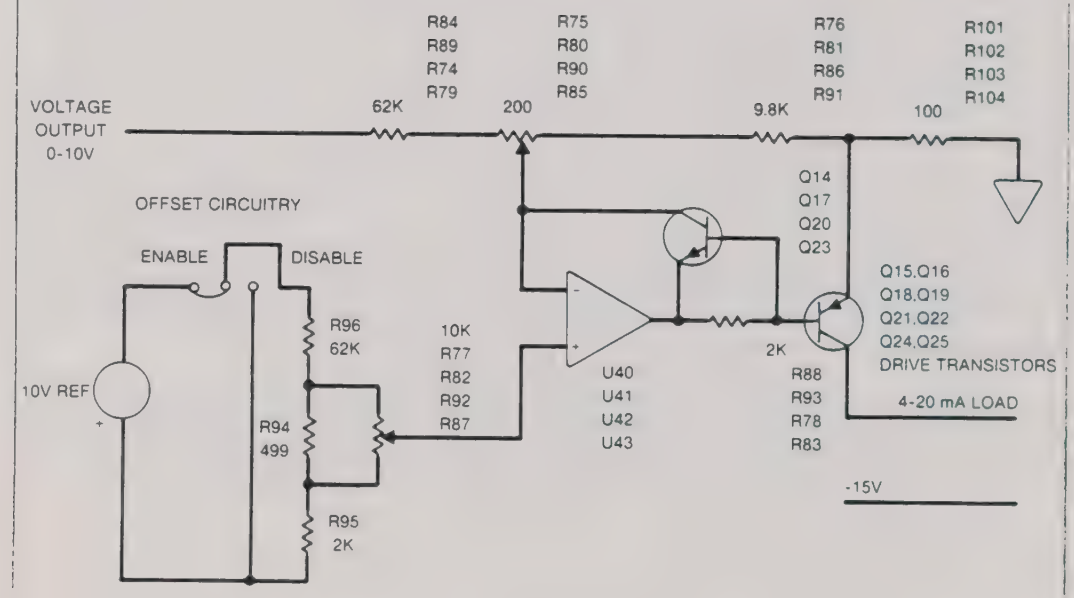


Figure 170-9. The Current Source

4. Reconnect line or battery power to the Data Logger

5. Set the Channel Decade switches on the rear panel of the Analog Output to 00.

6. Turn the keyswitch to PROGRAM.

7. Verify the ability of the mainframe controller to communicate with the Analog Output by executing the System Diagnostic test as shown in Table 170-4.

Table 170-4. Address Response Test Programming Steps

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	S	<S> SYSTEM DIAGNOSTICS
3	ENTER	S: DEVICE TO TEST <1-7>? 1
4	7	S<7> SERIAL LINK
5	ENTER	CHANNEL NUMBER = C0
6	00	CHANNEL NUMBER = 00
7	ENTER	TEST IN PROGRESS

8. Following the execution of step 7 in Table 170-4, the 2280 should have either TEST PASSED or TEST FAILED displayed. If TEST FAILED is displayed, the Analog Output cannot properly communicate with the mainframe controller with the current channel decade selected.

9. Depress the EXIT key twice. The display will read MAIN MENU CHOICE <M FOR MENU>? A

10. Repeat steps 5 through 9 with channel decade switch selections of 01, 02, 04, 08, 10, 20, 40, and 80. At step 6 of Table 170-4 a number ten times the switch selection should be entered. For example, when 40 is selected in the switches, 400 should be entered at step 6.

11. The address response test is complete. Continue with the accuracy verification test if you are performing a complete verification test of the Analog Output (option 2280A-170).

WARNING

THE DATA LOGGER CONTAINS HIGH VOLTAGES WHICH CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE EQUIPMENT. TURN OFF THE DATA LOGGER AND REMOVE ALL POWER SOURCES BEFORE PERFORMING THE FOLLOWING PROCEDURE.

1. Turn the 2280 keyswitch to the POWER OFF position. Disconnect the line power or battery input power and all other high voltage inputs.

2. Install the Analog Output to be tested in the uppermost option slot of the Data Logger. Set the Channel Decade switches to 00 on the back of the Analog Output.

3. Reconnect line or battery power to the Data Logger.

4. Allow for a one-half hour warmup

5. Turn the keyswitch to PROGRAM.

CAUTION

The exposed screws visible on the top of the Analog Output connector block can be probed only if it is screwed down tightly, otherwise, it does not make contact with the output from the assembly.

6. Using the multimeter, verify that the outputs of the Analog Output are within tolerance of their zero percent output values as given in Table 170-5.

Table 170-5 Output Values and Tolerances With Zero Percent Outputs

OUTPUT SIGNAL	OUTPUT VALUE	TOLERANCE	TERMINAL PAIR FOR EACH CHANNEL							
			0+	0-	1+	1-	2+	2-	3+	3-
0 to 10V	0.000V	+/- 0.010V	1	2	6	7	11	12	16	17
-5 to +5V	-4.997V	+/- 0.010V	1	3	6	8	11	13	16	18
4 to 20mA	4.000mA	+/- 0.020mA	4	5	9	10	14	15	19	20

7. Program the Data Logger to output full scale outputs to the Analog Output by performing the programming sequence in Table 170-6.

Table 170-6. Accuracy Verification Test Program

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
7	C0..3	CHANNEL NUMBER (OR BLOCK) = C0..3
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
10	O	A<O> ANALOG OUTPUT
11	ENTER	AO: CHANNEL MENU CHOICE <1-5>? 1
12	3	AO<3> CHANNEL PROCEDURE
13	ENTER	CP:
14	CX=1.0	CP: CX=1.0
15	ENTER	CP:
16	ENTER	AO: CHANNEL MENU CHOICE <1-5>? 4
17	EXIT	A: CHANNEL FUNCTION <A-Z>? O
18	EXIT	CHANNEL NUMBER (OR BLOCK) = C0..3
19	EXIT	MAIN MENU CHOICE <M FOR MENU>? A
20	K	<K> PROGRAM A SCAN GROUP
21	ENTER	SCAN GROUP NUMBER = 0
22	ENTER	PROGRAM COPY DELETE OR LIST<P,C,D,L>? P
23	ENTER	K: SCAN GROUP MENU CHOICE <1-5>? 1
24	2	K<2> SCAN GROUP CHANNEL LIST
25	ENTER	CL:
26	C0..3	CL: C0..3
27	ENTER	CL:
28	ENTER	K: SCAN GROUP MENU CHOICE <1-5>? 3
29	EXIT	SCAN GROUP NUMBER = 0
30	EXIT	MAIN MENU CHOICE <M FOR MENU>? A
31	SINGLE SCAN	SCAN GROUP NUMBER = 0
32	ENTER	MAIN MENU CHOICE <M FOR MENU>? A

8. Using the multimeter, verify that the outputs of the Analog Output are within tolerance of their full scale output values as given in Table 170-7.

CAUTION

The exposed screws visible on the top of the Analog Output connector block can be probed only if it is screwed down tightly, otherwise, it does not make contact with the output from the assembly.

Table 170-7. Output Values and Tolerances with Full Scale Outputs

OUTPUT SIGNAL	OUTPUT VALUE	TOLERANCE	TERMINAL PAIR FOR EACH CHANNEL							
			0+	0-	1+	1-	2+	2-	3+	3-
0 to 10V	9.997V	+/- 0.010V	1	2	6	7	11	12	16	17
-5 to +5V	4.997V	+/- 0.010V	1	3	6	8	11	13	16	18
4 to 20mA	20.00mA	+/- 0.020mA	4	5	9	10	14	15	19	20

9. The Analog Output assembly performance test is complete.

CALIBRATION

The calibration sequence for the 2280B-170 Analog Output is provided in this section. The results of the accuracy verification test in the performance test section will indicate whether calibration of the Analog Output is required. Perform the calibration only if it is required.

WARNING

THE DATA LOGGER CONTAINS HIGH VOLTAGES WHICH CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE EQUIPMENT. TURN OFF THE DATA LOGGER AND REMOVE ALL POWER SOURCES BEFORE PERFORMING ANY OF THE PROCEDURES IN THIS SECTION.

Analog Output Calibration Procedure

The following step by step procedure is used to calibrate the 2280A-170. The steps must be performed in order.

1. Turn the 2280 front panel keyswitch to the POWER OFF position.

2. Disconnect the Data Logger Power input and all other high voltage inputs.

3. Remove all A/D Converters (2280A-161), Digital I/O (2280A-168), Analog Outputs (2280B-170), Counter/Totalizers (2280B-167) options from the Data Logger.

4. Remove the Analog Output to be calibrated from the 2280 or 2281 chassis and install the Calibration/Extender fixture (Fluke Accessory Y2056) in place of the Analog Output. Install the Analog Output assembly on the Calibration/Extender fixture.

5. Set the channel decade switch on the rear panel of the Analog Output to 00.

6. Reconnect the Data Logger ac line or battery power input.

7. Turn the keyswitch to the PROGRAM position.

8. Set the digital multimeter to read +10V with 0.0001V resolution.

9. Connect the positive test lead of the multimeter to terminal 2 on the Analog Output connector and the negative lead to terminal 21.

10. Calibrate the -10 volt reference. Adjust R99 such that the voltage measured between connector terminals 2 and 21 is 10.000V within a tolerance of +/- 0.0005V.

11. Connect the positive test lead of the multimeter to terminal 2 on the connector and the negative lead to terminal 3.

12. Calibrate the 5 volt reference. Adjust R100 such that the voltage measured between connector terminals 2 and 3 is 5.000V within a tolerance of +/- 0.0005V.

10. Program the Data Logger to set the outputs on channels 0, 1, 2, and 3 to their full scale values by performing the programming sequence in Table 170-6. This is the same program sequence used in the performance test.

11. Calibrate the full scale outputs for channels 0, 1, 2, and 3. For each channel, adjust the appropriate pot such that the voltage measured is 9.9976V within a tolerance of +/- 0.0005V. Refer to Table 170-8 for terminal and adjustment pot identification. The voltage outputs are now calibrated. If the 4 to 20mA current outputs are not going to be used, you may skip the current output calibration and proceed with step 18.

Table 170-8. Full Scale Voltage Calibration Adjustments

CHANNEL	POSITIVE TERMINAL	NEGATIVE TERMINAL	ADJUSTMENT POT
0	1	2	R61
1	6	7	R64
2	11	12	R67
3	16	17	R70

12. Power down the 2280 and install the jumper on the Analog Output at W1 such that pins 3 and 4 are connected. This disables the 4mA offset.

13. Power up the 2280 and depress the SINGLE SCAN and then the ENTER key. This will put the outputs at their full scale output levels.

14. Calibrate the current outputs for channels 0, 1, 2, and 3. For each channel, adjust the appropriate pot such that the current measured current is 15.996mA within a tolerance of +/- 0.001mA. Refer to Table 170-9 for terminal and adjustment pot identification.

Table 170-9. Full Scale Current Calibration Adjustments (Without Offset)

CHANNEL	POSITIVE TERMINAL	NEGATIVE TERMINAL	ADJUSTMENT POT
0	4	5	R75
1	9	10	R80
2	14	15	R85
3	19	20	R90

15. Power down the 2280 and return jumper W1 such that pins 1 and 2 are connected. This enables the 4mA offset.

16. Power up the 2280 and depress the SINGLE SCAN and then the ENTER key. This will put the outputs at their full scale output levels.

17. Calibrate the current outputs for channels 0, 1, 2, and 3. For each channel, adjust the appropriate pot such that the current measured current is 19.996mA within a tolerance of +/- 0.001mA. Refer to Table 170-10 for terminal and adjustment pot identification.

Table 170-10. Full Scale Current Calibration Adjustments (With Offset)

CHANNEL	POSITIVE TERMINAL	NEGATIVE TERMINAL	ADJUSTMENT POT
0	4	5	R77
1	9	10	R82
2	14	15	R87
3	19	20	R92

18. The calibration of the Analog Output is now complete. Power down the 2280. Remove the Analog Output from the Calibration/Extender Fixture. Remove the Calibration/Extender Fixture from the 2280. Install the Analog Output in the 2280 or 2281 and set the channel decade switch for use within your 2280 system. Install the other hardware that may have been removed to calibrate the Analog Output.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the Analog Output Option is given in Table 170-11. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the Analog Output Option is given in Figure 170-10.

TABLE 170-11. 2280B-170 ANALOG OUTPUT PCA
(SEE FIGURE 170-10.)

REFERENCE DESIGNATOR A->NUMERICS---)	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOT -E
C 1, 13- 15		CAP,AL,270UF,+100-10%,20V	602656	89536	602656	4		
C 2		CAP,AL,330UF,+100-10%,25V	614404	89536	614404	1		
C 3		CAP,CER,5600PF,+-5%,50V,COG	528596	89536	528596	1		
C 4		CAP,CER,1000PF,+-5%,50V,COG	528539	51406	RPE113	1		
C 5		CAP,TA,1UF,+-10%,35V	161919	56289	196D010X0035G	1		
C 6		CAP,AL,22UF,+-20%,35V	655084	74840	RLR-PX	1		
C 8		CAP,CER,1.0UF,+-20%,50V,Z5U	436782	72982	8131-050-601-105M	1		
C 9, 19, 23,		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	9		
C 25- 30			519157					
C 10		CAP,POLYES,0.47UF,+-10%,100V	369124	89536	369124	1		
C 11		CAP,CER,1000PF,+-10%,500V,X5S	357806	56289	C016B102G102K	1		
C 12		CAP,CER,0.0012UF,+-10%,500V,Z5R	106732	71590	CF122	1		
C 16- 18		CAP,AL,47UF,+-20%,16V	643304	89536	643304	3		
C 20		CAP,CER,18PF,+-2%,100V,COG	512335	51406	RD870-100V	1		
C 21		CAP,CER,4.7PF,+-0.25PF,100V,COH	362772	89536	362772	1		
C 22, 24, 59,		CAP,TA,15UF,+-20%,20V	519686	56289	196D156X0020KE4	6		
C 60, 66, 67			519686					
C 31, 38, 45,		CAP,CER,2200PF,+-20%,100V,X7R	358291	89536	358291	4		
C 52			358291					
C 32, 39, 46,		CAP,CER,1200PF,+-20%,100V,X7R	358283	72982	8121-A100-W5R-122M	4		
C 53			358283					
C 33- 36, 40-		CAP,TA,2.2UF,+-20%,20V	161927	56289	196D225X0020HA1	17		
C 43			161927					
C 47- 50, 54-			161927					
C 57, 65			161927					
C 37, 44, 51,		CAP,CER,0.01UF,+-20%,100V,X7R	407361	72982	8121-A100-W5R-103M	4		
C 58			407361					
C 61		CAP,CER,22PF,+-2%,100V,COG	512871	89536	512871	1		
C 62- 64		CAP,CER,120PF,+-2%,100V,COG	543819	04222	SR15	3		
CR 1- 8, 11,	*	DIODE,SI, 50 PIV, 1.0 AMP	379412	04713	1N4933	10	1	
CR 12	*		379412					
CR 9, 13	*	DIODE,SI, 20 PIV, 1.0 AMP	507731	83003	VSK120	2	1	
CR 10, 16- 19	*	DIODE,SI, 100 PIV, 1.0 AMP	343491	01295	1N4002	5	2	
CR 14, 15	*	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	2		
E 1		JUMPER, RECEPTACLE	530253	00079	530153-2	1		
F 1		FUSE,1/4 X 1-1/4,FAST,1.0A,250V	369819	71400	AGC1	1		
H 1		NYLON, STEM:OD=.093", L=.115"	658450	89536	658450	8		
H 2		WASHER	110270	89536	110270	5		
H 2		SCREW,MACH,FHP,STL,6-32X3/8	114363	73734	182444	3		
H 3		SCREW	114223	89536	114223	2		
H 4		WASHER	110692	89536	110692	2		
J 1		POLARIZING INSERT,EDGE CONN. ACCESS.	543710	89536	543710	1		
MP 1		COVER,ANALOG/OUTPUT	729673	89536	729673	1		
MP 2		SPACER,SWAGED,RND,BRASS,6-32X0.250	446351	89536	446351	3		
MP 3		CABLE TIE,4"L,0.100"W,0.75 DIA	172080	89536	172080	1		
MP 4		FUSE HLDR,CLIP,PCB,1/4 DIA FUSE	485219	91833	3529	2		
MP 5		BAG,SHIELDING,TRANSPARENT,12"X16"	680983	89536	680983	1	5	
Q 1, 3, 10,	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	195974	64713	2N3906	6	1	
Q 12, 13, 26	*		195974					
Q 4	*	TRANSISTOR,SI,N-MOS,POWER,TO-220AB	586107	89536	586107	1	1	
Q 5, 6, 11,	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	4	2	
Q 27	*		218396					
Q 7, 8, 16,	*	TRANSISTOR,SI,BV= 80V,100W,TO-202	495689	04713	MPSU56	6	1	
Q 19, 22, 25	*		495689					
Q 9	*	TRANSISTOR,SI,BV= 80V, 10W,TO-202	495697	04713	MPS-U06	1	2	
Q 14, 17, 20,	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218081	04714	MPS6520	4	1	
Q 23	*		218081					
Q 15, 18, 21,	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	225599	07263	2N4250	4	1	
Q 24	*		225599					
R 1, 2, 10,		RES,CF,51,+-5%,0.25W	414540	80031	CR251-4-5P51E	8		
R 11, 59, 62,			414540					
R 66, 69			414540					
R 3, 13, 16,		RES,CF,5.6K,+-5%,0.25W	442350	80031	CR251-4-5P5K6	4		
R 20			442350					
R 5, 19		RES,CF,30,+-5%,0.25W	442228	80031	CR251-4-5P30E	2		
R 7, 12, 14,		RES,CF,270,+-5%,0.25W	348789	80031	CR251-4-5P270E	5		
R 15, 22			348789					
R 8, 9, 17,		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	10		
R 18, 21, 23,			348839					
R 25, 31, 44,			348839					
R 51			348839					
R 24		RES,CF,510,+-5%,0.25W	441600	80031	CR251-4-5P510E	1		
R 26, 36, 41		RES,CF,100,+-5%,0.25W	348771	80031	CR251-4-5P100E	3		
R 27		RES,CF,330,+-5%,0.25W	368720	80031	CR251-4-5P330E	1		

TABLE 170-11. 2280B-170 ANALOG OUTPUT PCA
(SEE FIGURE 170-10.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOT -E
R 28		RES,MF,9.53K,+-1%,0.125W,100PPM	288563	91637	CMF559530F	1		
R 29, 30, 32,		RES,MF,10K,+-1%,0.125W,100PPM	168260	91637	CMF551002F	6		
R 40, 42, 50			168260					
R 33		RES,MF,39.2K,+-1%,0.125W,100PPM	236414	91637	CMF553922F	1		
R 34		RES,MF,14.3K,+-1%,0.125W,100PPM	291617	91637	CMF551432F	1		
R 37		RES,CF,100K,+-5%,0.25W	348920	80031	CR251-4-5P100K	1		
R 38		RES,MF,46.4K,+-1%,0.125W,100PPM	188375	89536	188375	1		
R 39		RES,MF,40.2K,+-1%,0.125W,100PPM	235333	91637	CMF554022F	1		
R 43		RES,CF,8.2K,+-5%,0.25W	441675	80031	CR251-4-5P8K2	1		
R 45		RES,MF,332K,+-1%,0.125W,100PPM	289504	91637	CMF553323F	1		
R 46		RES,MF,28.7K,+-1%,0.125W,100PPM	235176	91637	CMF552872F	1		
R 47		RES,MF,1K,+-1%,0.125W,100PPM	168229	91637	CMF551001F	1		
R 48		RES,MF,154K,+-1%,0.125W,100PPM	289447	91637	CMF551543F	1		
R 49, 52		RES,CF,1M,+-5%,0.25W	348987	80031	CR251-4-5P1M	2		
R 53, 56		RES,MF,2.49K,+-1%,0.125W,100PPM	226209	91637	CMF552491F	2		
R 54, 57		RES,CF,680,+-5%,0.25W	368779	80031	CR251-4-5P200E	2		
R 55		RES,MF,11.5K,+-1%,0.125W,100PPM	267138	91637	CMF551152F	1		
R 58		RES,MF,15K,+-1%,0.125W,100PPM	285296	91637	CMF551502F	1		
R 60, 63, 65,		RES,MF,80.6,+-1%,0.125W,100PPM	306969	89536	306969	4		
R 68			306969					
R 61, 64, 67,		RES,VAR,CERM,200,+-10%,0.5W	721464	89536	721464	9		
R 70, 75, 80,			721464					
R 85, 90,100			721464					
R 71		RES,6.983K(+-.05%0+-3PPM TC 1/4W BOBB	292896	89536	292896	1		
R 72		RES,WW,40K,+-0.1%,0.125W	271403	89536	271403	1	1	
R 73,112		RES,CF,22K,+-5%,0.25W	348870	80031	CR251-4-5P22K	2		
R 74, 79, 84,		RES,62K(+-.05% 0+-3PPM TC 1/4W BOBB	292904	89536	292904	5	1	
R 89, 96			292904					
R 76, 81, 86,		RES,WW,9.8K,+-0.1%,0.15W	446484	89536	446484	4	1	
R 91			446484					
R 77, 82, 87,		RES,VAR,CERM,10K,+-10%,0.5W	485458	32997	3299W-CR2-103	4		
R 92			485458					
R 78, 83, 88,		RES,CF,2K,+-5%,0.25W	441469	80031	CR251-4-5P2K	4		
R 93			441469					
R 94		RES,MF,499,+-1%,,0.125W,100PPM	168211	91637	CMF554990F	1		
R 95		RES, 2.0K(+-.1% 0+-10PPM TC1/4W BOBB	243048	89536	243048	1	1	
R 97		RES,MF,61.9K,+-1%,0.125W,25PPM	484923	91637	CMF5561192F	1		
R 98,106	*	ZENER REFERENCE SET	377283	89536	377283	1		
R 3	*		377283					
R 99		RES,VAR,CERM,500,+-10%,0.5W	520783	32997	3299W-CR2-501	1		
R 101-104		100(	112151	89536	112151	4	1	
R 105		RES,WW,11.35K,+-0.1%,0.15W	385542	89536	385542	1	1	
R 107		RES,WW,20K,+-0.1%,0.125W	271395	89536	271395	1	1	
R 108		RES,CF,4.7K,+-5%,0.25W	348821	01121	CB4725	1		
R 109		RES,CF,180,+-5%,0.25W	441436	80031	CR251-4-5P180E	1		
R 110,111		RES,CF,390,+-5%,0.25W	441543	80031	CR251-4-5P390E	2		
S 1		SWITCH,ROTARY,1 POLE,10 POS,1 THUMB	602888	97527	1A-21-60-02-G-F	1	1	
S 2		SWITCH,ROTARY,1 POLE,16 POS,1 THUMB	615096	97527	1A-21-60-33-G-F	1		
T 1		INVERTER,TRANSFORMER	716209	89536	716209	1		
TB 1		CONNECTOR PWB EDGE TERMINAL BLOCK	739995	89536	739995	1		
U 2	*	IC,BPLR,DUAL DIFF LINE DRVR W/3-STATE	586081	12040	DS1692J	1	1	
U 3	*	IC,BPLR,DIFFERENTIAL LINE RECEIVER	586073	01295	SN55182J	1	1	
U 4	*	ISOLATOR,OPTO,HI-SPEED,DUAL	429894	28480	5082-4355	1	1	
U 5, 9	*	ISOLATOR,OPTO,HI-SPEED,8 PIN DIP	354746	89536	354746	2	1	
U 6	*	IC,REGULATING PULSE WIDTH MODULATOR	454678	01295	SG3524N	1	1	
U 7	*	IC,CMOS,HEX INVERTER	381848	02735	CD4049AE	1	1	
U 8	*	IC,VOLT REG,FIXED,+15 VOLTS,0.1 AMPS	453035	04713	MC78L15ACG	1	1	
U 10, 14	*	IC,OP AMP,DUAL,INDUSTRIAL TEMP RANGE	605550	01295	LM258JG	2	1	
U 11	*	IC, 2.5 V,40 PPM T.C.,BANDGAP REF	472845	04713	MC1403V	1	1	
U 12	*	IC,COMPARATOR,DUAL,LO-PWR,8 PIN DIP	478354	12040	LM393N	1	1	
U 13	*	IC, 1.22V,100 PPM T.C.,BANDGAP REF	452771	89536	452771	1	1	
U 15	*	IC,CMOS,UNIV ASYNC RECEIVR/TRANSMITER	453464	32293	1M6402CPL	1	1	
U 16	*	IC,NMOS,8 BIT MICROCOMPUTER	685529	89536	685529	1		
U 17, 26- 31	*	IC,CMOS,DUAL 4BIT LTCH W/STROBE&RESET	605261	04713	MC14508BCP	7	1	
U 18		IC,2K X 8 EPROM (PROGRAMMED)	747956	89536	747956	1		
U 19, 20	*	IC,CMOS,HEX BUFFER W/3-STATE OUTPUT	407759	12040	MM80C97N	2	1	
U 21	*	IC,LSTTL,QUAD 2 INPUT OR GATE	605618	01295	SN54LS32J	1	1	
U 22	*	IC,CMOS,TRIPLE 3 INPUT OR GATE	408575	02735	CD4075BE	1	1	
U 23	*	IC,LSTTL,HEX INVERTER	393058	01295	SN74LS04N	1		
U 24	*	IC,CMOS,QUAD D LATCH,W/XOR ENABLE	355149	02739	CD4042AE	1	1	
U 25	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,W/CLEAR	454892	01295	SN74LS273N	1	2	
U 32, 34, 36,	*	IC,OP AMP,LO-OFFSET VOLTAGE,LO-NOISE	605980	06665	OP-07DP	9	1	
U 38, 40- 44	*		605980					
U 33, 35, 37,	*	CMOS,12 BIT MULTIPLYING DAC	722264	89536	722264	4	1	

TABLE 170-11. 2280B-170 ANALOG OUTPUT PCA
(SEE FIGURE 170-10.)

REFERENCE DESIGNATOR A->NUMERICS---)	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
U 39	*		722264					
U 45	*	IC,OP AMP,GENERAL PURPOSE,TO-78 CASE	418368	89536	418368	1	2	
VR 1	*	ZENER,UNCOMP,6V TRANSIENT SUPPRESSOR	508655	24444	1N5908	1	1	
VR 2	*	ZENER,UNCOMP, 20.0V, 5%, 12.5MA, 1.0W	291575	12969	UZ8720	1	1	
W 1		CONN,PWB,HEADER,SIP,0.100,4 PIN	417329	89536	417329	1		
XU 15, 16		SOCKET,DIP,0.100 CTR,40 PIN	429282	09922	DILB40P-108	2		
XU 18		SOCKET,DIP,0.100 CTR,24 PIN	376236	91506	324-AG39D	1		
Y 1	*	CRYSTAL,6MHZ,+-0.01%,HC-18/U	461665	89536	461665	1	1	
Z 1, 2		RES,NET,DIP,16 PIN,15 RES,10K,+-5%	355305	89536	355305	2	1	
Z 3		RES,NET,SIP,10 PIN,9 RES,10K,+-2%	414003	80031	95081002CL	1		
02B 4		CONN,TAB,FASTON,PRESS-IN,0.110 WIDE	512889	02660	62395	3		

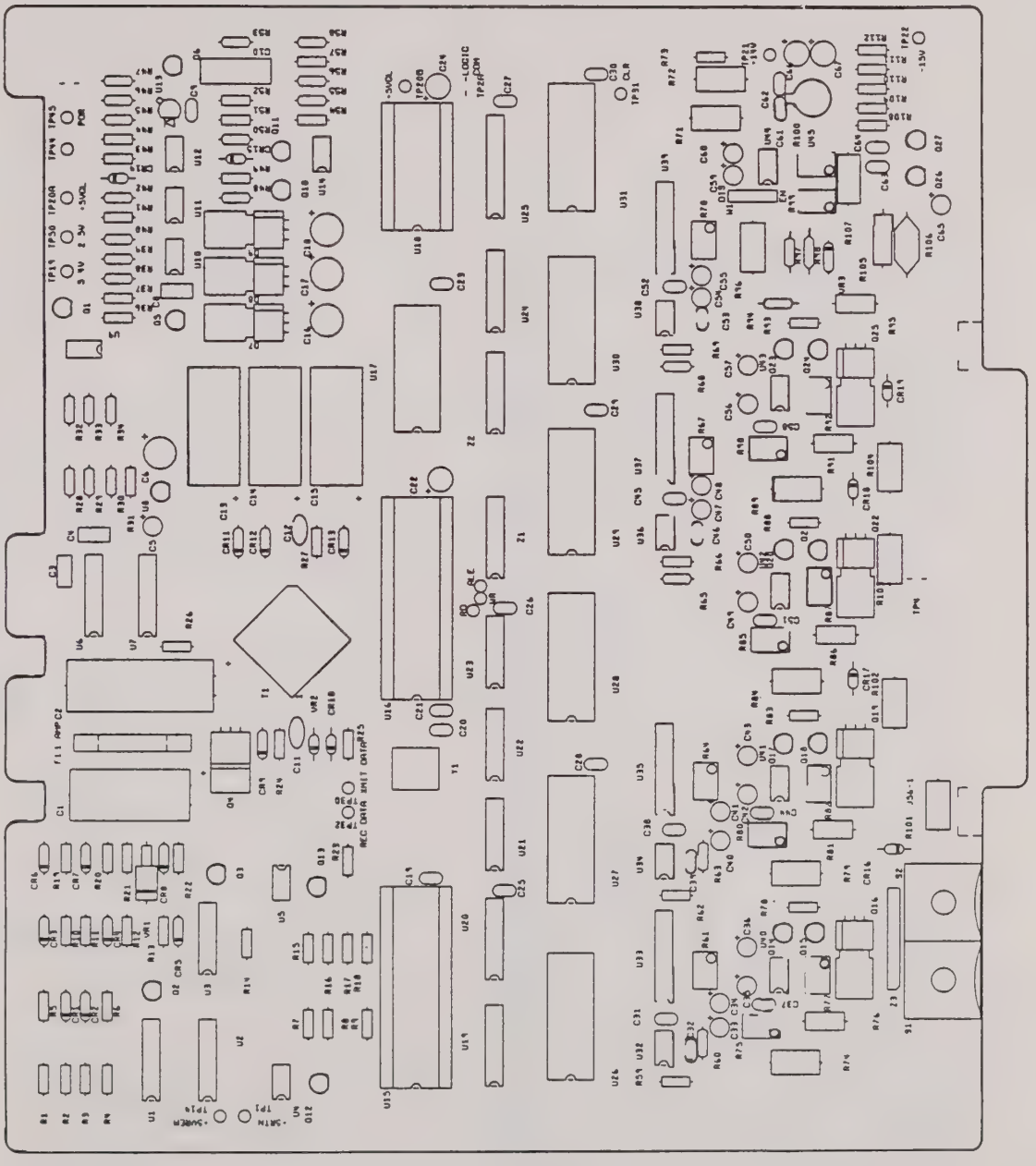


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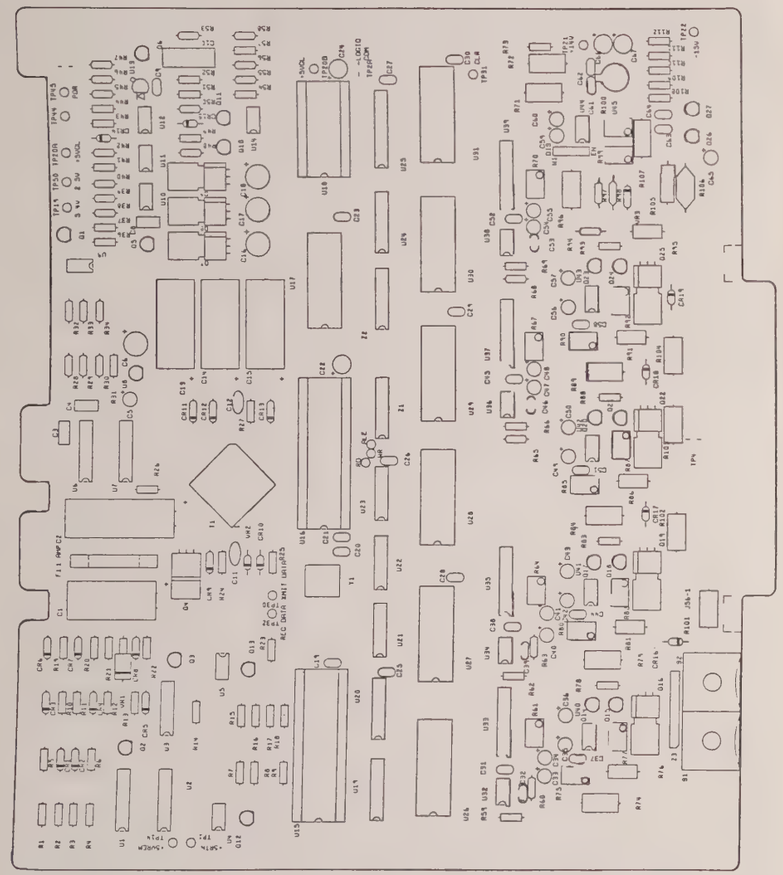
Figure 170-10. 2280B-170 Analog Output PCA



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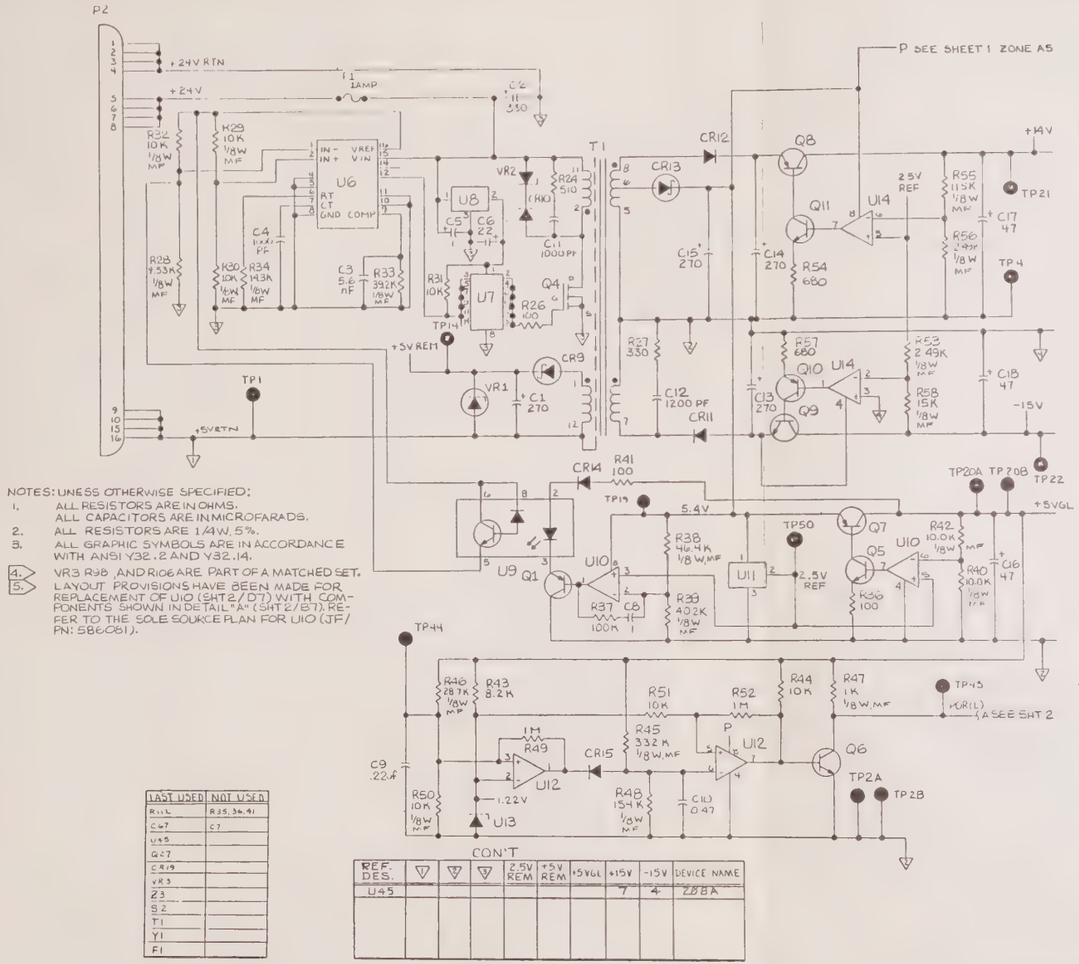

NOTES: UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTORS ARE IN OHMS. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE 1/4W, 5%.
3. ALL GRAPHIC SYMBOLS ARE IN ACCORDANCE WITH ANSI Y32.2 AND Y32.14.
4. VR3 R98 AND R106 ARE PART OF A MATCHED SET.
5. LAYOUT PROVISIONS HAVE BEEN MADE FOR REPLACEMENT OF U10 (SHT 2/D7) WITH COMPONENTS SHOWN IN DETAIL "A" (SHT 2/E5). REFER TO THE SOLE SOURCE PLAN FOR U10 (JF/PN: 586081).

LAST USED	NOT USED
R115	R35, 36, 41
C47	C7
U45	
Q27	
CR19	
VR3	
Z3	
S2	
T1	
Y1	
F1	

REF. DES.	▽	▽	▽	2.5V REM	+5V REM	+5VGL	+15V	-15V	DEVICE NAME
U45							7	4	Z88A

REF DES	▽	▽	▽	2.5V REM	+5V REM	+5VGL	+15V	-15V
U1	8				1			
U2	9,5,8				1			
U3	1,3,7				4,10,14			
U4	5				8			
U5		5				8		
U6			15&16					
U7			8					
U8			3					
U9								
U10		4						
U11		3						
U12		4						
U13								
U14			5					
U15		3,16 15,28,29				1,34 37,38		
U16		20				12&40		
U17		3,12,15				24		
U18		12,18				4,24		
U19		8,14				15,16		
U20		8				15,16		
U21		7				14		
U22		3,4,5,7 11,12,20				14		
U23		7				13,14		
U24		6,8				16		
U25		10				1,20		
U26		3,12,15				24		
U27		3,12,15				24		
U28		3,12,15				24		
U29		3,12,15				24		
U30		3,12,15				24		
U31		3,12,15				24		
U32							7	4
U33							7	4
U34							7	4
U35							14	
U36							7	4
U37							7	4
U38							7	4
U39							7	4
U40							7	4
U41							7	4
U42							7	4
U43							7	4
U44							7	4

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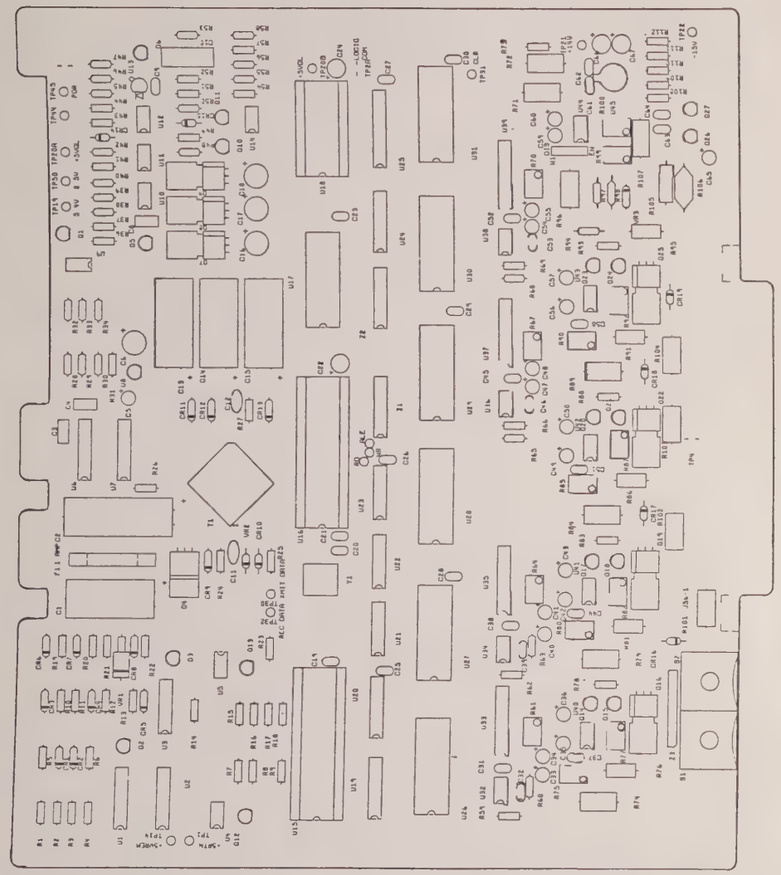
Figure 170-10. Analog Output Option Schematic Diagram



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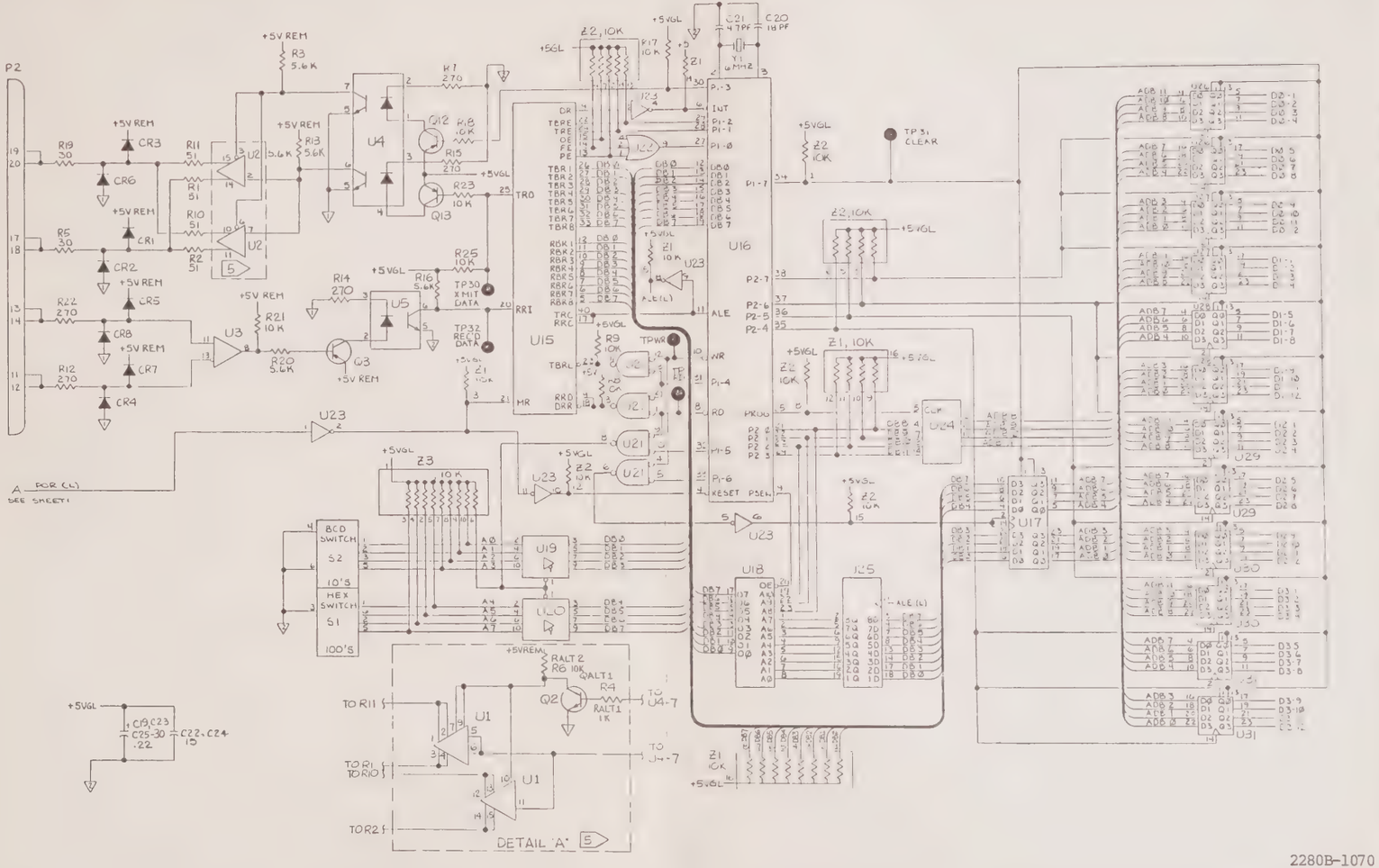

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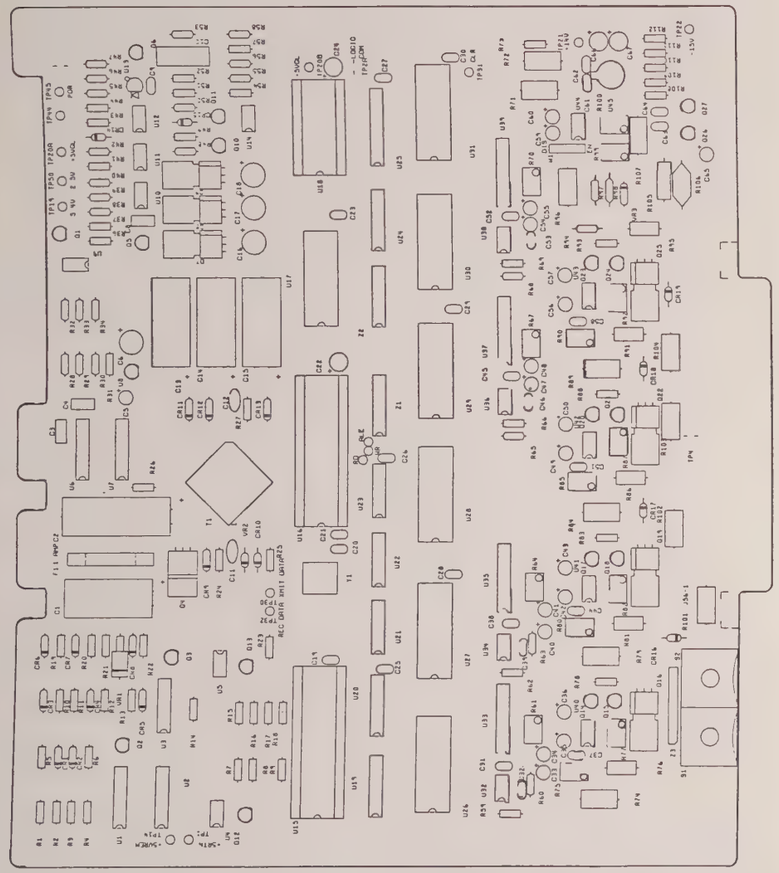
Figure 170-10. Analog Output Option Schematic Diagram (cont.)



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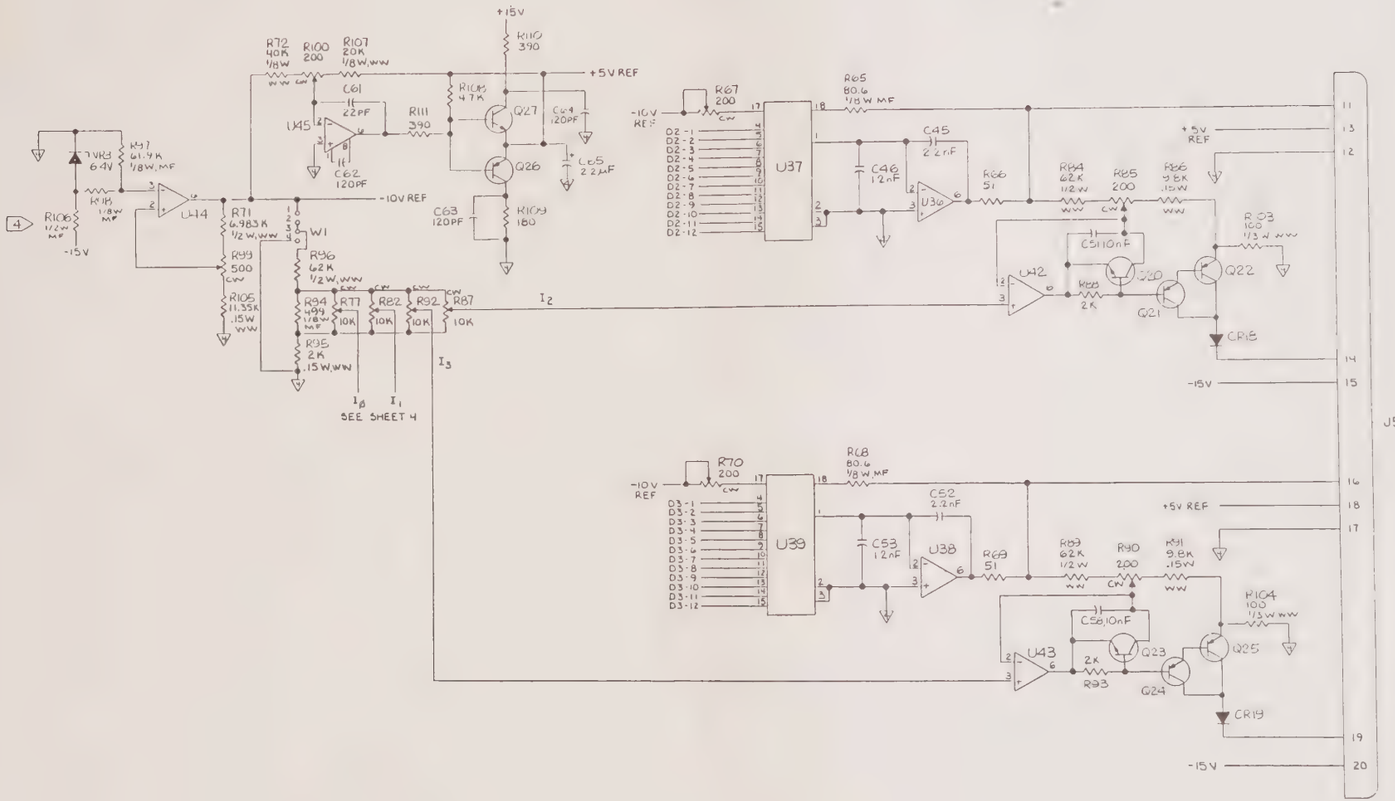

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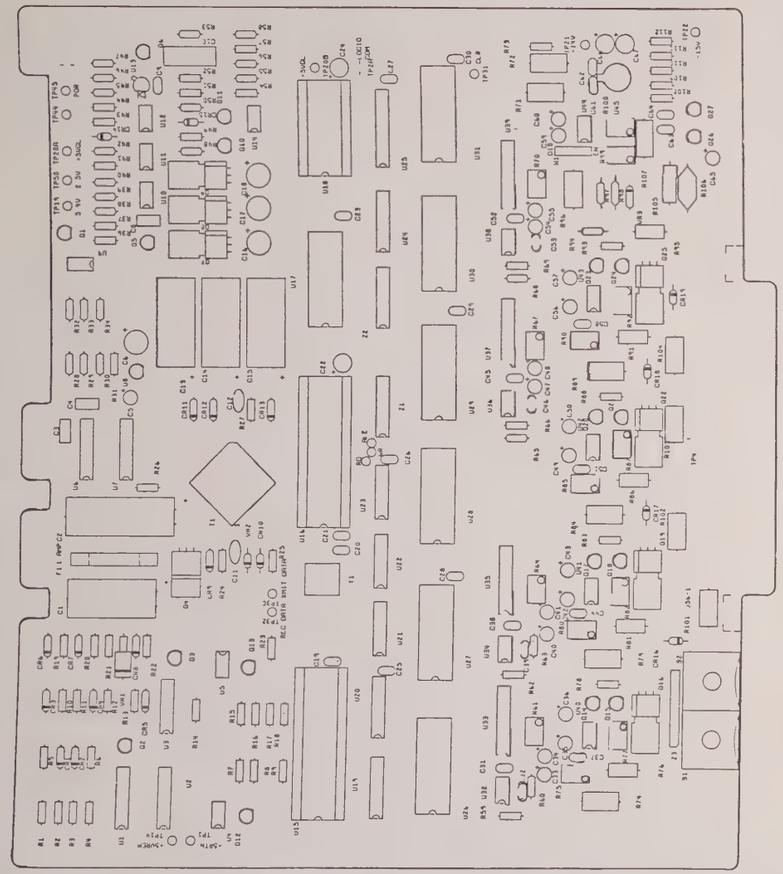
Figure 170-10. Analog Output Option Schematic Diagram (cont.)



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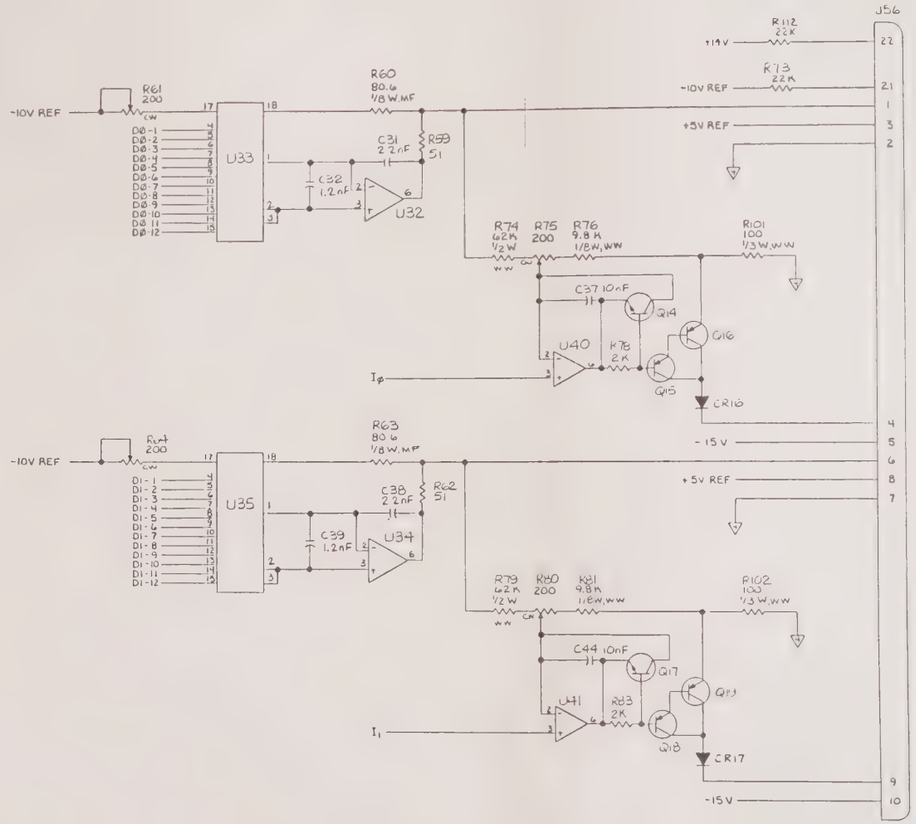

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Figure 170-10. Analog Output Option Schematic Diagram (cont.)

Option 2280A-171
Current Input Connector

DESCRIPTION

The Option 2280A-171 Current Input Connector is a screw-terminal assembly that mates through a card-edge connector with the Thermocouple/DC Volts Scanner (Option 2280A-162). Up to 20 channels of current inputs may be connected to the Current Input Connector. The Current Input Connector converts current to proportional voltages to be measured by the A/D Converter in the Data Logger. The Current Input Connector connects to the scanner through two 44-pin card-edge connectors. The entire connector assembly is enclosed in a plastic housing that provides protection for the terminal connections and strain relief for external wiring. When the connector is installed, the protective housing is attached to the Data Logger chassis with two retaining screws on each end of the assembly.

Each Input Connector channel has a precision shunt resistor and two screw terminals labeled HIGH and LOW (see Figure 171-1). Unlike the Isothermal and Voltage input connectors, there is no screw terminal for shield. The shield is internally connected to the LOW screw terminal.

WHERE TO FIND ADDITIONAL INFORMATION

In this subsection are Current Input Connector theory of operation, general maintenance, performance tests, calibration procedure, a parts list, and a schematic diagram. Installation and system configuration instructions are in the 2280 Series System Guide, and operating instructions are in the 2280 Series User Guide.

Test equipment required to perform the procedures in this subsection is listed in Table 171-1. A summary of test equipment required to perform all procedures in this manual is given in Table 1-1 in Section 1 of this manual.

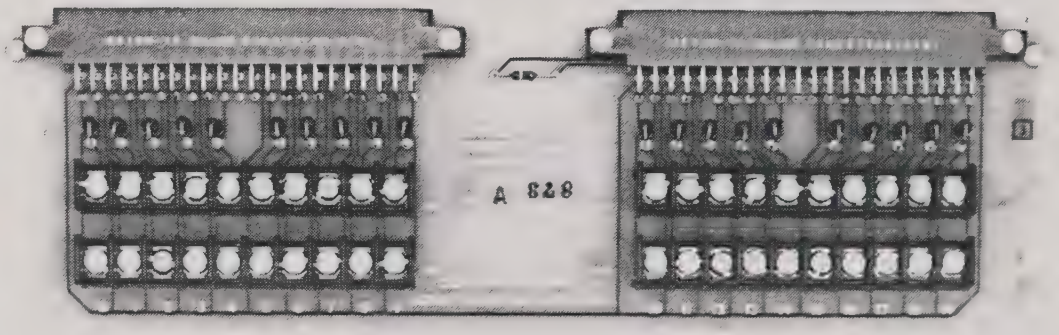


Figure 171-1. Current Input Connector

Table 171-1. Required Test Equipment

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
DC Calibrator	+/- 31.3 mV +/- 20 uV +2.048V +/- 50 uV -2.048V +/- 2 uV of +2.048 500 mV +/- 20 uV 6.2V +/- 155 uV 6.8V +/- 0.1V 5.0V +/- 100 uV 7.9V +/- 200 uV *63V +/- 800 uV 1.008V, +/- 40 uV	Fluke 343 *63V output used only for one optional test.
Resistor	8 Ohm, +/- .25%	Fluke Part # 641449
High Performance A/D Converter	.....	Fluke Option 2280A-161
Thermocouple/DC Volts Scanner	.....	Fluke Option 2280A-162

THEORY OF OPERATION

The Current Input Connector theory of operation discussion includes a functional description and a circuit analysis. In the case of this connector assembly, the schematic diagram at the end of this option subsection is the quickest and simplest circuit reference and should provide the answers to most questions.

Functional Description

The Current Input Connector receives dc currents through screw terminals and passes them through precision shunt resistors to produce dc voltages proportional to the current inputs. The dc voltages are routed through the Thermocouple/DC Volts Scanner to the A/D Converter, where they are digitized.

Circuit Analysis

Up to twenty dc current sources can be attached to the Current Input Connector through two screw terminals per channel: HI and LO. Dc current flows into the HI screw terminal, through an 8 ohm, .7W, 0.25% tolerance shunt resistor, and out the LO screw terminal. The resulting dc voltage that appears across the resistor is applied, on data logger command, through the Thermocouple/DC Volts Scanner to the A/D Converter where the voltage is converted to a digital value.

GENERAL MAINTENANCE

The Current Input Connector PCA normally does not require cleaning unless dirt, dust, or other contamination is visible on the surface. To clean the pca, follow PCA cleaning instructions in Section 4 of this manual.

PERFORMANCE TEST

The following test verifies that the Current Input Connector is fully functional. This procedure can be used as an initial acceptance test or as a troubleshooting aid.

1. Turn the front panel keyswitch to OFF. Disconnect all data logger power and high voltage inputs.

2. Set the A/D Converter address switch to 0, and install the A/D Converter in the top Data Logger option slot. Install the Thermocouple/DC Volts Scanner in the option slot immediately below the A/D Converter.

3. Connect test leads to the channel 0 HI and LO terminals on the Current Input Connector.

4. Install the Current Input Connector on the Thermocouple/DC Volts Scanner.

5. Connect an 8 ohm, 0.25% tolerance resistor in series between the test lead from the Current Input Connector HI terminal and the calibrator HI output. Connect the calibrator LO terminal to the Current Input Connector LO test lead.

6. Reconnect the data logger ac line or dc power input.

7. Turn the keyswitch to PROGRAM.

8. Program the Data Logger using the steps given in Table 171-2.

Table 171-2. Performance Test Programming Steps

STEP	KEYSTROKE (S)	RESULTING DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
7	0..19	CHANNEL NUMBER (OR BLOCK) = 0..19
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>?
10	D	A<D> DC VOLTS/CURRENT
11	ENTER	AD: DC RANGE <1-5>? 1
12	5	AD<5> 64.000 MADC
13	ENTER	AD: CHANNEL MENU CHOICE <1-5>? 1
14	EXIT	A: CHANNEL FUNCTION <A-Z>? D
15	EXIT	CHANNEL NUMBER (OR BLOCK) = C0..19
16	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

9. Set the calibrator to output 1.0080 Volts.

10. Press MONITOR, then 0, then ENTER. Verify that the value displayed for channel 0 is 63.000 mA, +/-0.010 mA.

11. Press MONITOR. The Data Logger should display:

    MAIN MENU CHOICE <M FOR MENU>? A

12. Set the calibrator for no output, disconnect the Current Input Connector test leads, and reconnect the test leads to HI and LO of the next channel to be tested.

13. Repeat steps 9 through 12 for each remaining channel, 1 through 19, substituting the appropriate channel number in step 10.

CALIBRATION

The Current Input Connector requires no calibration.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the Current Input Connector is given in Table 171-3. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the Current Input Connector is given in Figure 171-2.

TABLE 171-3. 2280A-171 CURRENT INPUT CONNECTOR
(SEE FIGURE 171-2.)

REFERENCE DESIGNATOR A->NUMERICS---)	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
H 1		STEEL,CAD.PLATED,.125X .500	276493	89536	276493	4		
H 2		WASHER,FLAT,STEEL,#4,0.030 THK	147728	89536	147728	4		
MP 1		CONNECTOR HOUSING, TOP	578971	89536	578971	1		
MP 2		CONNECTOR HOUSING, BOTTOM	656876	89536	656876	1		
MP 3		DECAL, CURRENT INPUT CONNECTOR	634576	89536	634576	1		
MP 4		DECAL, OPTION -171	634501	89536	634501	1		
MP 5		TAPE,FOAM,PVC,1/4W, 3/8 THK	601134	89536	601134	2		
P 36, 37		CONN,PWB EDGE,REC,90,0.156 CTR,44 POS	614313	89536	614313	2		
R 1- 19		RES,WW,8,+-0.25%,0.7W	641449	89536	641449	20		
R 20		RES,CF,3.9K,+-5%,0.25W	342600	80031	CR251-4-5P3K9	1	4	
TB 1- 4		SINGLE ROW, .325 CENTERS, 10 POSITION	615328	89536	615328	4		

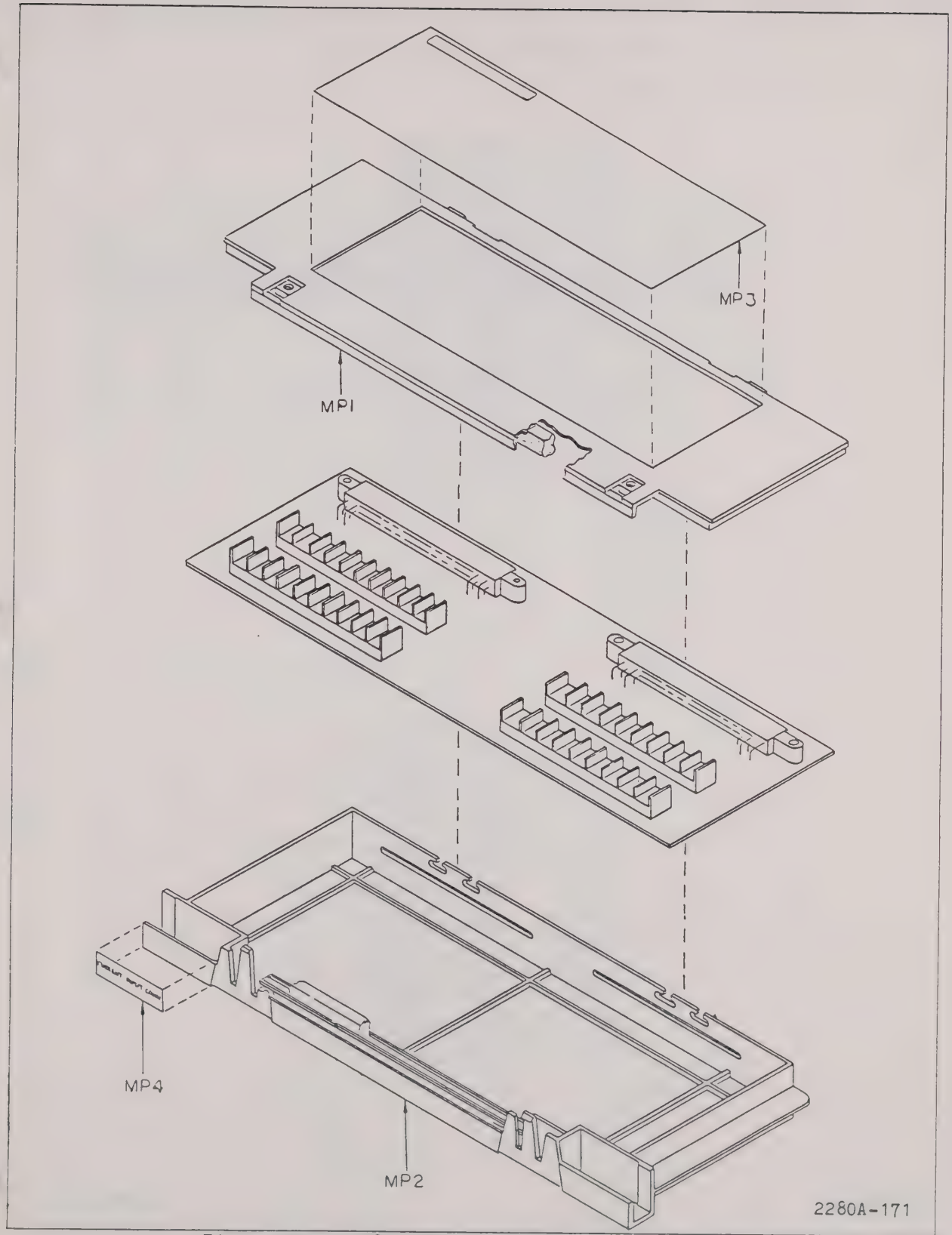
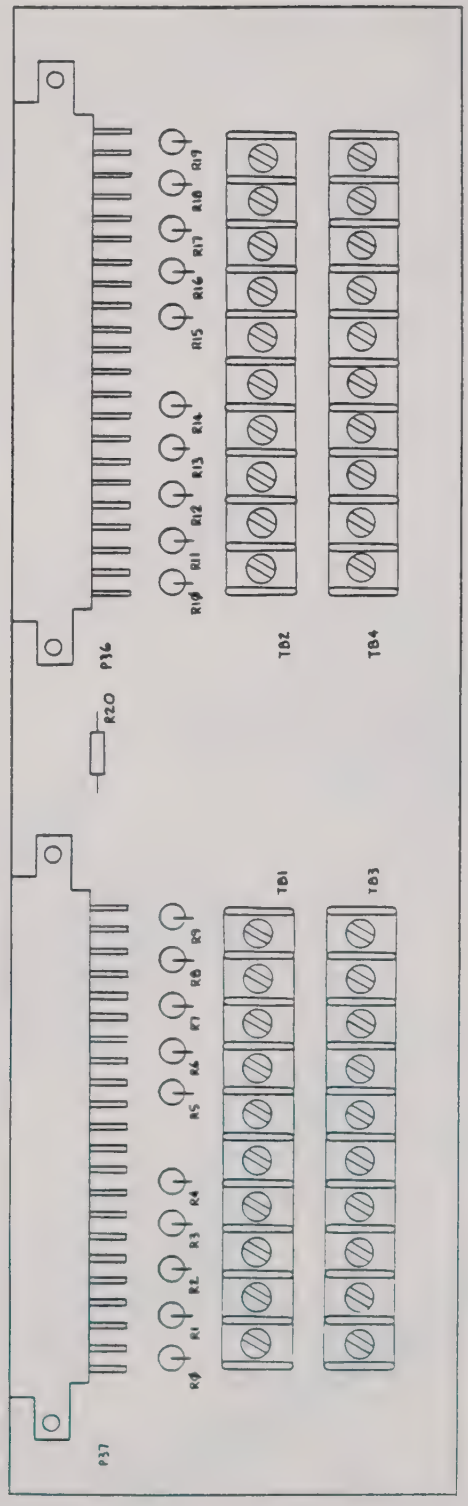


Figure 171-2 2280A-171 Current Input Connector



2280A-1671

Figure 171-2 2280A-171 Current Input Connector (cont.)

Figure 171-2. Current Input Connector Schematic Diagram

Option 2280A-174
Transducer Excitation Connector

DESCRIPTION

The Option 2280A-174 Transducer Excitation Connector, shown in Figure 174-1, mounts on the Transducer Excitation Module (Option 2280A-164) and provides it with screw-terminal connections for voltage and current sources. The combination of the -164 and -174 options allows the 2280 to make RTD temperature measurements, strain gage measurements, strain-based transducers measurements, and low resistance transducer measurements.

Five connecting terminals are available for each channel and twenty sets of these terminals are provided on each input connector. Wiring for each set of terminals is defined by the mode (4-Wire, 3-Wire Accurate, or 3-Wire Common) selected for the Transducer Excitation Scanner. Refer to the 2280 Series System Guide for wiring instructions.

WHERE TO FIND FURTHER INFORMATION

In this subsection are Transducer Excitation Connector theory of operation, general maintenance, a parts list, and a schematic diagram. Installation and system configuration instructions are in the 2280 Series System Guide, and operating and programming instructions are in the 2280 Series User Guide. Option specifications are in the Appendix in this manual and in the System Guide.

THEORY OF OPERATION

The Transducer Excitation Connector provides a path from screw terminals on the connector body to the card-edge connector pins on the Option 2280A-164 Transducer Excitation Module. Jumpers on the connector select either current or voltage excitation mode. The jumpers are set to current excitation when the connector is shipped from the factory. The 2280 Series System Guide gives instructions for connector configuration.

GENERAL MAINTENANCE

The Transducer Excitation Connector PCA normally does not require cleaning, but if dirt, dust, or other contamination is visible on the surface, the PCA should be cleaned. Follow PCA cleaning instructions in Section 4 of this manual.

PERFORMANCE TESTS

There is no separate performance test for the Transducer Excitation Connector since the connector is tested with the Transducer Excitation Module in that option's performance test (see subsection for Option 2280A-164).

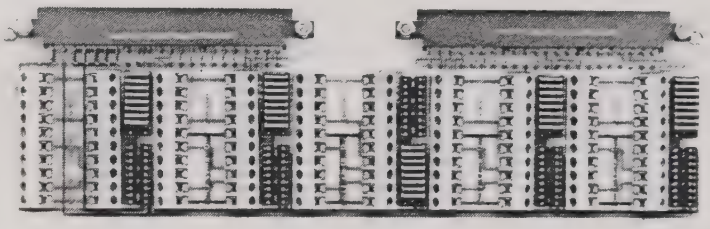


Figure 174-1. Transducer Excitation Connector

CALIBRATION

There are no calibration adjustments for the Transducer Excitation Connector.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the Transducer Excitation Connector is given in Table 174-1. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the Transducer Excitation Connector is given in Figure 174-2.

TABLE 174-1 2280A-174 TRANSDUCER EXCITATION CONNECTOR
(SEE FIGURE 174-2.)

REFERENCE DESIGNATOR A->NUMERICS---)	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
H 1		WASHER,FLAT,STEEL,#4,0.030 THK	147728	89536	147728	4		
H 2		STEEL,CAD.PLATED,.125X .500	276493	89536	276493	4		
JR 1I 2I 3I		HEADER,DIP,PROGRAMMED,18 PIN	715227	89536	715227	5		
JR 4I 5I			715227					
MP 1		CONNECTOR HOUSING, TOP	578971	89536	578971	1		
MP 2		CONNECTOR HOUSING, BOTTOM	656876	89536	656876	1		
MP 3		DECAL, TRANSDUCER EXCITATION CONN	722041	89536	722041	1		
MP 4		DECAL, OPTION -174	722058	89536	722058	1		
MP 5		TAPE,FOAM,PVC,1/4W,3/8 THK	603134	89536	603134	2		
P 54, 55		CONN,PWB EDGE,REC,90,0.156 CTR,44 POS	614313	89536	614313	2		
TB 1- 10		TERM STRIP,PWB,ANGL ENTRY,10 CONTACTS	501403	89536	501403	10		
XJR 1- 5		SOCKET,DIP,0.100 CTR,18 PIN	418228	91506	318-AG39D	10		

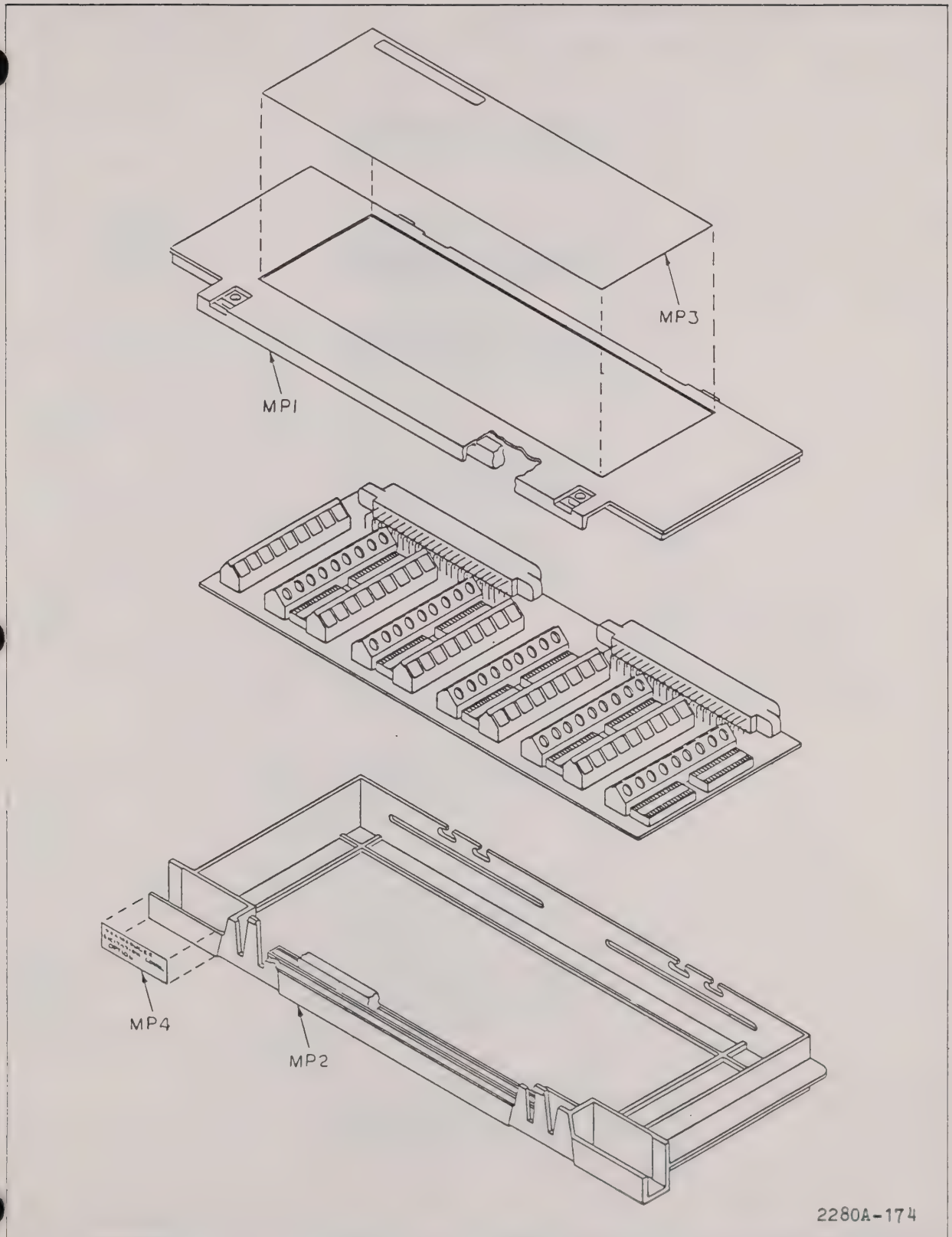
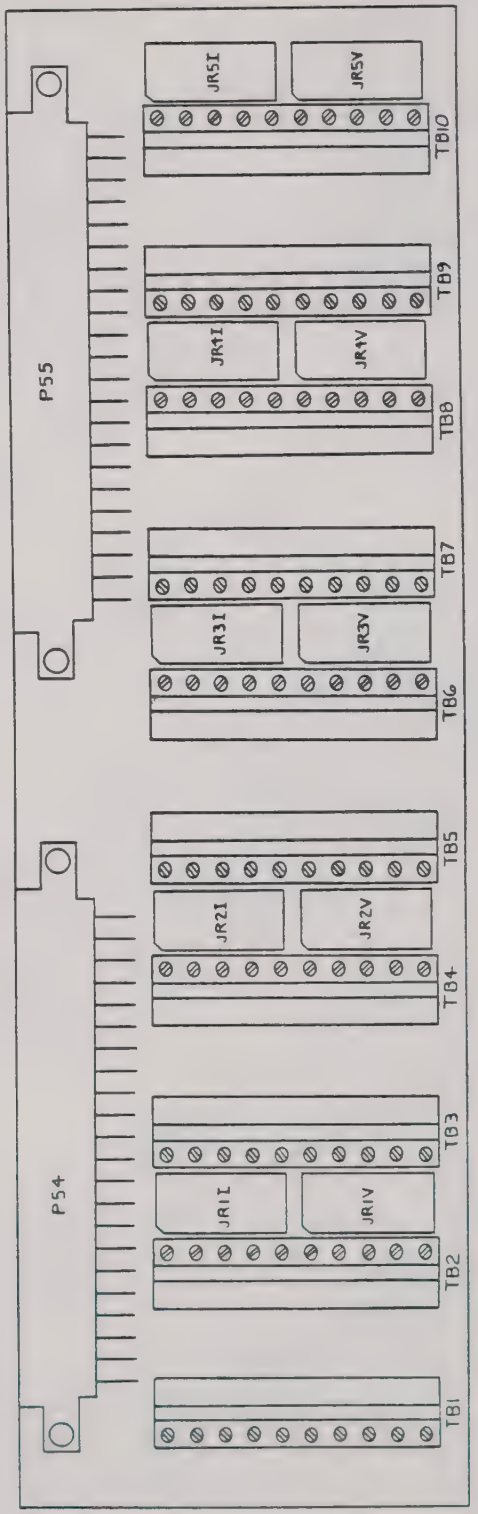
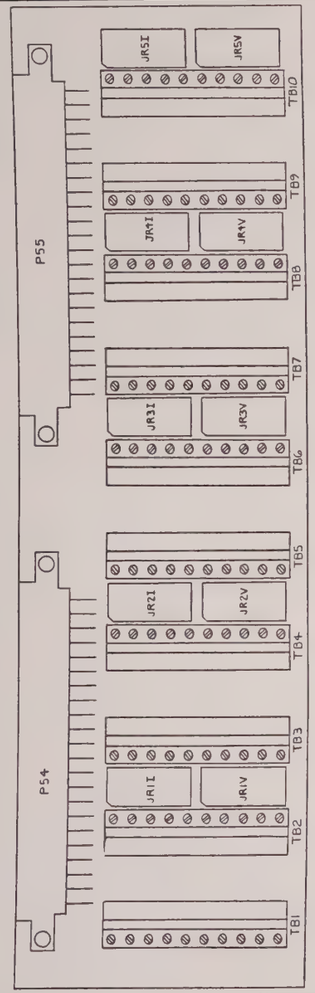


Figure 174-2. 2280A-174 Transducer Excitation Connector

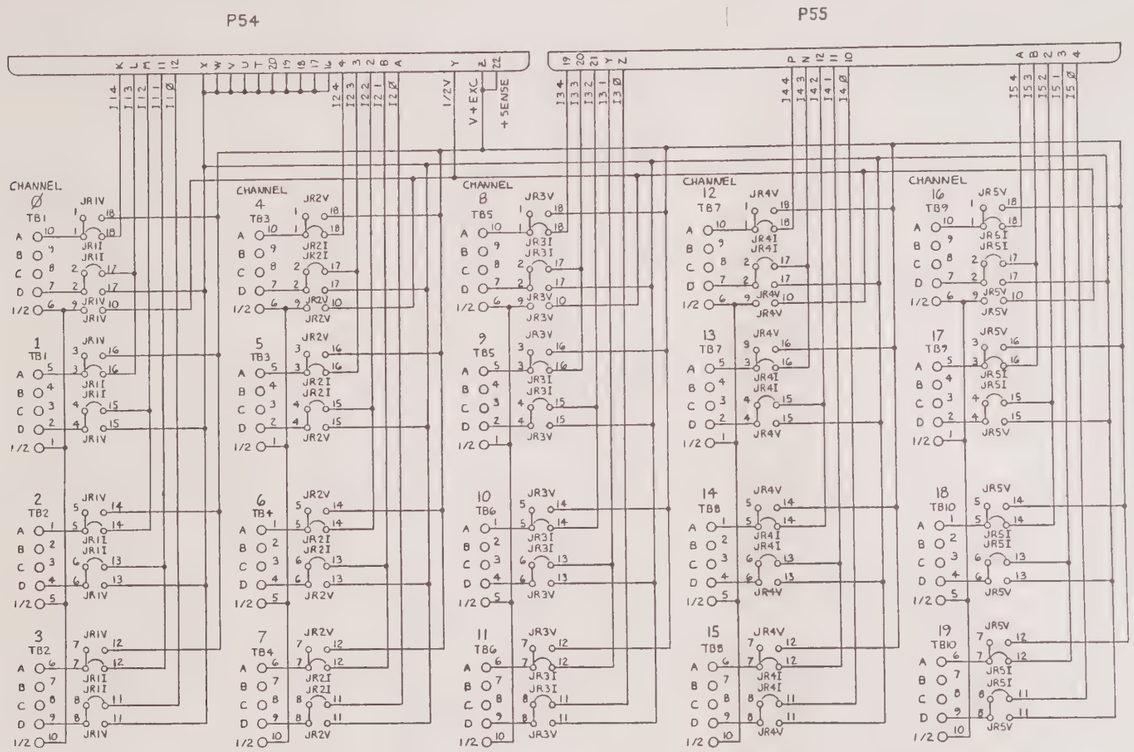


2280A-1674

Figure 174-2. 2280A-174 Transducer Excitation Connector (cont.)



2280A-1674



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL GRAPHIC SYMBOLS ARE IN ACCORDANCE WITH ANSI Y32.2 AND Y32.14
2. JUMPERS ON JR1 – JR5 ARE SHOWN INSTALLED IN CURRENT CONFIGURATION.

2280A-1074

Figure 174-2. Transducer Excitation Connector Schematic Diagram

Option 2280A-175
Isothermal Input Connector

DESCRIPTION

The Isothermal Input Connector illustrated in Figure 175-1 is a card-edge connector assembly that allows up to 20 channels of thermocouple or voltage input to be connected to the 2280A-162 Thermocouple/DC Volts Scanner option. The Isothermal Input Connector connects to the scanner through two 44-pin card-edge connectors. The entire connector assembly is enclosed in a plastic connector housing that provides protection for terminal connections and strain relief for external wiring. When installed, the housing is attached to the Data Logger chassis with retaining screws on each side.

There are three screw terminals per channel: HIGH, LOW and SHIELD. All channel terminals maintain 250 volts rms separation, and all terminals are surrounded by a block of aluminum that helps to maintain a uniform temperature among the terminals. A temperature sensor mounted in the isothermal block returns temperature readings to the Data Logger through the Thermocouple/DC Volts Scanner and the A/D Converter.

WHERE TO FIND ADDITIONAL INFORMATION

In this subsection, the Isothermal Input Connector theory of operation, general maintenance, performance tests, calibration procedure, a parts list, and a schematic diagram are given. Installation and system configuration instructions are given in the 2280 Series System Guide, and operating and programming instructions are given in the 2280 Series User Guide.

Test equipment required to perform the procedures in this subsection is listed in Table 175-1. A summary of test equipment required to perform all procedures in this manual is given in Table 1-1 in Section 1 of this manual.

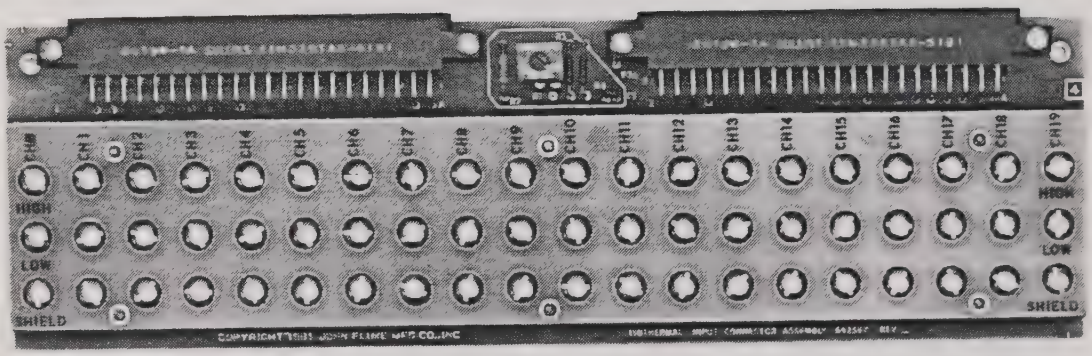


Figure 175-1. Isothermal Input Connector

Table 175-1. Required Test Equipment

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
High Performance A/D Converter	.....	Fluke Option 2280A-161
Thermocouple/DC Volts Scanner	.....	Fluke Option 2280A-162
Room Temperature Oil/Water Bath	.....	.....
Mercury Thermometer	0.02 degrees C resolution	Princo ASTM-56C
Thermocouple	Type J or K	Fluke P-20J or P-20K

THEORY OF OPERATION

The Isothermal Input Connector theory of operation includes a functional description and a detailed circuit description. The schematic diagram for this assembly is given at the end of this option subsection.

Functional Description

By providing connections for up to twenty thermocouples through its screw terminals, the Isothermal Input Connector allows the Data Logger to make stable temperature readings. The assembly contains a temperature sensor that measures the isothermal block temperature, allowing automatic reference-junction compensation of thermocouple inputs. The isothermal aluminum block surrounds the terminals on the connector maintains the terminals, input leads, and reference junction at the same temperature.

The Isothermal Input Assembly, when installed on the Thermocouple/DC Volts Scanner, changes the type code of the scanner, thereby signaling the mainframe to permit thermocouple measurements on the channels associated with that scanner and Isothermal Input Connector.

Detailed Circuit Description

TERMINAL CIRCUIT

There are three terminals for each channel, one each for the high input (HI), the low input (LO), and shield (SHIELD). They provide termination points for the wiring carrying the incoming dc voltages from thermocouples or voltage sources. The incoming voltages are passed through the Isothermal Input Connector to the Thermocouple/DC Volts Scanner, where channels are selected and conditioned for conversion by the A/D Converter.

REFERENCE JUNCTION CIRCUIT

The temperature of the isothermal terminal block is sensed by the base-emitter junction of transistor Q1. Bias voltage is supplied to the transistor by the A/D Converter +6.2V reference voltage which is passed through the Thermocouple/DC Volts Scanner and divided down by factory-chosen resistors. The Q1 base-emitter voltage of approximately 600mV is divided in half by R3 and R4, with the 300mV output of the divider supplied to the Thermocouple/DC Volts Scanner. The scanner and the A/D Converter measure this signal on the 512mV range each time a thermocouple measurement is made on the associated input channels, thereby providing a measurement to the data logger for thermocouple linearization processes. Capacitor C1 reduces the sensor's susceptibility to electro-magnetic interference (EMI), and resistor R5 provides a bias current return path.

GENERAL MAINTENANCE

The Isothermal Input Connector Assembly PCA normally does not require cleaning unless dirt, dust, or other contamination is visible on the surface. Follow PCA cleaning instructions in Section 4 of this manual.

PERFORMANCE TESTS

The following performance test can be used to verify that the Isothermal Input Connector is functioning properly. The performance test can also be used as an initial acceptance test. The performance test is divided into two parts, either of which may be performed independently. Both parts are necessary to fully test the connector. The two parts of the performance test are:

- Channel Integrity Test

  The channel integrity test verifies that all channels on the Isothermal Input Connector are functional.

- Reference Junction Accuracy Test

  The reference junction accuracy test verifies that the Isothermal Input Connector channels meet accuracy specifications.

WARNING

THE DATA LOGGER CONTAINS HIGH VOLTAGES WHICH CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE EQUIPMENT. TURN OFF THE DATA LOGGER AND REMOVE ALL POWER SOURCES BEFORE PERFORMING ANY OF THE PROCEDURES IN THIS SECTION.

1. Turn the keyswitch to OFF. Disconnect the Data Logger power input, and remove the High Performance A/D Converter (Option 2280A-161) if one is installed.

2. Set the address switch on the A/D Converter to 0 (refer to the A/D Converter subsection of the 2280 Series System Guide for switch setting instructions).

3. Install the A/D Converter in the top Data Logger option slot, then install the Thermocouple/DC Volts Scanner (2280A-162) in the slot immediately below the A/D Converter.

4. Reconnect the Data Logger ac line or battery power input.

5. Turn the keyswitch to the PROGRAM position.

6. Enter the steps given in Table 175-2 to program Data Logger.

7. Connect a shorting wire between the HIGH and LOW terminals of channel 0 on the Isothermal Input Connector. Install the connector on the scanner.

8. Press MONITOR, then 0 for channel 0, then ENTER. Verify that the value displayed for channel 0 is approximately the ambient temperature.

9. Press MONITOR. The Data Logger should display:

   MAIN MENU CHOICE <M FOR MENU>? A

10. Repeat steps 7 through 9 for the remaining channels (1 through 19), substituting the appropriate channel number in steps 7 and 8.

11. The channel integrity test is complete.

Table 175-2. Temperature Sensor Type Programming Steps

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = CO
7	O..19	CHANNEL NUMBER (OR BLOCK) = O..19
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>? P
10	T	A<T> THERMOCOUPLE
11	ENTER	AT: TC TYPE <J,K,T,E,R,S,B,N,C,H,V>? J
12	ENTER	AT: CHANNEL MENU CHOICE <1-5>? 1
13	EXIT	A: CHANNEL FUNCTION <A-Z>? T
14	EXIT	CHANNEL NUMBER (OR BLOCK) = CO..19
15	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

*If a thermocouple type other than J is in use, type the appropriate code letter in step 11 (refer to the 2280 Series System Guide for thermocouple programming instructions).

Accuracy Verification Test

WARNING

THE DATA LOGGER CONTAINS HIGH VOLTAGES WHICH CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE EQUIPMENT. TURN OFF THE DATA LOGGER AND REMOVE ALL POWER SOURCES BEFORE PERFORMING ANY OF THE PROCEDURES IN THIS SECTION.

1. Perform steps 1 through 6 of the channel integrity test.
2. Connect a thermocouple to the HIGH and LOW terminals of channel ' ' on the Isothermal Input Connector. Install the connector on the scanner.
3. Turn the keyswitch to RUN.
4. Insert the thermocouple and a thermometer in a room temperature bath, and allow them to thermally stabilize.
5. Press MONITOR, then 11, then ENTER.
6. Verify that the value displayed on the Data Logger is the temperature of the room temperature bath as measured by the mercury thermometer within the tolerances stated in Table 175-3.

7. The accuracy verification test is complete.

Table 175-3. Thermocouple Accuracy Specifications

TC TYPE	90 DAYS @ 15-35 DEGREES C	1 YEAR @ 15-35 DEGREES C
JNBS	.35	.4
KNBS	.35	.4
TNBS	.35	.4
ENBS	.35	.4
RNBS	1.15	1.35
SNBS	1.15	1.35
BNBS	1.05	1.25
JDIN	.35	.4
TDIN	.35	.4
NNBS	.35	.4
C	.85	1.05

CALIBRATION

If thermocouple readings taken in the previous accuracy verification tests are found to be out of tolerance, the Thermocouple Input Connector requires calibration. Perform the following steps to calibrate the Isothermal Input Connector:

WARNING
THE DATA LOGGER CONTAINS HIGH VOLTAGES WHICH CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE EQUIPMENT. TURN OFF THE DATA LOGGER AND REMOVE ALL POWER SOURCES BEFORE PERFORMING ANY OF THE PROCEDURES IN THIS SECTION.

1. Turn the keyswitch to OFF. Disconnect the Data Logger power and high voltage inputs, and remove the High Performance A/D Converter (2280A-161) if one is installed.

2. Set the address switch on the A/D Converter to 0 (refer to the A/D Converter option section for switch setting information).

3. Install the A/D Converter in the top Data Logger option slot, then install the Thermocouple/DC Volts Scanner (Option 2280A-162) in the slot immediately below the A/D Converter.

4. Reconnect the Data Logger ac line or dc battery power input.

5. Turn the keyswitch to PROGRAM.

6. Enter the steps given in Table 175-4 to program Data Logger.

Table 175-4. Temperature Sensor Type Programming Steps

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
7	0..19	CHANNEL NUMBER (OR BLOCK) = 0..19
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>?
10	T	A<T> THERMOCOUPLE
11	ENTER	AT: TC TYPE <J,K,T,E,R,S,B,N,C,H,V>? J
12	ENTER	AD: CHANNEL MENU CHOICE <1-5>? 1
13	EXIT	A: CHANNEL FUNCTION <A-Z>? T
14	EXIT	CHANNEL NUMBER (OR BLOCK) = C0..19
15	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

*If a thermocouple type other than J is in use, enter the appropriate code letter in step 11 (refer to the 2280 Series User Guide for programming instructions).

8. Connect a thermocouple to the HIGH and LOW terminals of channel 11 on the Isothermal Input Connector. Install the connector on the Thermocouple/DC Volts Scanner (Option 2280A-162).

9. Insert the thermocouple and thermometer in a room temperature bath, and allow 20 minutes for the temperature indication to stabilize.

10. Press MONITOR, then 11, then ENTER.

11. Adjust resistor R1 on the Thermocouple Input Connector until the Data Logger displays the same temperature reading as the mercury thermometer.

12. Calibration of the Isothermal Input Connector is complete.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the Isothermal Input Connector is given in Table 175-5. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the Isothermal Input Connector is given in Figure 175-2.

TABLE 175-5. 2280A-175 ISOTHERMAL INPUT CONNECTOR
(SEE FIGURE 175-2.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOT -E
C 1		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	1		
H 1		WASHER,LOCK,SPLIT,S STEEL,#4	147603	89536	147603	6		
H 2		SCREW,MACH,PHS,BR,6-32X1/4	615591	89536	615591	60		
H 3		STEEL,CAD.PLATED,.125X .500	276493	89536	276493	4		
H 4		SCREW,MACH,PHP,S.STL,4-40X1-7/16	403782	89536	403782	6		
H 5		WASHER,FLAT,STEEL,#4,0.030 THK	147728	89536	147728	4		
MP 1		BLOCK,ISOTHERMAL	579110	89536	579110	1		
MP 2		ISOTHERMAL,INSULATOR	579128	89536	579128	1		
MP 3		STANDOFF,BR,RD,SWGD,ANTI-ROT,6-32THRD	643148	89536	643148	60		
MP 4		CONNECTOR HOUSING, TOP	578971	89536	578971	1		
MP 5		CONNECTOR HOUSING, BOTTOM	656876	89536	656876	1		
MP 6		DECAL, ISOTHERMAL INPUT CONNECTOR	634584	89536	634584	1		
MP 7		DECAL, OPTION -175	634519	89536	634519	1		
MP 8		TAPE,FOAM,PVC,1/4W,3/8 THK	603134	89536	603134	2		
P 36, 37		CONN,PWB EDGE,REC,90,0.156 CTR,44 POS	614313	89536	614313	2	1	
Q 1	*	TRANSISTOR,SI,NPN,SELECTD,TEMP SENSOR	640862	89536	640862	1		
R 1		RES,VAR,CERM,50K,+-10%,0.5W	697300	89536	697300	1		
R 2		RES,MF,34.8K,+-1%,0.125W,25PPM	312181	89536	312181	1		
R 3, 4		MATCHED RES. SET ISOTHERMAL	617597	89536	617597	1		
R 8		RES,MF,100K,+-1%,0.125W,100PPM	248807	91637	CMF551003F	1		

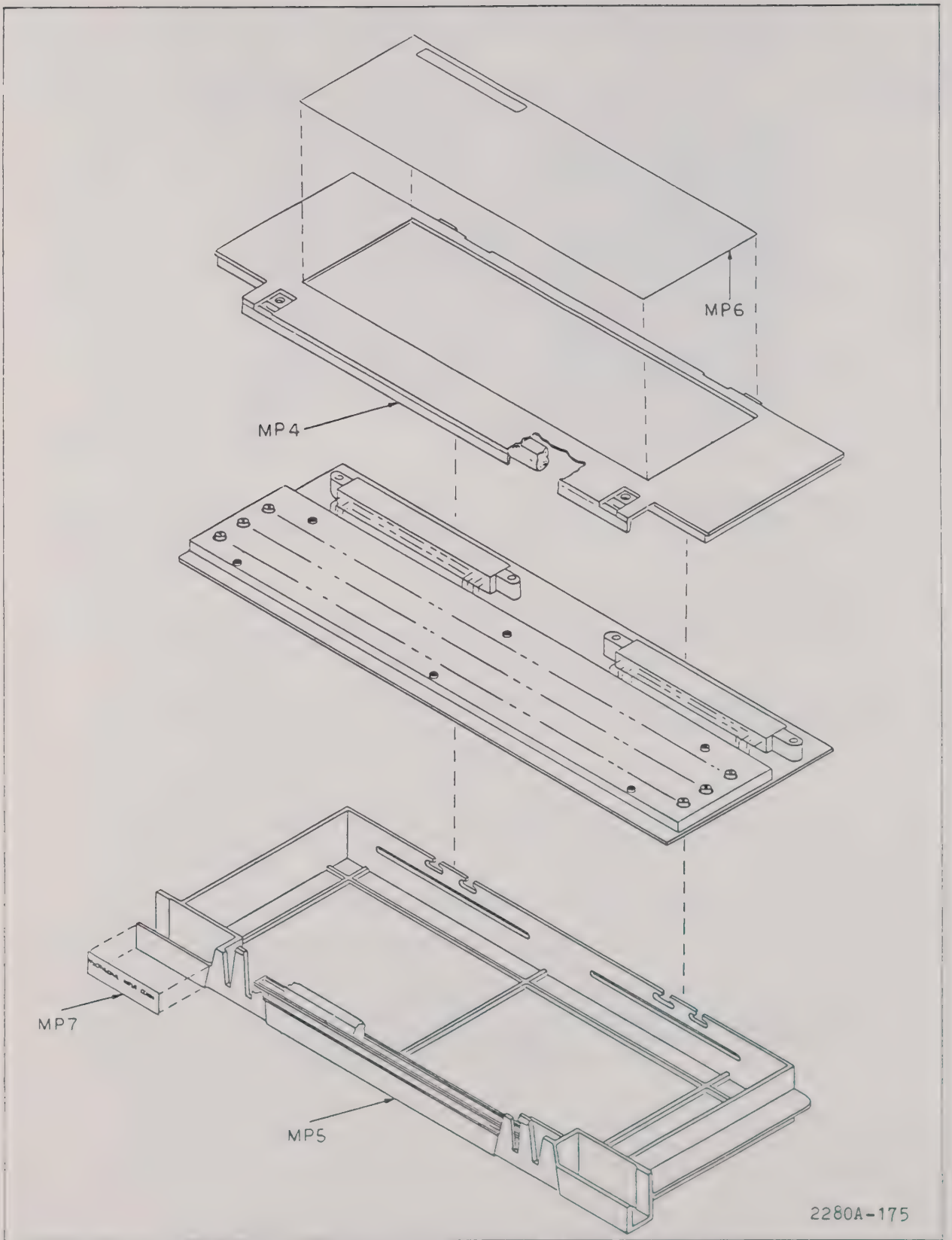
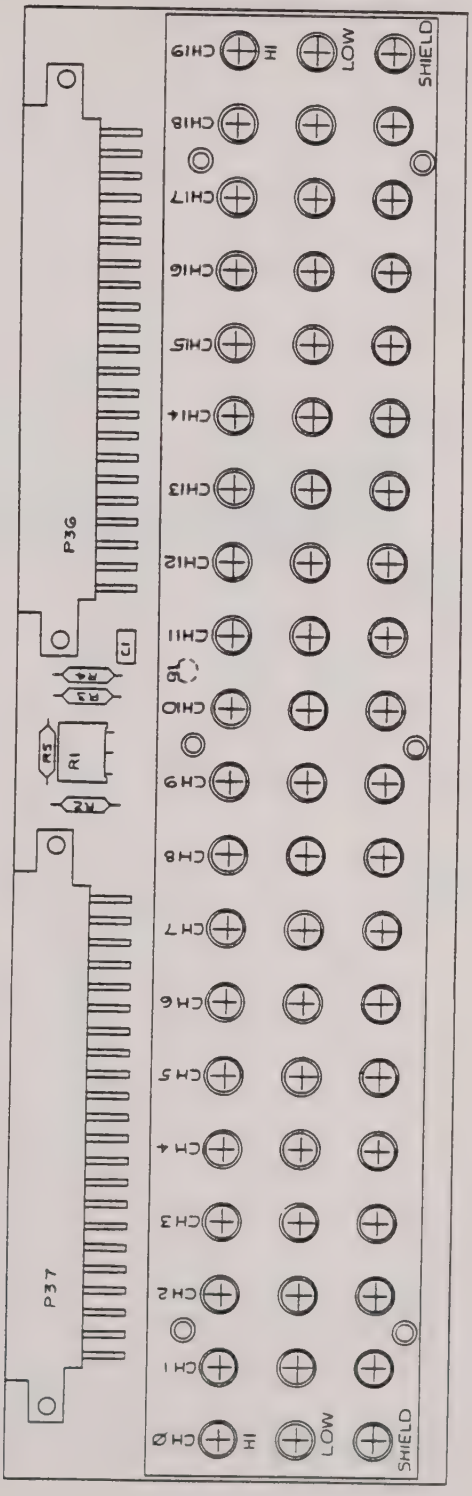
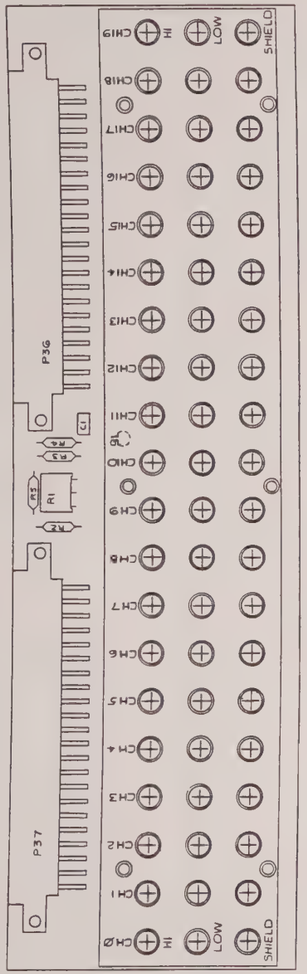


Figure 175-2. 2280A-175 Isothermal Input Connector

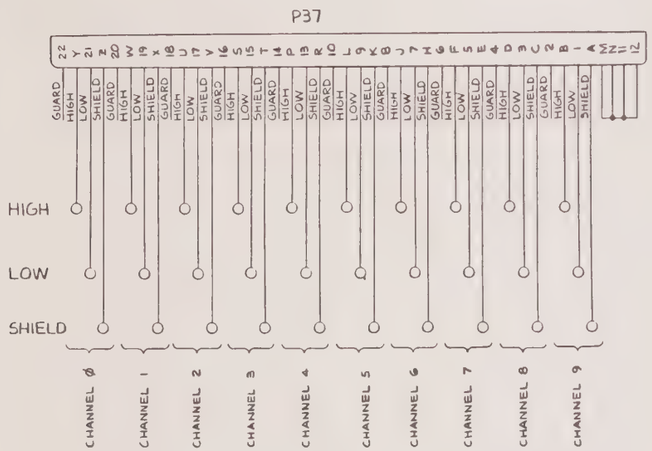


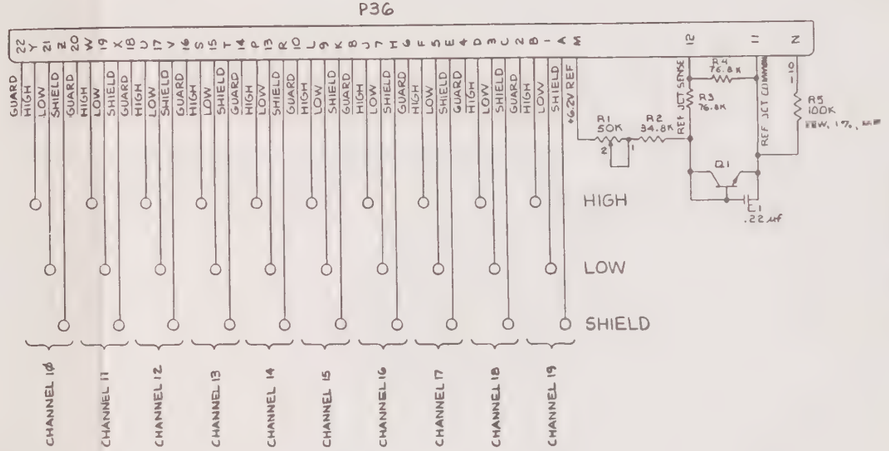
2280A-1675

Figure 175-2. 2280A-175 Isothermal Input Connector (cont.)



2280A-1675





2280A-1075

Figure 175-2. Isothermal Input Connector Schematic Diagram

Voltage Input Connector
Option 2280A-176

DESCRIPTION

The 2280A-176 Voltage Input Connector option is a card-edge connector assembly which connects to the 2280A-162 Thermocouple/DC Volts Scanner and provides up to 20 channels of dc voltage input. The entire connector assembly is enclosed in a plastic housing that provides protection for terminal connections and strain relief for external wiring. When installed, the housing attaches to the Data Logger chassis with retaining screws on each end. The Voltage Input Connector is illustrated in Figure 176-1.

WHERE TO FIND ADDITIONAL INFORMATION

The Voltage Input Connector theory of operation, performance tests, general maintenance, calibration procedure, parts list, and schematic diagram are located in this subsection. Installation and system configuration instructions are in the 2280 Series System Guide, and operating and programming instructions are in the 2280 Series User Guide.

Test equipment required to perform the procedures in this subsection is listed in Table 176-1. A summary of test equipment required to perform all procedures in this manual is given in Table 1-1 in Section 1 of this manual.

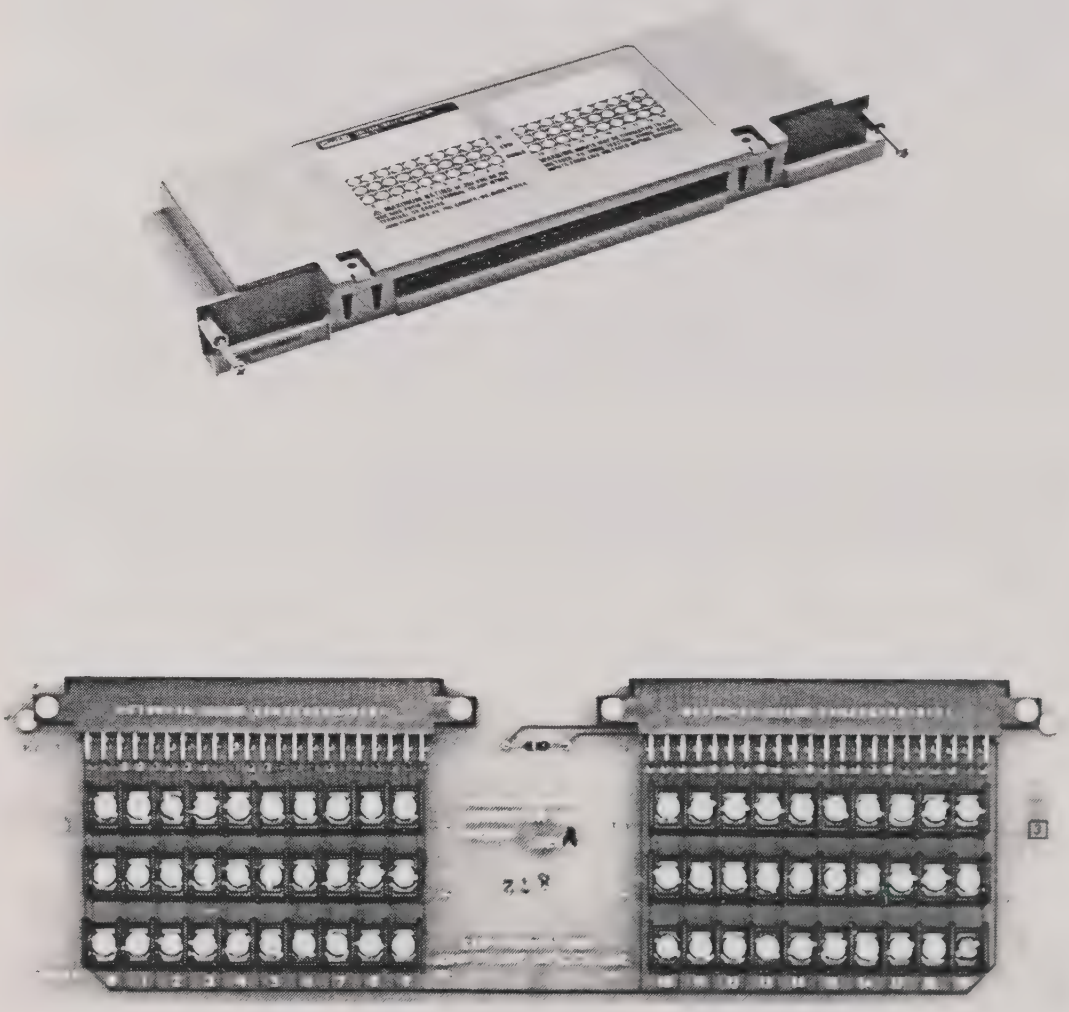


Figure 176-1. Voltage Input Connector

Table 176-1. Required Test Equipment

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
DC Calibrator	+/- 31.3 mV +/- 20 uV +2.048V +/- 50 uV -2.048V +/- 2 uV of +2.048 500 mV +/- 20 uV 6.2V +/- 155 uV 6.8V +/- 0.1V 5.0V +/- 100 uV 7.9V +/- 200 uV *63V +/- 800 uV 1.008V, +/- 40 uV	Fluke 343 *63V output used only for one optional test.
100:1 Divider	+/- 0.005%	Fluke Y2022
High Performance A/D Converter	.....	Fluke Option 2280A-161
Thermocouple/DC Volts Scanner	.....	Fluke Option 2280A-162
Voltage Input Connector	.....	Fluke Option 2280A-176

THEORY OF OPERATION

The Voltage Input Connector theory of operation includes a functional description and a detailed circuit description. The schematic diagram for the connector is located at the end of this option subsection.

Functional Description

The Voltage Input Connector provides screw terminal inputs for external dc voltage sources. Received voltages are then routed to the Thermocouple/DC Volts Scanner.

Detailed Circuit Description

Up to twenty dc voltage sources can be attached to the Voltage Input Connector through HIGH, LOW and SHIELD terminals for each channel, with 250 V rms spacing maintained between terminals.

The dc voltages across the high and low channel terminals are routed to the scanner through two card-edge connectors. The voltage inputs are then selected and conditioned by the Thermocouple/DC Volts Scanner for conversion by the A/D Converter.

GENERAL MAINTENANCE

The Voltage Input Connector PCA normally does not require cleaning unless dirt, dust, or other contamination is visible on the surface. Follow PCA cleaning instructions in Section 4 of this manual.

PERFORMANCE TEST

The following performance test can be used to verify that the Voltage Input Connector is functioning properly. The performance test can also be used as an initial acceptance test.

WARNING

THE DATA LOGGER CONTAINS HIGH VOLTAGES WHICH CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE EQUIPMENT. TURN OFF THE DATA LOGGER AND REMOVE ALL POWER SOURCES BEFORE PERFORMING ANY OF THE PROCEDURES IN THIS SECTION.

1. Turn the keyswitch to OFF. Disconnect all data logger power and high voltage inputs, and remove the High Performance A/D Converter (2280A-161) if one is installed.

2. Set the address switch on the A/D Converter to 0 (refer to the A/D Converter subsection of the 2280 Series System Guide for switch setting instructions).

3. Install the A/D Converter in the top Data Logger option slot, then install the DC Volts/Thermocouple Scanner (Option 2280A-162) in the slot immediately below the A/D Converter.

4. Connect test leads to the HI and LO terminals for channel 0 on the input connector, then install the Voltage Input Connector on the Scanner.

5. Reconnect the data logger ac line or dc battery power input.

6. Turn the keyswitch to the PROGRAM position.

7. Program the Data Logger using the steps given in Table 176-2.

Table 176-2. Performance Test Programming

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1		MAIN MENU CHOICE <M FOR MENU>.? A
2	E	<E> ERASE ALL OF PROGRAM MEMORY
3	ENTER	REALLY ERASE ALL MEMORY <Y,N>? N
4	Y	REALLY ERASE ALL MEMORY <Y,N>? Y
5	ENTER	MAIN MENU CHOICE <M FOR MENU>? A
6	ENTER	CHANNEL NUMBER (OR BLOCK) = C0
7	0..19	CHANNEL NUMBER (OR BLOCK) = 0..19
8	ENTER	PROGRAM COPY DELETE OR LIST <P,C,D,L>? P
9	ENTER	A: CHANNEL FUNCTION <A-Z>?
10	D	A<D> DC VOLTS/CURRENT
11	ENTER	AD: DC RANGE <1-5>? 1
12	4	AD<4> 64.000 MVDC
13	ENTER	AD: CHANNEL MENU CHOICE <1-5>? 1
14	EXIT	A: CHANNEL FUNCTION <A-Z>? D
15	EXIT	CHANNEL NUMBER (OR BLOCK) = C0..19
16	EXIT	MAIN MENU CHOICE <M FOR MENU>? A

8. Connect the calibrator output to the input of the 100:1 divider. Connect the voltage divider output to the input connector test leads.

9. Set the calibrator output to 6.3 volts.

10. Press MONITOR, then 0, then ENTER. Verify that the value displayed for channel 0 is 63.000 mV +/- 0.010 mV.

11. Press MONITOR. The Data Logger should display:

    MAIN MENU CHOICE <M FOR MENU>? A

12. Set the calibrator output to zero. Move the voltage input connector test leads to the terminals of the next channel to be tested.

13. Repeat steps 9 through 12 for each remaining channel, 1 through 19, substituting the appropriate channel number in step 10.

14. The Voltage Input Connector performance test is complete.

CALIBRATION

The Voltage Input Connector requires no calibration.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the Voltage Input Connector is given in Table 176-3. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the Voltage Input Connector is given in Figure 176-2.

TABLE 176-3. 2280A-176 VOLTAGE INPUT CONNECTOR PCA
(SEE FIGURE 176-2.)

REFERENCE DESIGNATOR A->NUMERICS----)	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
H 1		STEEL,CAD.PLATED,.125X .500	276493	89536	276493	4		
H 2		WASHER,FLAT,STEEL,#4,0.030 THK	147728	89536	147728	4		
MP 1		CONNECTOR HOUSING, TOP	578971	89536	578971	1		
MP 2		CONNECTOR HOUSING, BOTTOM	656876	89536	656876	1		
MP 3		DECAL, OPTION -176	634527	89536	634527	1		
MP 4		DECAL, VOLTAGE INPUT CONNECTOR	634592	89536	634592	1		
MP 5		TAPE,FOAM,PVC,1/4W,3/8 THK	603134	89536	603134	2		
P 36, 37		CONN,PWB EDGE,REC,90,0.156 CTR,44 POS	614313	89536	614313	2		
R 1		RES,CF,3.9K,+-5%,0.25W	342600	80031	CR251-4-5P3K9	1		
TB 1- 6		SINGLE ROW, .325 CENTERS, 10 POSITION	615328	89536	615328	6		

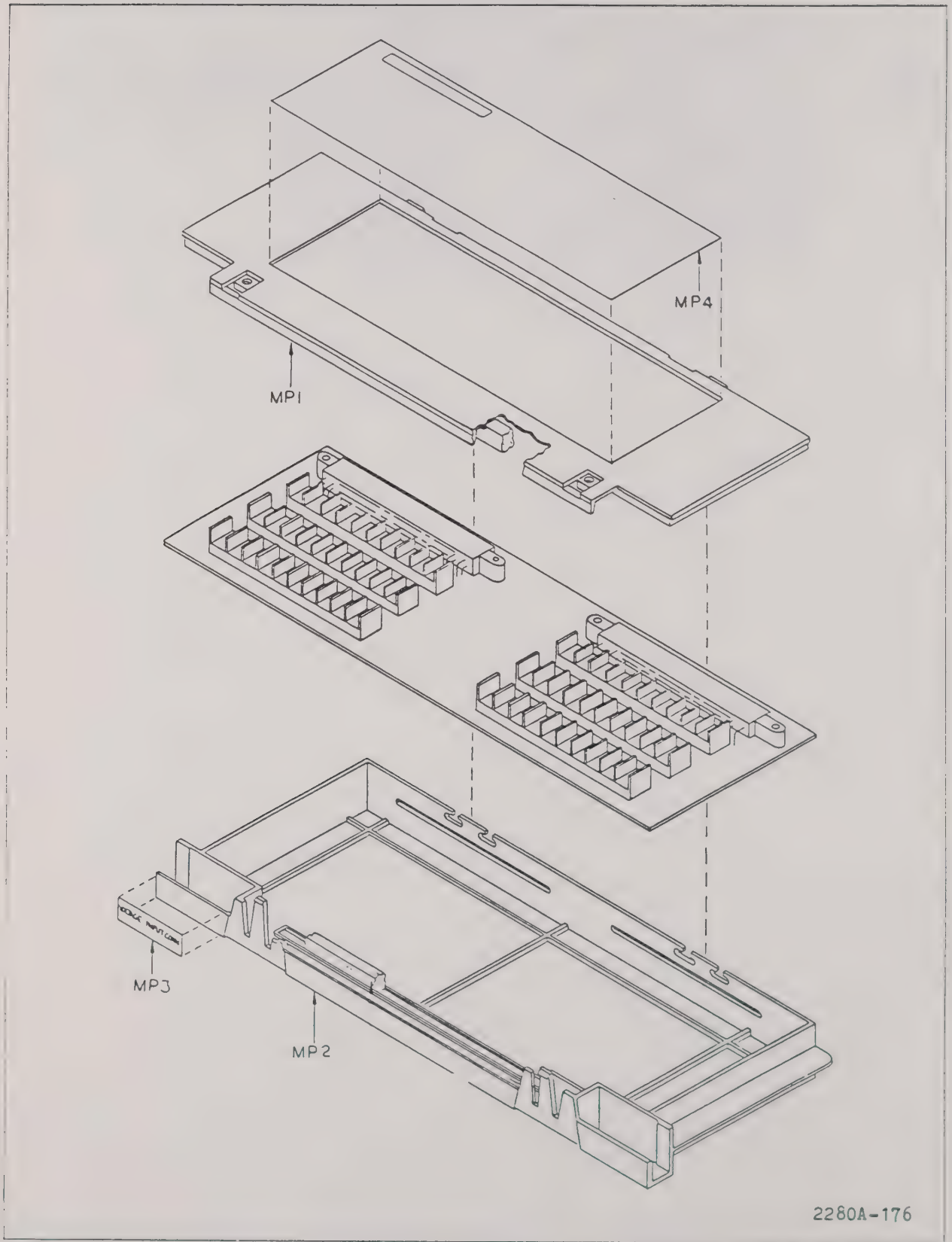
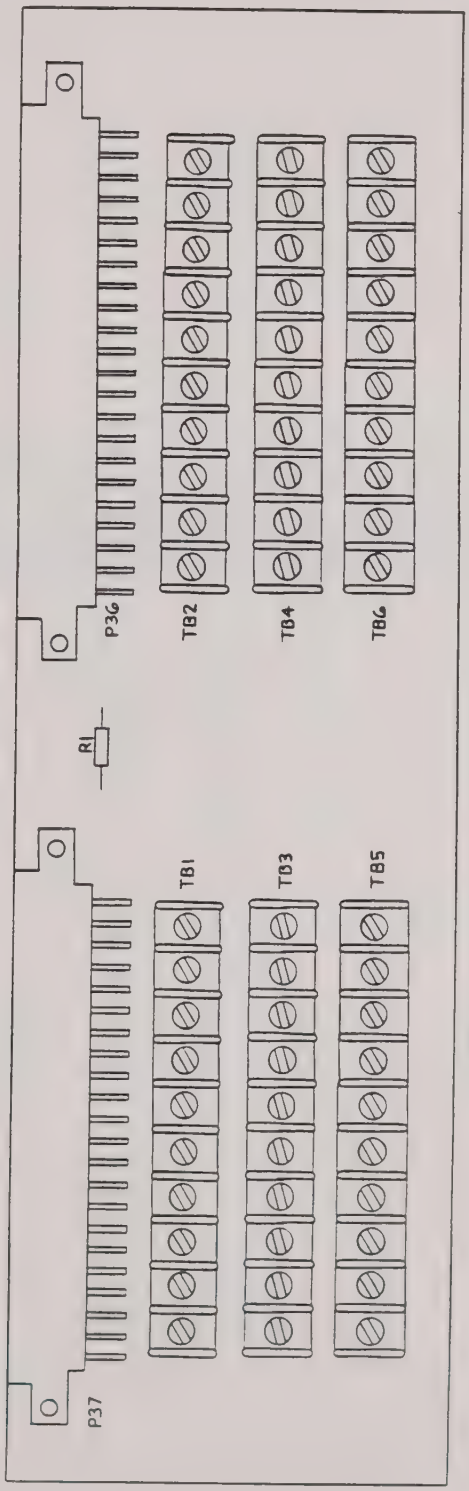
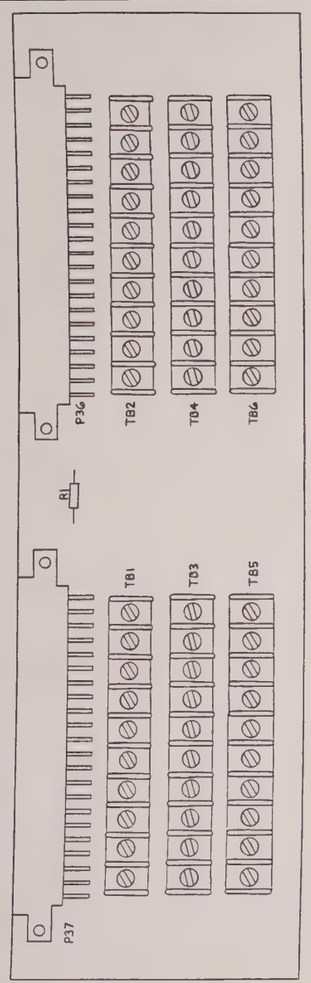


Figure 176-2. 2280A-176 Voltage Input Connector

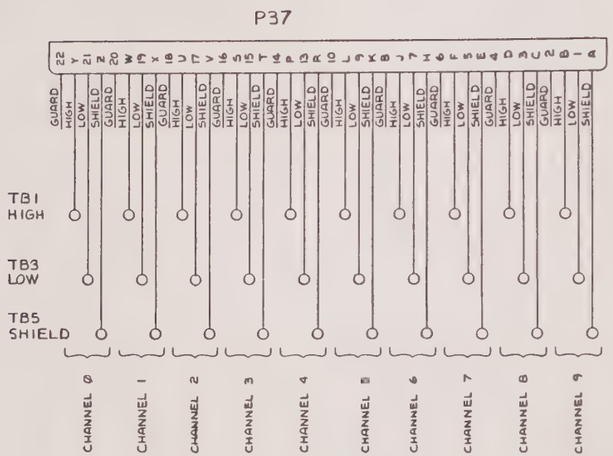


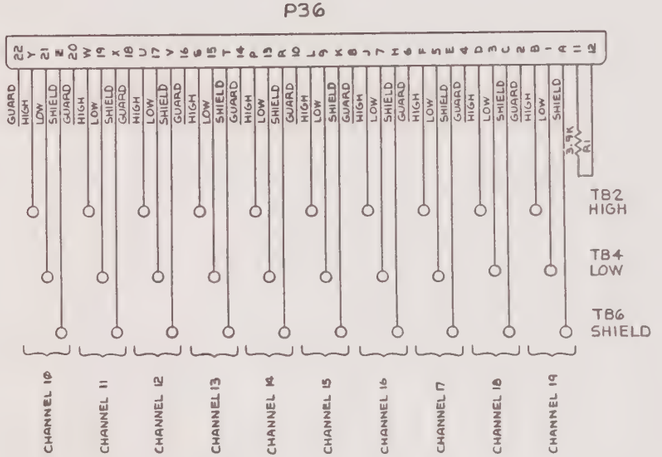
2280A-1676

Figure 176-2. 2280A-176 Voltage Input Connector (cont.)



2280A-1676





2280A-1076

Figure 176-2. Voltage Input Connector Schematic Diagram

DESCRIPTION

The 2280B-177 RTD/Resistance Connector installs on the rear of the 2280B-163 RTD/Resistance Scanner, and it provides 20 sets of input screw terminals for connection to RTDs and resistances. The connector assembly is enclosed in a plastic housing that provides protection for terminal connections and strain relief for external wiring. Retaining screws at each end of the housing fasten the assembly to the Data Logger chassis. The RTD/Resistance Connector is shown in Figure 177-1.

WHERE TO FIND FURTHER INFORMATION

The RTD/Resistance Input Connector theory of operation, performance test, general maintenance, calibration procedure, parts list, and schematic diagram are given in this subsection. Installation and system configuration instructions are located in the 2280 Series System Guide, and operating and programming instructions are located in the 2280 Series User Guide.

THEORY OF OPERATION

The RTD/Resistance Input Connector theory of operation discussion includes an overall functional description and a detailed circuit description. The schematic diagram for the Input Connector is located at the end of this option subsection.

OVERALL FUNCTIONAL DESCRIPTION

The RTD/Resistance Input Connector provides screw terminal inputs for connection to external resistances. These resistances are passed through two connectors to the 2280B-163 RTD/Resistance Scanner for conditioning.

DETAILED CIRCUIT DESCRIPTION

Twenty RTD's or other resistance sensors can be attached to the connector using five terminals per channel; HI EXC, HI, LO, LO EXC, and LO COM. Four terminals per channel are isolated from the other channels, providing for 4-wire and one 3-wire mode of operation. The fifth terminal on each channel, LO COM, is a common return for either channels 0 through 9 or 10 through 19, providing for accuracy in the other 3-wire mode of operation. The 44-pin edge connectors provide paths through which the RTD/Resistance Scanner can select, excite, and measure resistances wired to the connector terminals.

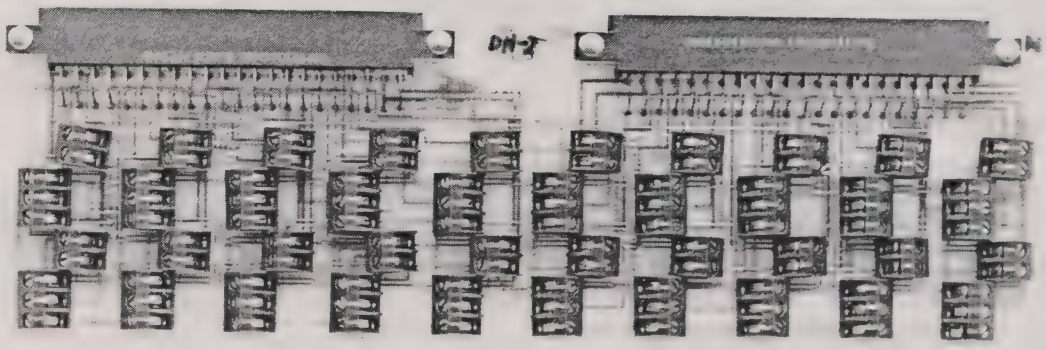


Figure 177-1. RTD/Resistance Input Connector

PERFORMANCE TEST

This Input Connector is tested along with the 2280B-163 RTD/Resistance Scanner in that scanner's subsection.

GENERAL MAINTENANCE

The Resistance Input Connector PCA normally does not require cleaning unless dirt, dust, or other contamination is visible on the surface. PCA Cleaning instructions are given in Section 4 of this manual.

CALIBRATION

The RTD/Resistance Input Connector does not require calibration.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the RTD/Resistance Input Connector is given in Table 177-1. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the RTD/Resistance Input Connector is given in Figure 177-2.

TABLE 177-1. 2280B-177 RTD/RESISTANCE INPUT CONNECTOR
(SEE FIGURE 177-2.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
H 1		STEEL,CAD.PLATED,.125X .500	276493	89536	276493	4		
H 2		WASHER,FLAT,STEEL,#4,0.030 THK	147728	89536	147728	4		
MP 1		CONNECTOR HOUSING, TOP	578971	89536	578971	1		
MP 2		CONNECTOR HOUSING, BOTTOM	656876	89536	656876	1		
MP 3		DECAL,RTD/OHMS INPUT CONN.	748038	89536	748038	1		
MP 4		DECAL, OPTION -177	748020	89536	748020	1		
MP 5		TAPE,FOAM,PVC,1/4W,3/8 THK	603134	89536	603134	2		
P 39, 40		CONN,PWB EDGE,REC,90,0.156 CTR,44 POS	614313	89536	614313	2		
TB 1- 10, 21- TB 30		TERM STRIP,PWB,ANGL ENTRY,2 CONTACTS	478867 478867	89536	478867	20		
TB 11- 20, 31- TB 40		TERM STRIP,PWB,ANGL ENTRY,3 CONTACTS	474221 474221	89536	474221	20		

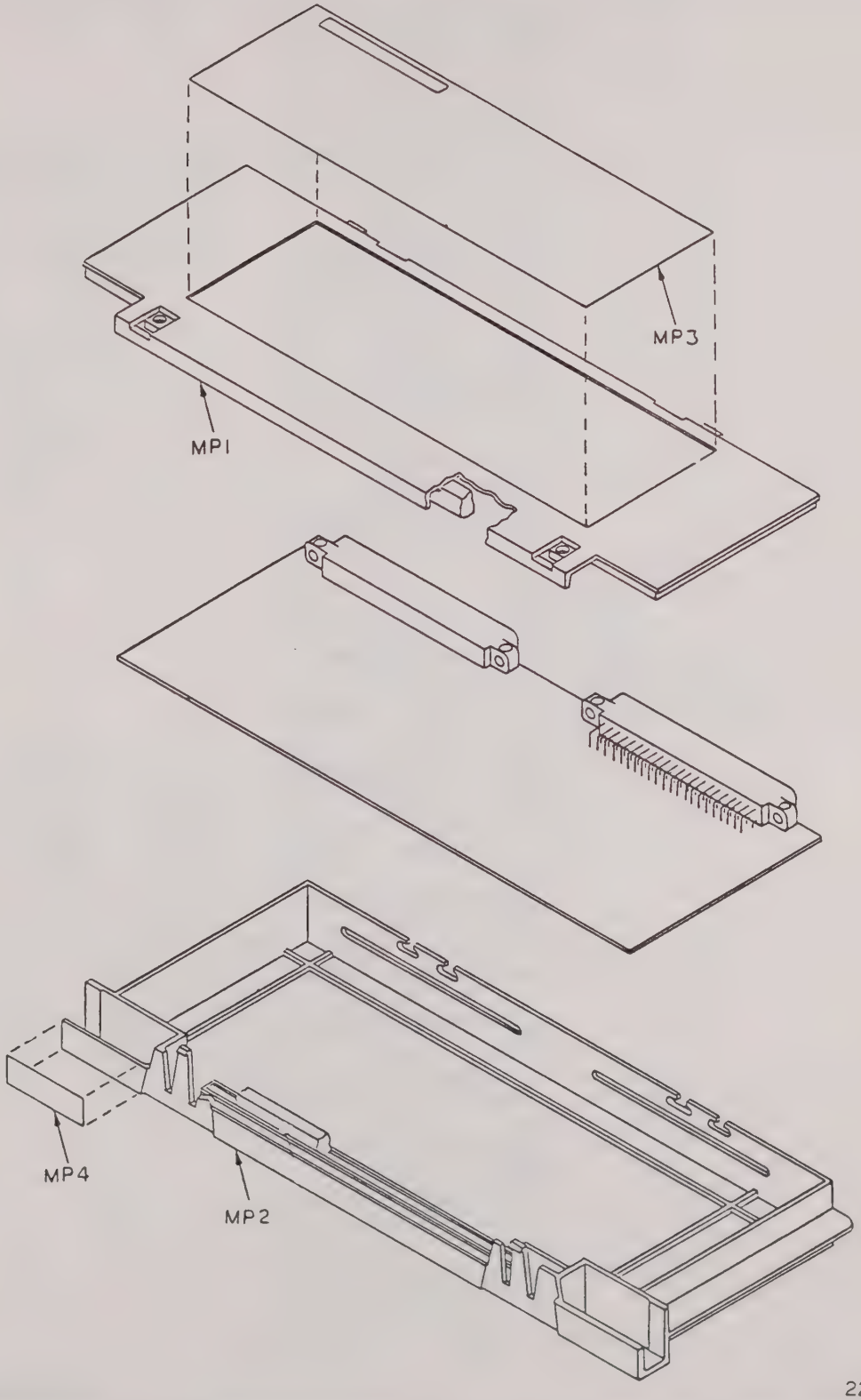
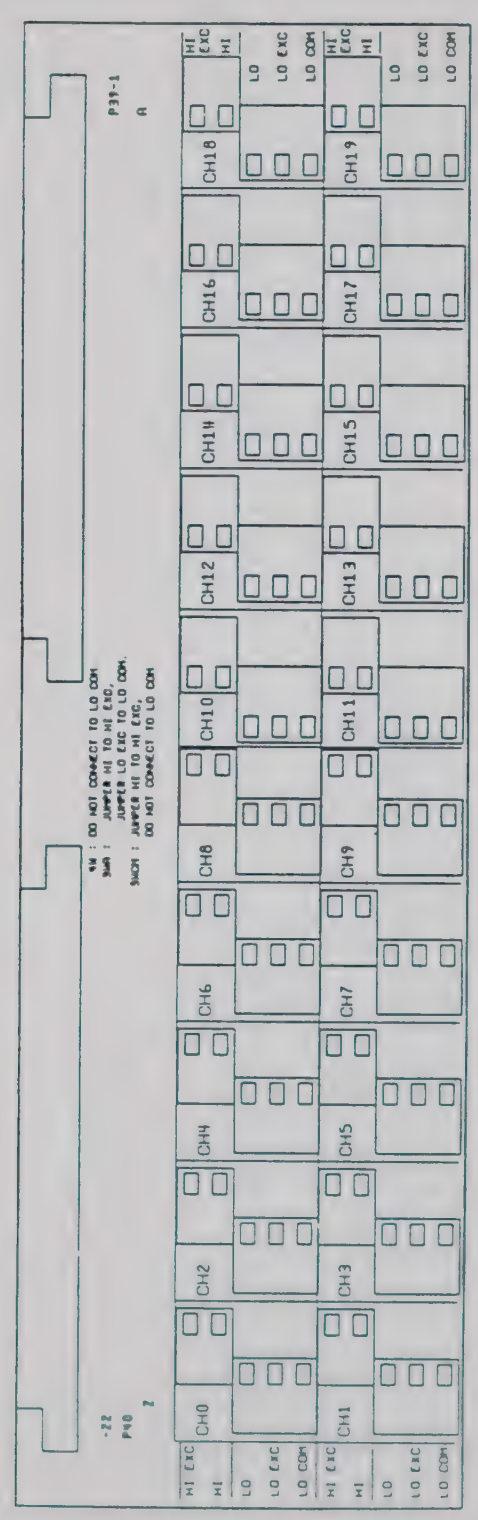
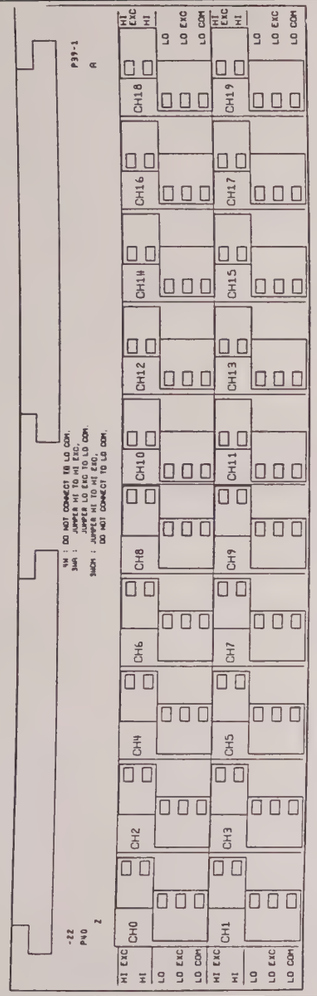


Figure 177-2. 2280B-177 RTD/Resistance Input Connector

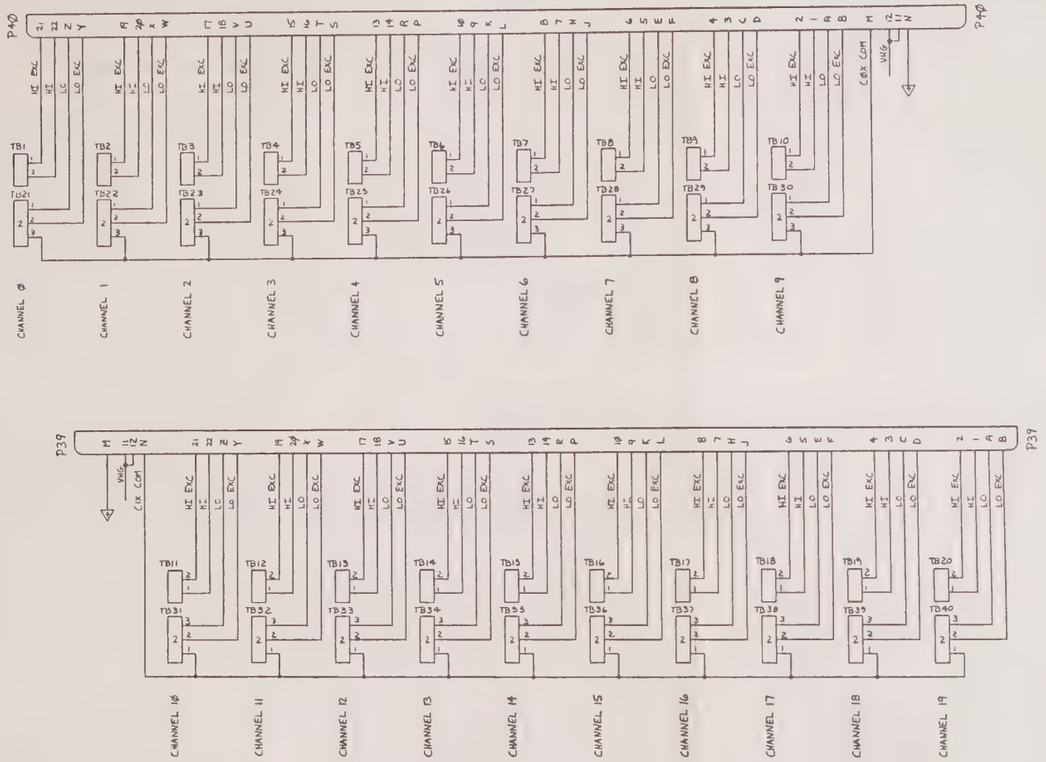


2280B-1677

Figure 177-2. 2280B-177 RTD/Resistance Input Connector (cont.)



2280B-1677



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL GRAPHIC SYMBOLS ARE IN ACCORDANCE WITH ANSI Y32.2 AND Y32.14.

2280B-1077

Figure 177-2. RTD/Resistance Connector Schematic Diagram

Option 2280A-179
Digital/Status Input Connector

DESCRIPTION

The Option 2280A-179 Digital/Status Input Connector connects to the Digital I/O Board (Option 2280A-168). The connector provides screw-terminal connections that allow input of BCD digital data, binary digital data, or status input information to the 2280 Series Data Logger.

WHERE TO FIND FURTHER INFORMATION

In this subsection are Digital/Status Input Connector theory of operation, general maintenance, a parts list, and a schematic diagram. Installation and system configuration instructions are in the 2280 Series System Guide, and operating and programming instructions are in the 2280 Series User Guide. Option specifications are in the Appendix in this manual and in the System Guide.

THEORY OF OPERATION

The Digital/Status Input Connector provides a path from screw terminals on the connector body to the card-edge connector pins on the Digital I/O Board. There is no circuitry on the connector PCA other than printed traces. The 2280 Series System Guide gives instructions for connector configuration.

When configured for status input, the Digital/Status Input Connector allows the Digital I/O Board to accept a maximum of 20 separate one-bit inputs from an external source for each Digital I/O Board installed in either the 2280 Mainframe or the 2281A Extender Chassis. Each bit is associated with a channel programmed as status input.

When configured for digital input, the Digital/Status Input Connector allows the Digital I/O Board to accept 20 bits of parallel digital data from an external source. This data is received at the channel address set on the associated Digital I/O Board.

GENERAL MAINTENANCE

The Digital/Status Input Connector PCA normally does not require cleaning, but if dirt, dust, or other contamination is visible on the surface, the PCA should be cleaned. Follow PCA cleaning instructions in Section 4 of this manual.

PERFORMANCE TESTS

There is no separate performance test for the Digital/Status Input Connector since the connector is tested with the Digital Input Board in that option's performance test (see subsection for Option 2280A-168).

CALIBRATION

There are no calibration adjustments for the Digital/Status Input Connector.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the Digital/Status Input Connector is given in Table 179-1. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the Transducer Excitation Connector is given in Figure 179-1.

TABLE 179-1. 2280A-179 DIGITAL/STATUS INPUT CONNECTOR
(SEE FIGURE 179-1.)

REFERENCE DESIGNATOR A->NUMERICS---)	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
H 1		STEEL,CAD.PLATED,.125X .500	276493	89536	276493	2		
H 2		WASHER,FLAT,STEEL,#4,0.030 THK	147728	89536	147728	2		
MP 1		CONNECTOR HOUSING, TOP	578971	89536	578971	1		
MP 2		CONNECTOR HOUSING, BOTTOM	656876	89536	656876	1		
MP 3		DECAL,DIGITAL/STATUS INPUT CONN.	634626	89536	634626	1		
MP 4		DECAL, OPTION -179	634550	89536	634550	1		
MP 5		TAPE,FOAM,PVC,1/4W,3/8 THK	603134	89536	603134	2		
P 43		CONN,PWB EDGE,REC,90,0.156 CTR,44 POS	614313	89536	614313	1		
TB 1- 6		SINGLE ROW, .325 CENTERS, 12 POSITION	615690	89536	615690	6		

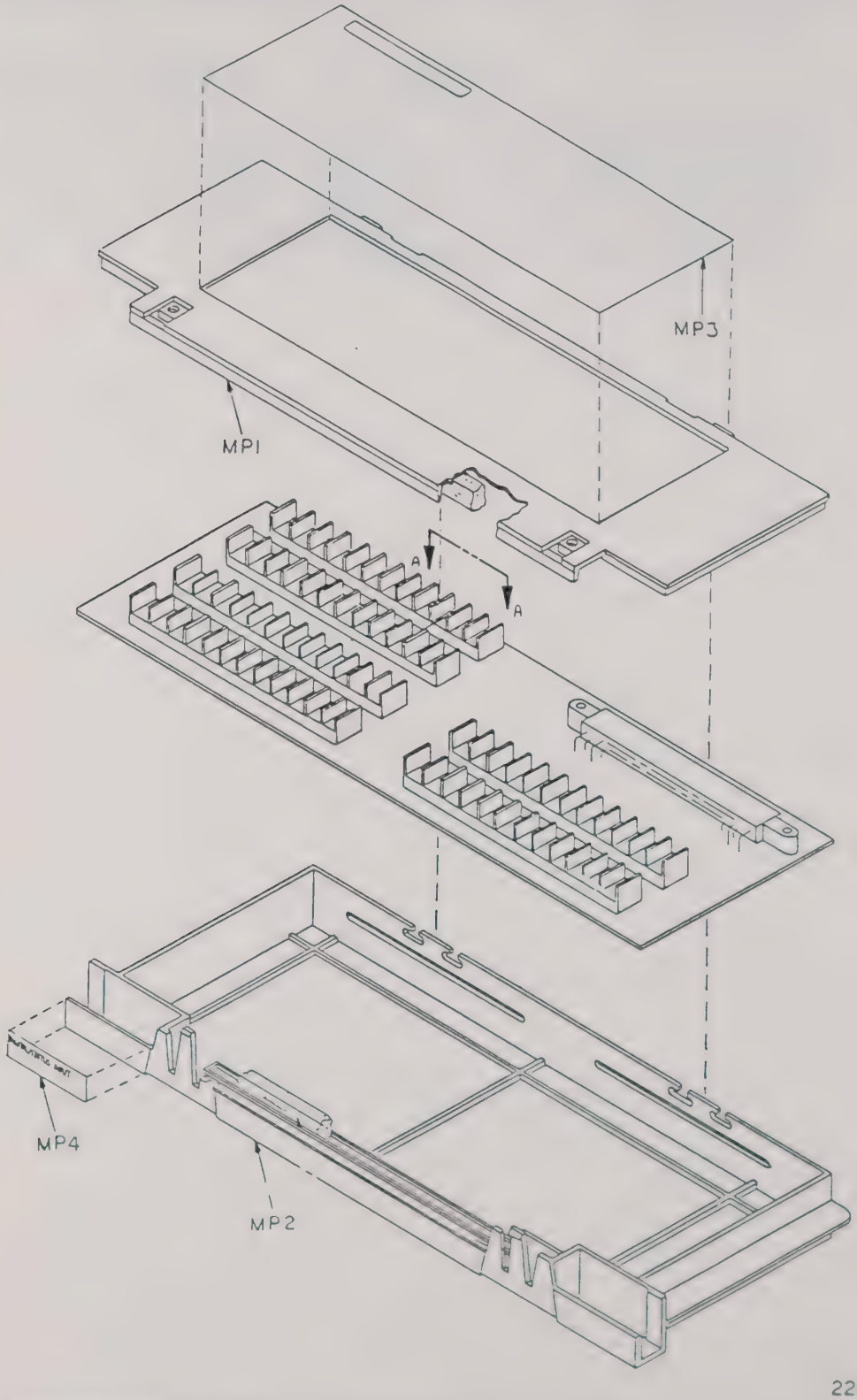
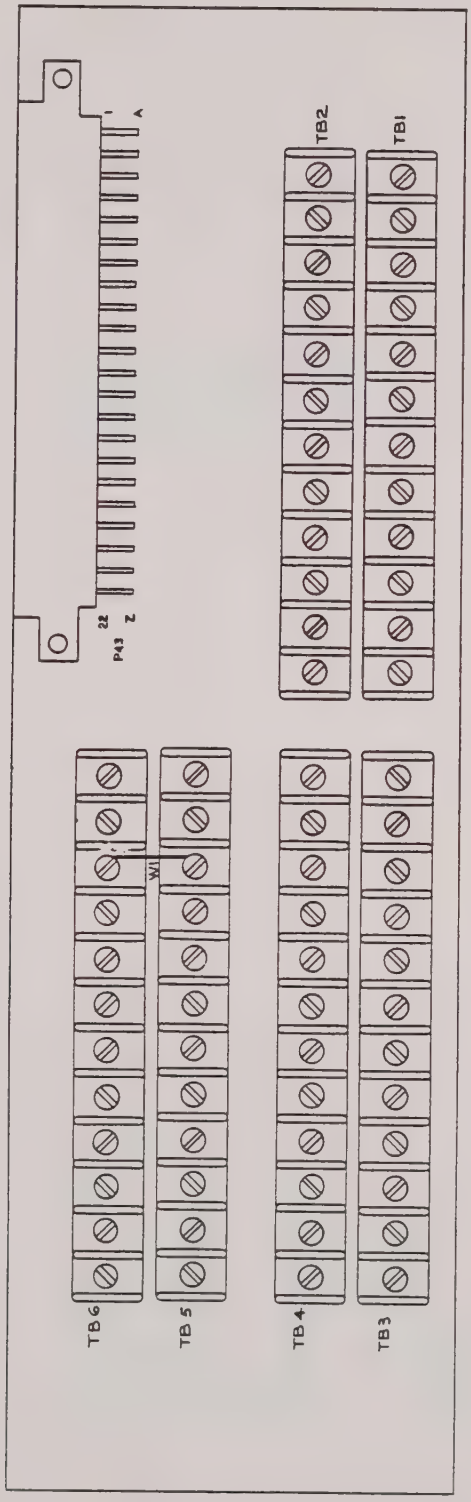
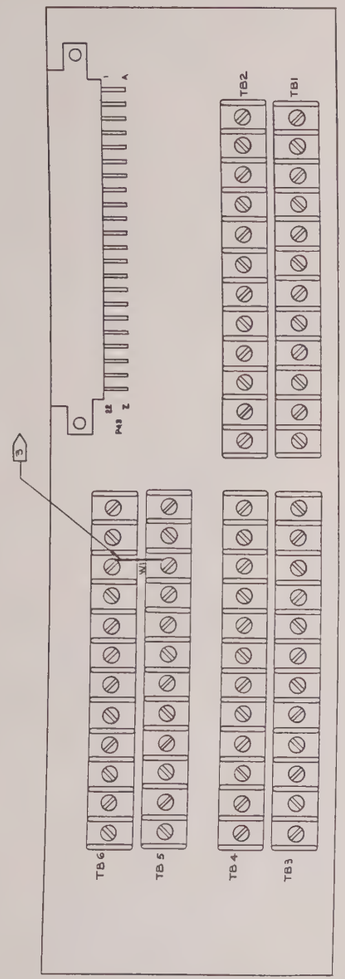


Figure 179-1. 2280A-179 Digital/Status Input Connector

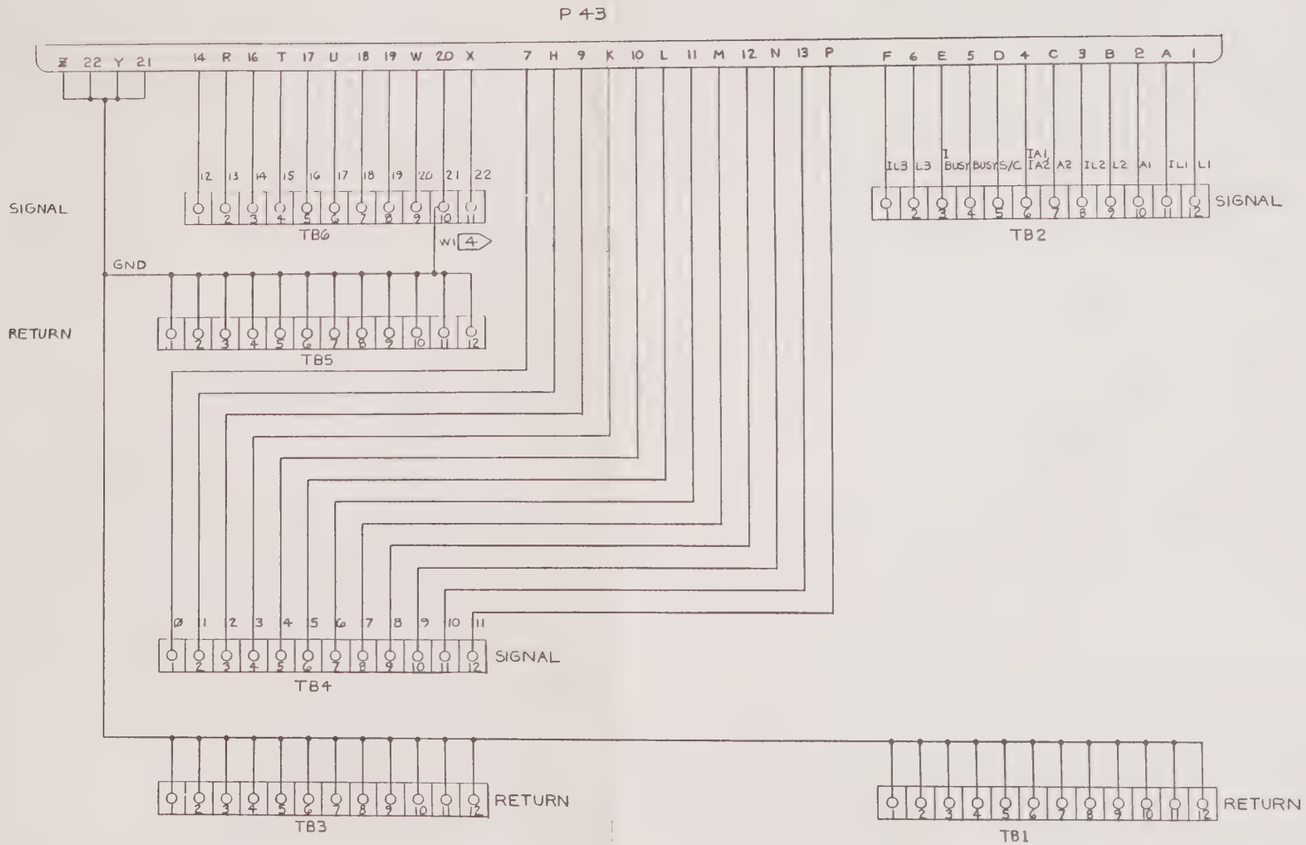


2280A-1679

Figure 179-1. 2280A-179 Digital/Status Input Connector (cont.)



2280A-1679



2280A-1079

Figure 179-2. Digital/Status Input Connector Schematic Diagram

SECTION 10

OPTIONS -200 AND ABOVE

CONTENTS

Option 2280A-211 Advanced Math Processor 211-1
Option 2280A-214 DC-100 Cartridge Tape Drive 214-1
Option 2280A-341 RS-232-C Interface 341-1
Option 2280A-342 IEEE-488 Interface 342-1

Option 2280A-211
Advanced Math Processor

DESCRIPTION

The Advanced Math option is a circuit board assembly that plugs into connector J4 on the 2280 Series Data Logger motherboard to provide the 2280 with enhanced mathematical capabilities. Calculations not possible using the 2280 Series alone can be performed by a 2280 with an Advanced Math option installed, because of the option's associated arithmetic processing unit.

Added mathematical functions are not the only features of the Advanced Math option. Calculations that can be done by the 2280B without an Advanced Math Option (thermocouple linearization, for example) are performed more rapidly by the Data Logger when an Advanced Math Option is installed.

WHERE TO FIND FURTHER INFORMATION

In this subsection are Advanced Math Processor theory of operation, general maintenance, performance tests, calibration procedure, a parts list, and a schematic diagram. Installation and system configuration instructions are in the 2280 Series System Guide, and operating and programming instructions are in the 2280 Series User Guide. Option specifications are in the Appendices in this manual and the 2280 Series System Guide.

No test equipment is required to perform the procedures given in this section. A summary of test equipment required for all procedures in this manual is given in Table 1-1 in Section 1 of this manual.

NOT AVAILABLE AT THIS PRINTING

Figure 211-1. Advanced Math Processor

THEORY OF OPERATION

The Advanced Math Option theory of operation includes an overall functional description, a block diagram analysis, and a detailed circuit analysis which describes each major circuit block. A block diagram is included with the text, and full schematic diagrams are located at the end of this option subsection.

Overall Functional Description

The 2280A-211 Advanced Math Option greatly increases Data Logger capability by providing additional math functions and reducing computation demands placed on the Controller Assembly.

Since they both handle the same data, the Controller and the Advanced Math assemblies communicate directly, and share a section of memory located on the Data Logger Memory Assembly. A math interface buffer, the instrument program data base, and the scan buffer which contains readings and flags for each scanned channel are located on the Data Logger Memory Assembly.

Two processors on the Advanced Math board implement the many available functions. A central processing unit (CPU) handles data manipulation, routing, and control, while an arithmetic processing unit (APU) crunches the numbers.

Other circuitry supports the two processors. This includes on board memory, tri-state bus buffers, a memory arbitration circuit, a test LED circuit, a 12 volt supply, and combinational logic, buffers, and decoders.

Block Diagram Analysis

The Advanced Math Assembly is shown in block diagram form in Figure 211-2. The following paragraphs discuss the function of each of the diagram blocks.

o Central Processing Unit (CPU)

The main processor on the advanced Advanced Math Option, a Z80 microprocessor, communicates with the Controller, controls the arithmetic processor IC, checks entered mathematical expressions, and handles all general mathematical data flow.

o Arithmetic Processing Unit (APU)

The arithmetic processing unit is an integrated circuit that performs the actual mathematical calculations. Its speed and power enable it to quickly perform complex trigonometric and standard mathematical operations.

o On Board Memory

This block includes all resident random access memory (RAM) and read only memory (ROM) needed to perform Math Assembly functions. 28k-bytes of ROM hold the programming used by the CPU, and 4k-bytes of RAM is used as scratch pad.

o Memory Arbitration Circuit

This circuit is centered around an asynchronous state-machine controller which looks at several logic control lines to determine whether the Controller Assembly or the Advanced Math Assembly should have access to shared, non-volatile RAM resident on the Memory Assembly. Other memory arbitration and wait generation circuits are also included in this block.

o Test LED Circuitry

A seven-segment LED located at the lower, front corner of the Math Assembly indicates the status and results of circuit self tests. Different segments of the LED will light when specific circuit sections fail.

o 12 Volt Supply

This supply generates +12 volts dc from a +24 volt dc input, referencing the output to GND 1, the +5 volt return.

o Bus Buffers

The tri-state bus buffers provide drive capability for the address bus lines as they leave the Math Assembly, and enable and provide drive for the data bus lines as they leave.

o Decode, Combinational Logic, and Buffer Circuitry

These three small blocks represent circuitry components that buffer input lines, generate control signals, and decode addresses for use by the other circuit blocks.

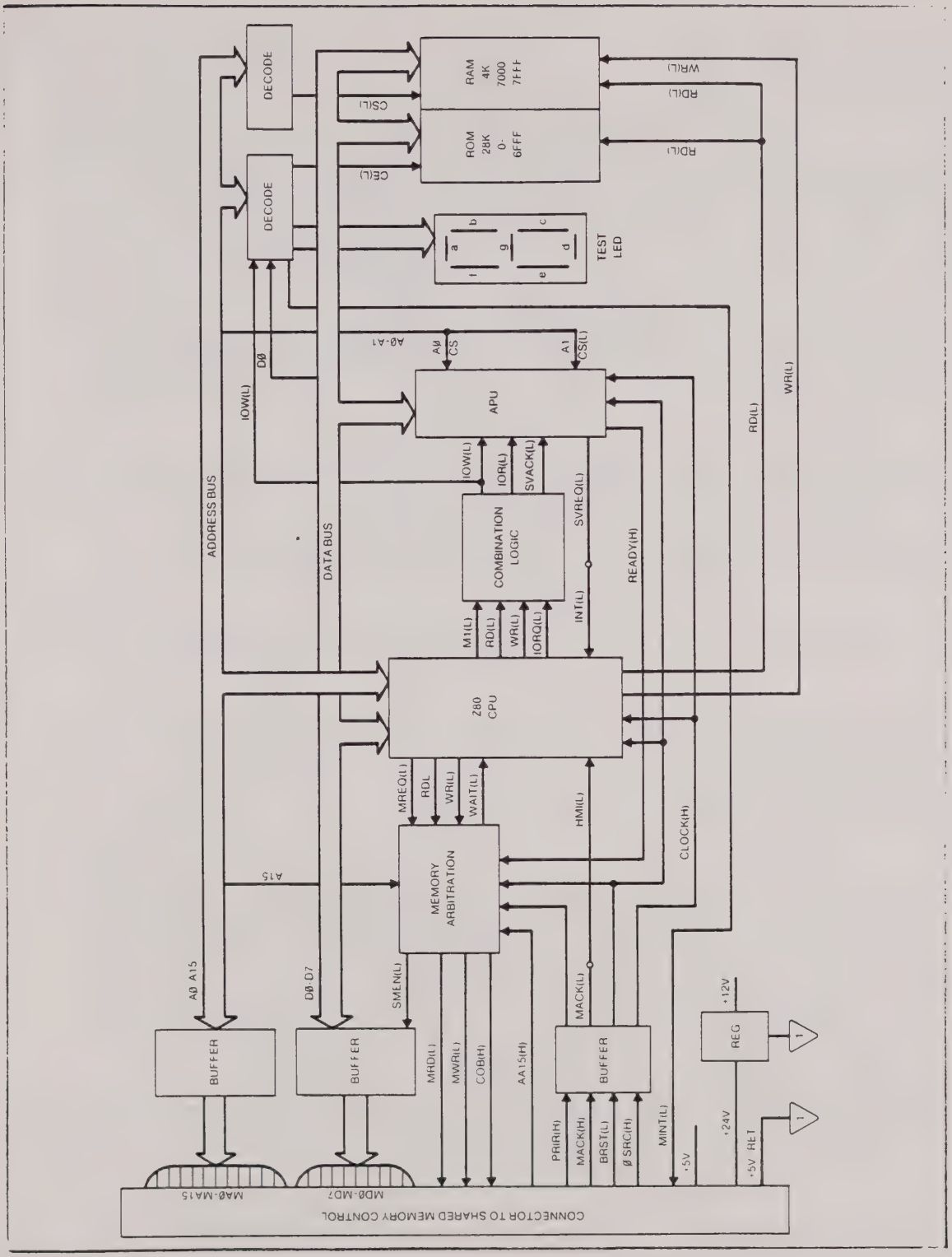


Figure 211-2. Advanced Math Block Diagram

Detailed Circuit Analysis

CENTRAL PROCESSING UNIT (CPU)

The central processing unit is a Z80 micro-processor, U13, which fetches raw data and expressions, and controls data flow between the Controller and the arithmetic processing unit. This allows computation of mathematical expressions that can have a maximum of 80 characters and manipulate raw data measurements and previously computed results. Stored expressions that have been previously checked are used by the CPU to sequence the APU through an evaluation of the data.

Communication between the Controller and the Advanced Math Assembly is coordinated through flags and interrupts. The Controller Assembly initiates a computation by placing a raw reading in the scan buffer and activating flags in the math interface buffer located in shared memory.

After reading the active flags, the Math CPU obtains channel equation or linearization information from the instrument program data base. The CPU uses the information to coordinate data and equation routing to and from the arithmetic processing unit. While waiting for SVREQ(H), a service request interrupt which drives U22 and thereby the Z80 INT(L) line, the CPU organizes information for processing the next reading.

When a computation is completed, the CPU obtains the result, checks for limit violations, and returns it to shared memory along with appropriate flags.

Next, the Controller Assembly is told that the task has been completed when the MINT(L) interrupt line is driven low by the Q0 output of 8-bit addressable latch U27. This interrupt is asserted by the CPU when it performs an I/O write to the proper location, and U20 and U21 combine IORQ(L), WR(L), and A1(L) to enable latch U27 with data bus line D0 set high.

When the Controller Assembly recognizes the MINT interrupt, it asserts the interrupt acknowledge line, MACK(H). This is inverted by U19 and applied to the NMI(L) line of the Advanced Math Option CPU, causing the CPU to de-assert MINT(L) to a high state. To complete the handshake operation, the Controller de-asserts MACK to a low state.

Setting flags and placing calculation results in shared memory is always controlled by the memory arbitration circuit.

A more comprehensive discussion of Z80 microprocessor operation and timing relationships is given in the Controller Assembly theory of operation.

ARITHMETIC PROCESSING UNIT (APU)

Integrated circuit U17 is the Arithmetic Processing Unit (APU). In addition to the four basic operations of addition, subtraction, multiplication, and division, it provides floating point square root, sine, cosine, tangent, arcsine, arccosine, arctangent, natural log, base 10 log, exponent of "e", and power of one number to another operations. Additional operations are also made possible by using the IC's internal stack to move and convert data.

Table 211-2 lists the four operations whereby the CPU controls the APU and communicates with the APU (U17). The states of the various APU control lines when it is being written to or read from are also given in the table.

Table 211-2. APU Control Line States

OPERATION	CONTROL LINES				
	RD(L)	WR(L)	C/^D(H)	CS(L)	
read status	L	H	H	L	
read data	L	H	L	L	
load command	H	L	H	L	
load operand	H	L	L	L	L < 0.4 volts
APU de-selected	X	X	X	H	H > 2.0 volts X = don't care

The status register within the APU chip can be read by the CPU and contains the following information:

- Whether the APU is busy performing an operation
- The sign of the most recent result
- Whether the last operation resulted in a carry or borrow from the most significant bit
- And whether the last calculation resulted in an error from

  Dividing by zero
  Taking the square root of a negative number
  Too large of an inverse sine, cosine or ex argument
  Calculation overflow
  Calculation underflow.

The status register is accessed when the APU is selected by CS(L) going low with C/^D(H) remaining high. Driving the RD(L) input low with U21, which AND's IORQ(L) and RD(L) from the CPU, strobes the status register contents onto the data bus. The register is then read and checked by the CPU for the APU status, or for potential errors generated by the just completed APU operation. By reading the status register in this manner, the state of the APU can be determined at any time without interrupting calculations.

Numerical data is written to the APU by the CPU in the following manner. Control lines C/^D(H) and CS(L) are driven low by the address bus signals A0 and A1 respectively, thereby selecting the APU and its 16 byte stack. The CPU then places one byte of the 4-byte operand on the data bus and drives WR(L) and IORQ(L) low to provide a write strobe to the U17 WR(L) line for one clock cycle. The WR(L) signal for one clock cycle strobs the byte onto the APU's internal stack. For a floating point operand, 4 bytes are transferred in this manner.

Once the first operand has been placed in the APU, a second may be written to it in the same manner, pushing the bytes previously on the top of the stack farther down.

Once the operand(s) is(are) on the stack, the CPU drives A0 high and A1 low to select the command register of the APU, then places the appropriate op-code for the desired mathematical operation on the data bus. The APU WR(L) line is then strobed low to store the op-code in the APU command register. Following this, the APU uses the stored operand(s) in the calculation specified by the op-code.

Upon completion of the math operation, one of the bits in the op-code flags the APU to generate a service request. In response, the APU drives SVREQ high, thereby driving the CPU INT(L) line low to generate an interrupt request. The CPU responds to the request by driving M1(L) and IORQ(L) low. These two signals are gated together in the combinational logic block by U21 to drive the APU SVACK(L) line low and cause the APU to remove its service request by de-asserting SVREQ(H) low. In this way, the APU signals the CPU that it has finished an operation, and a handshake occurs.

If the CPU requires the result of an operation, it selects the data stack of the APU by setting CS(L) and C/^D(H) low, and reads the 4 bytes of the result, one byte at a time.

The APU drives the READY(H) line low to hold off the CPU when the APU is asked for data while performing an operation or stack manipulation. This causes U15 to assert the CPU WAIT(L) input and hold the CPU in a wait state until the APU is ready to communicate.

ON BOARD MEMORY - RAM AND ROM

The Advanced Math CPU is capable of addressing up to 64K bytes of memory. 32k-bytes of this with addresses from 0000 through 7FFF is located on the Advanced Math Assembly and is reserved for Math CPU use. 28k-bytes of memory with addresses from 9000 to FFFF is non-volatile shared RAM located on the Memory Assembly. Both the 2280B controller and Advanced Math CPU may access the RAM located on the Memory Assembly.

Standard Program ROM occupies 28k-bytes of the 32k-bytes on the Math Assembly, and it contains the executable code and all linearization constants required by the Z80 Math CPU. This program memory resides in locations 0000 to 6FFF in U2, U3, U4, U5, U8, U9, and U10. ROM address decoder U14 selects a specific ROM, determined by address lines A12 to A15, by asserting the desired ROM chip CE(L) line when the MREQ(L) line is asserted low, as listed in Table 211-3.

Table 211-3. ROM Address Selection

ADDRESS LINES				SELECTED ROM	
A15	A14	A13	A12		
0	0	0	0	U8	
0	0	0	1	U2	
0	0	1	0	U3	
0	0	1	1	U4	MREQ(L) = L
0	1	0	0	U5	
0	1	0	1	U9	
0	1	1	0	U10	

The ROM's used on the Math Assembly are 2732 EPROM's. Since these have slower access times than the CPU provides for at a 4 MHz clock rate, a wait state generation circuit described in the memory arbitration block places the CPU in wait for a small fraction of the memory access cycle. If a clock rate of 2 MHz is used, or if faster 2732A EPROM's are used, the wait may be disabled by removing resistor R17 on the Advanced Math Option.

In addition to program memory, the Math Option contains 4k-bytes of RAM that can be used for scratch pad memory and for storing mathematical expression information. This RAM resides at addresses 7000 to 7FFF in U6 and U11. The RAM address decode circuit made up of U14, U16, and U19 selects the RAM chip specified by address lines A11 to A15 by asserting that IC's CS(L) line. The RAM selected by each address combination is listed in Table 211-4.

Table 211-4. RAM Address Selection

ADDRESS LINES					SELECTED RAM	
A15	A14	A13	A12	A11		
0	1	1	1	0	U11	MREQ(L) = L
0	1	1	1	1	U6	

SHARED MEMORY ARBITRATION CIRCUIT

The core of the memory arbitration circuitry is an asynchronous state machine, formed by U25 and U26, which has an output labeled AOB(L) for controller on bus. This signal is asserted when the Controller Assembly has access to shared memory, prohibiting access by the Math CPU. The Controller is granted access in the following situations:

- Only the Controller CPU is requesting shared memory.
- The Math and Controller CPU's simultaneously request shared memory and shared memory was last accessed by the Controller.
- The Controller requests shared memory and has been granted access to it. Here, the Math CPU is placed in a wait state until the Controller finishes its memory access cycle.
- The Controller asserts the priority (PRIR) signal to force the Math CPU out of shared memory. The PRIR signal will only be activated if the Math CPU fails a self-test or is not able to access shared memory.

The state machine blocks out the Controller and allows the Math Assemoly to access shared memory in the following situations:

- Only the Math CPU is requesting shared memory.
- The Math and Controller simultaneously request shared memory and shared memory was last accessed by the Math CPU.
- The Math CPU requests shared memory and has been granted access to it. Here, the Controller is placed in a wait state until the Math CPU finishes its memory access cycle.

AOB(L) grants Controller access to shared memory when it is asserted to clear the U24 synchronization flip-flop that drives the BOBDL lines and to steer the Controller address, control, and data lines into the Memory Assembly shared memory block.

Another section of circuitry made up of a flip-flop in U24, one in U23, plus gates in U15 and U26, forms a wait state generation circuit that forces the Math CPU to wait when it is accessing ROM memory. The output of this circuit is the ROMWAIT(L) signal, and the inputs are RAM(L), BA15(L), MREQ(L), and RESET(L), and the clock is CLOCK(H).

When the Math Assembly CPU is not performing a memory access, MREQ(L) is de-asserted high, Q(L) of U23 is asserted low, Q(H) of U24 is asserted high, the ROMWAIT(L) output of U26 is de-asserted high, and the CPU is not placed in a wait state.

When ROM memory is accessed, the Math Z80 asserts MREQ(L) low. The next positive edge of CLOCK, clocks the low state through U23 to de-assert Q(L) to a high level, while the Q(H) output of U24 remains asserted high. This causes U26 to assert ROMWAIT(L), thereby asserting WAIT(L) through U15, and placing the Math Assembly CPU in a wait state. On the next positive CLOCK transition, U24 clocks the low state of the U23 Q(H) output through to de-assert the U24 Q(H) signal. This results in ROMWAIT(L) being removed by U26, WAIT(L) being de-asserted by U15, and the CPU being allowed to continue.

Once the ROM access has been completed, MREQ(L) is de-asserted high. The next two positive clock edges assert the U23 Q(L) and the U24 Q(H) outputs, and ROMWAIT(L) is kept de-asserted. ROMWAIT(L) remains high until the next program memory access cycle begins.

If shared memory or on board RAM is being addressed by the Math CPU, RAM(L) or BA15(L) will be asserted, causing U15 to clear U24 Q(H) to a low level and disable the wait state generating signals. This is done since both of these memory sections are fast enough that a wait state is not needed.

If the Math board has requested access to shared memory as signaled by the asserted low SMREQ(L) line, but hasn't yet been granted access as indicated by the still de-asserted BOBDL(H) line, U20 will assert WAIT(L) through U15. This forces the Math CPU to wait until it has been granted access to shared memory before continuing.

Many signals are involved in the memory arbitration and wait state generation circuits, with each having specific meanings and functions. A description of these signals follows:

PRIR(H) Priority is asserted whenever the Controller decides to force its way into shared memory. This is only asserted to prevent a defective Advanced Math option from disrupting the contents of shared memory.

AA15(H) This is asserted by the Controller when access to shared memory is desired. This signal holds access to shared memory if it has been previously granted to the Controller.

BA15(L) This is asserted low when the Math CPU desires access to shared memory. BA15(L) is generated by U26 when A15 goes high to address the upper 32k-bytes of memory and IORQ(L) stays high to indicate that the transfer about to occur will not involve I/O. This signal holds access to shared memory if the Math CPU is still using it.

AOB(L) This is the output of the memory arbitration circuit. It is asserted low when the Controller has been granted access to shared memory and the Math Assembly is to be excluded. This remains asserted until the Math CPU is to be granted access.

AOB(H) This is the inverted and buffered memory arbitration signal that leaves the Math Assembly.

BOBDL(H) This stands for Math on bus delayed, and it is synchronously asserted when AOB(L) is de-asserted to allow the Math CPU to access shared memory. When AOB(L) is asserted to give shared memory access to the Controller, MOBDL(H) is immediately and asynchronously de-asserted low.

BOBDL(L) This signal is the inverted version of the signal above obtained from the Q(L) output of U24 instead of the Q(H) output. This signal is asserted low synchronously with the Math Board clock, and it is de-asserted high asynchronously with COB(L).

SMREQ(L) This shared memory request line is asserted low by U20 when MREQ(L) is asserted low by the Math CPU during a memory access and BA15(L) is asserted low.

SMEN(L) This is the shared memory enable signal that enables the Math data bus onto the shared memory bus. SMEN(L) is asserted low when the Advanced Math option is about to read or write to shared memory after being granted access to it.

WRDLY(L) This write strobe delayed signal is generated by U20 as a result of WR(L) and SMEN(L) both being asserted low. This strobe allows the address lines to settle before data is written to shared memory.

TEST LED CIRCUITRY

The seven-segment LED display which signals the error status of the board, is driven by 8-bit addressable latch U27. Upon power-up, this addressable latch is cleared so that the outputs go low to turn on all seven display segments. After each local power up test is successfully completed by the Math CPU, a specific I/O location between 000B and 001F is addressed to turn off a segment, as listed in Figure 211-3.

ADDRESS	DISPLAY SEGMENT	
		A
001F	A	-----
001B	B	F| |B
0017	E	| G |
0013	D	-----
000F	E	E| |C
000B	F	| D |
0007	G	-----

Figure 211-3. Math Board Test LED Segments

When the CPU performs an I/O write to one of the addresses in Figure 211-3, IORQ(L) and WR(L) both go low with A1 left high. This keeps the APU de-selected while U27 is enabled by U20, allowing data present on lines A2 through A4 to select or de-select decoder outputs, thereby turning the individual LED segments on or off.

All segments of the test LED status indicator are illuminated at power up and individually extinguished upon the successful completion of each self-test executed after power is applied. After power-up, any segments remaining iluminated will indicate the areas of failure.

Segment A is the first LED indicator turned off by the mathboard processor after power-up. If the indicator remains illuminated, the mathboard processor is not operating properly, that is, it cannot successfully access the ROM, RAM, and the test status indicator latch.

Segment B is extinguished when the processor successfully completes the ROM checksum test. If the segment remains illuminated, the ROM contents have been determined to be incorrect.

Segment C is turned off when the RAM test is successfully completed.

Segment D is turned off when the mathboard processor determines that it can properly access the memory shared with the controller assembly's processor.

Segment E is extinguished when the mathboard determines (by reading information contained in shared memory) that its software version is compatible with the mainframe software version.

Segment F is turned off when the test of the arithmetic processing LSI (APU) is successfully completed. If the indicator remains on, the APU chip is faulty.

Segment G is turned off when the mathboard processor determines that it can interrupt the controller assembly's processor.

12 VOLT SUPPLY

This circuit is centered around linear regulator VR1 and generates a +12 volt dc output from the +24 volt dc mainframe input. The output, which powers the APU, is referenced to the 5 volt return so that logic level inputs to the APU will be interpreted properly. Capacitors C2 and C3 provide stability and high frequency filtering for the output.

BUS BUFFERS

The tri-state bus buffer IC's drive the memory and address lines that leave the Math Assembly to drive onto, or to receive information from, the shared memory section located on the Memory Assembly. U1 is a bi-directional data bus buffer enabled by the SMEN(L) line, while U7, U12, and U18 are the always-enabled memory address buffers that drive all 16 address lines plus the MRD(L) and MWR(L) lines.

BUFFER, COMBINATIONAL LOGIC, AND DECODE CIRCUITRY

One portion of the buffer section made up of a flip-flop in U23, R16A, U22, Q1, and associated circuitry forms a divide by two and CLOCK drive circuit. The divide by two function is not used unless the 2MHz clock frequency is desired and R16A has been installed. The normal clock rate selected by R16B is 4 MHz, and this signal is buffered by U19, U22, and Q1.

Another portion of the buffer section is formed by the Schmidt-trigger inverters in U19 which sharpen up the edges of, and buffer, the signals entering the Math Assembly from other assemblies. Some of the signals treated include BRST(L), PRIR(H), and MACK(H).

The combinational block is made up of circuitry that has been described in more detail in previous circuit sections, and includes gates in U20, U21, U16, and U22. An example is the gate in U21 which AND's WR(L) and IORQ(L) to generate the block diagram IOW(L) signal which drives U17 and one gate in U20.

Decode circuitry has also been mentioned in previous sections, and is made up of U14 and U27 which are both 8-output decoders, and U16.

GENERAL MAINTENANCE

The Advanced Math Processor PCA normally does not require cleaning, but if dirt, dust, or other contamination is visible on the surface, the PCA should be cleaned. Follow PCA cleaning instructions in Section 4 of this manual.

PERFORMANCE TESTS

Entering And Running System Tests

1. Enter the System Test Menu from the Main Menu by pressing the "S" key. The Data Logger acknowledges with the prompt:

   <S> SYSTEM DIAGNOSTICS

2. Press the ENTER key. The prompt becomes:

   S: DEVICE TO TEST <1-7>? 1

   Now, the system is ready for you to choose a test from the System Test Menu. The seven system tests as they are shown on the Data Logger display are:

   S<1> CONTROLLER AND MEMORY
   S<2> KEYBOARD AND DISPLAY
   S<3> PORT A
   S<4> PORT B
   S<5> CARTRIDGE TAPE
   S<6> ADVANCED MATH PROCESSOR
   S<7> SERIAL LINK

3. Select the Advanced Math Processor test by pressing the 6, followed by the ENTER key. Several test functions can be performed on the Advanced Math Processor. The prompt becomes:

   TEST <1-n>? 1

4. Select, by number, a particular test to be performed. When the selection has been made and ENTER is pressed, the prompt TEST IN PROGRESS is displayed. The test results are then displayed on the front panel, indicating that either the test was successful (TEST PASSED) or that it has failed (TEST FAILED). Some tests also provide other helpful prompts. To step through and acknowledge these results, press EXIT successively to view each test result response until there are no more. Press EXIT twice to return to the system test menu and obtain the following prompt:

   S: DEVICE TO TEST <1-7>? _

5. When all desired tests are completed, press the EXIT key. The Data Logger will execute a power-on sequence and return to the Main Menu.

The following tests may be run after selecting the Advanced Math Assembly test (selection 6) from the test menu:

S<6> Advanced Math Processor

<1> ITEMS FAILED AT POWER UP

This displays the errors encountered during the math board power-up self tests. Possible errors are:

MATH BOARD INTERFACE FAILED
INCOMPATIBLE MATH BOARD SOFTWARE
MATH BOARD ROM CHECKSUM TEST FAILED
MATH BOARD RAM TEST FAILED
MATH BOARD APU TEST FAILED
MATH BOARD DOES NOT RESPOND

<2> ROM CHECKSUM TEST

This checks each ROM on the Math Board to see if the information stored in it is still correct. If the information has changed, the following error message is displayed:

Unn ROM CHECKSUM TEST FAILED

(Where Unn is the reference designation of the faulty part).

<3> MATH BOARD RAM TEST

This ensures that the Math Board RAM is completely functional by performing a sequential read after write at every RAM location.

4> FULL RAM TEST (destroys the configuration programming)

This checks the RAM for proper internal and external read, write, and address decoding by performing sequential write and reads at every RAM location. If any RAM location fails, the following failure message is displayed:

AUnn RAM TEST FAILED

(Where A indicates the Advanced Math Assembly, and Unn indicates the reference designation of the failed RAM).

5> SIMPLE APU (Advanced Math Processor) TEST

This causes the math board CPU to run some simple mathematical tests on the math processor.

‹6› COMPLEX APU (Advanced Math Processor) TEST

The Math Board CPU runs a full functional test on the math processor.

CALIBRATION

The Advanced Math Assebmly does not require calibration.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the Advanced Math Processor is given in Table 211-5. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the Advanced Math Processor is given in Figure 211-4.

TABLE 211-5. 2280A-211 ADVANCED MATH PROCESSOR PCA
(SEE FIGURE 211-4.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q
C 1- 3, 5-		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	30	
C 31			519157				
C 4		CAP,MICA,33PF,+-5%,500V	160317	02799	DM15E330J	1	
DS 1	*	DIODE,LED,RED 7 SEGMENT,ALPHA NUMERIC	472944	28480	QDSP3016	1	
H 1		STUD,THREADED,PENN KFH,6-32,.250	493833	89536	493833	1	
H 2		SCREW,THD CUT,PHP,STL,6-32X5/16	268037	89536	268037	2	
H 3		WASHER,FLAT,STEEL,#8,0.031 THK	110288	89536	110288	2	
H 4		WASHER,LOCK,SPLIT,STEEL,#6	110692	89536	110692	1	
H 5		NUT,HEX,MINI,S.STL,6-32	110569	89536	110569	1	
H 6		SCREW,MACH,PHP,STL,4-40X3/16	129882	89536	129882	2	
H 7		WASHER,LOCK,SPLIT,S STEEL,#4	147603	89536	147603	2	
MP 1		EJECTOR,RETAINER	488346	89536	488346	2	
MP 2		SPACER,SWAGED,RND,BRASS,4-40X0.070	343996	89536	343996	2	
MP 3		BAG,SHIELDING,TRANSPARENT,8"X12"	680942	89536	680942	1	
MP 4		HEATSINK	648402	89536	648402	1	
Q 1	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	195974	64713	2N3906	1	1
R 1, 5- 8,		RES,CF,22K,+-5%,0.25W	348870	80031	CR251-4-5P22K	11	
R 10- 13, 15,			348870				
R 19			348870				
R 2		RES,CF,1.2K,+-5%,0.25W	441378	80031	CR251-4-5P1K2	1	
R 3		RES,CF,220,+-5%,0.25W	342626	80031	CR251-4-5P220E	1	
R 4		RES,CF,22,+-5%,0.25W	381145	80031	CR251-4-5P22E	1	
R 16- 18		RES,CF,1,+-5%,0.25W	357665	80031	CR251-4-5P1E	3	
TP 1, 10, 12,		TURRET,MINI HOLLOW LUG #2010B-1	179283	88245	2010B-5	15	1
TP 50, 53, 54,			179283				
TP 70- 78			179283				
U 1	*	IC,LSTTL,OCTL BUS TRNSCVR W/3-ST OUT	477406	01295	SN74LS245N	1	1
U 2- 5, 8-		IC,4K X 8 EPROM (PROGRAMMED)	718387	89536	718387	7	
U 10			718387				
U 6- 11		IC,2K X 8 STAT RAM	584144	89536	584144	2	
U 7, 12, 18	*	IC,LSTTL,HEX BUFFER W/3-STATE OUTPUT	536458	01295	SN74LS365N	3	1
U 13		IC,NMOS,8 BIT MICROCOMPUTER	478073	89536	478073	1	
U 14	*	IC,LSTTL,3-8 LINE DCDR W/ENABLE	407585	01295	SN74LS138N	1	1
U 15	*	IC,LSTTL,TRIPLE 3 INPUT AND GATE	393082	04713	SN74LS11N	1	1
U 16, 20, 21	*	IC,LSTTL,QUAD 2 INPUT OR GATE	393108	01295	SN74LS32N	3	1
U 17		IC,NMOS,ARITHMETIC PROCESSING UNIT	584151	89536	584151	1	
U 19	*	IC,LSTTL,HEX INVERTER W/SCHMT TRIG	483180	01295	SN74LS14N	1	1
U 22	*	IC,FTTL,HEX INVERTER	634444	07235	74F04PC	1	1
U 23	*	IC,STTL,DUAL D F/F,+EDG TRG,W/SET&CLR	418269	01295	SN74S74N	1	1
U 24	*	IC,LSTTL,DUAL D F/F,+EDG TRG,W/CLR	393124	01295	SN74LS74N	1	1
U 25	*	IC,LSTTL,4 WIDE 2 IN AND-OR-INVT GATE	504662	01295	SN74LS54N	1	1
U 26	*	IC,LSTTL,QUAD 2 INPUT NAND GATE	393033	01295	SN74LS00N	1	1
U 27	*	IC,LSTTL,8BIT ADDRSABLE LATCH,W/CLR	419242	01295	SN74LS259N	1	1
VR 1	*	IC,VOLT REG,FIXED,+12 VOLTS,1.5 AMPS	413195	04713	MC7812TP	1	1
XU 2- 6, 8-		SOCKET,DIP,0.100 CTR,24 PIN	376236	91506	324-AG39D	9	
XU 11			376236				
XU 13		SOCKET,DIP,0.100 CTR,40 PIN	429282	09922	DILB40P-108	1	
XU 17		SOCKET,SIP,0.100 CTR,12 PIN	478610	00779	583773-4	2	
Z 1- 4		RES,NET,SIP,8 PIN,7 RES,22K,+-2%	500041	89536	500041	4	
Z 5		RES,NET,DIP,14 PIN,7 RES,220,+-5%	423426	89536	423426	1	

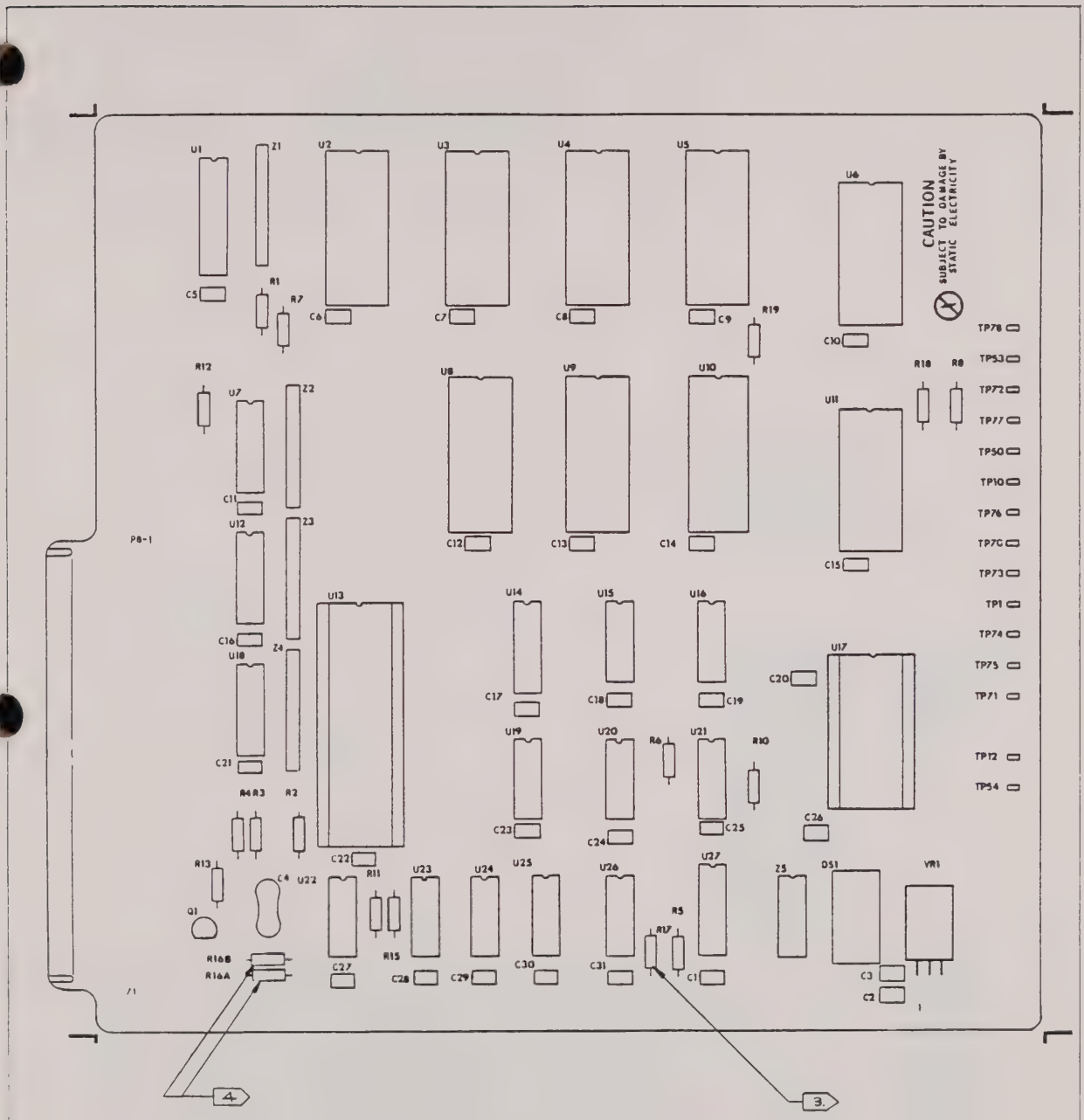
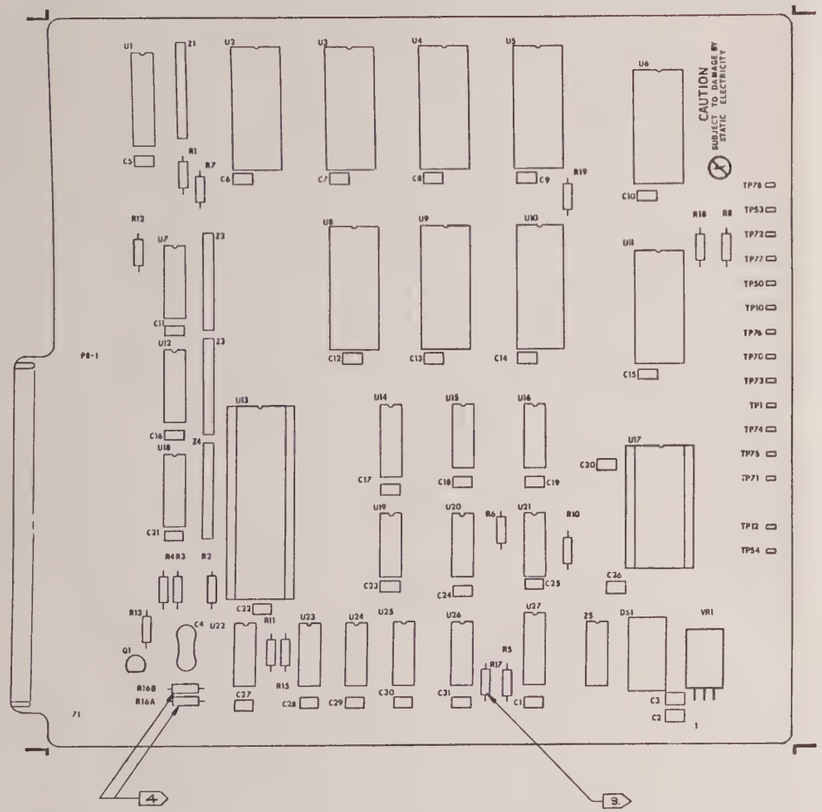
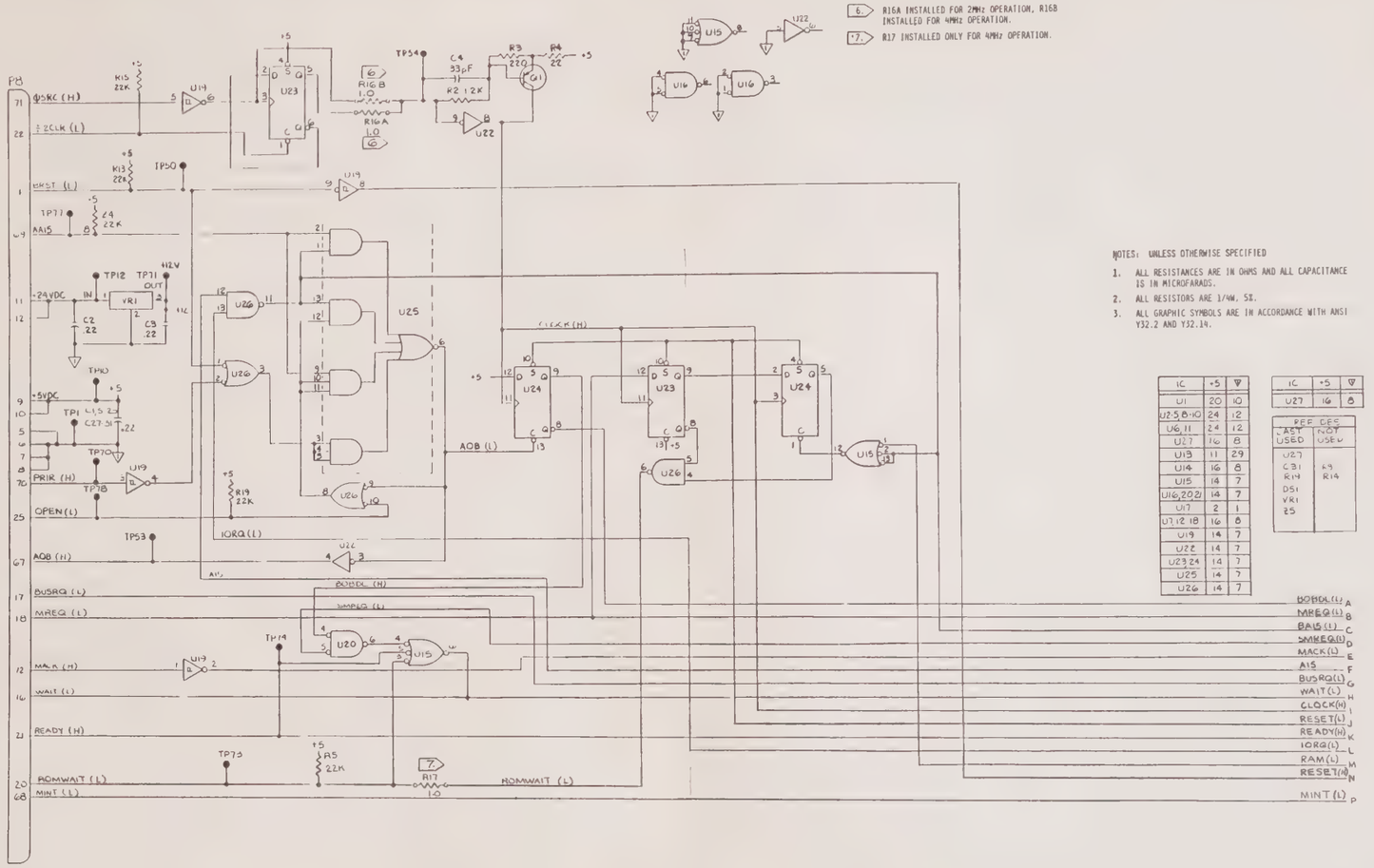


Figure 211-4. 2280A-211 Advanced Math Processor PCA

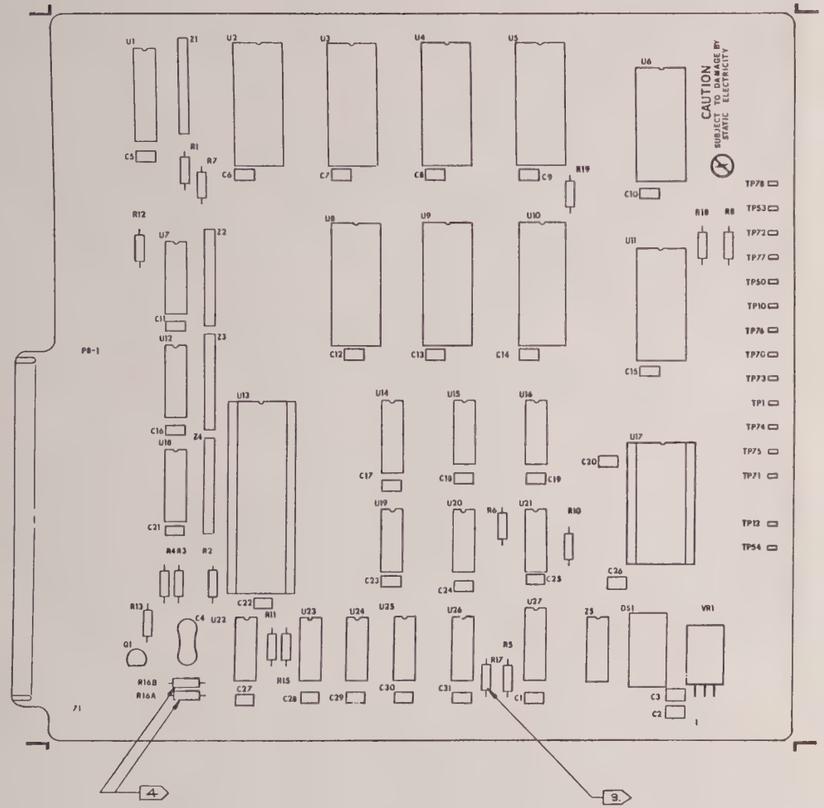


2280A-1611

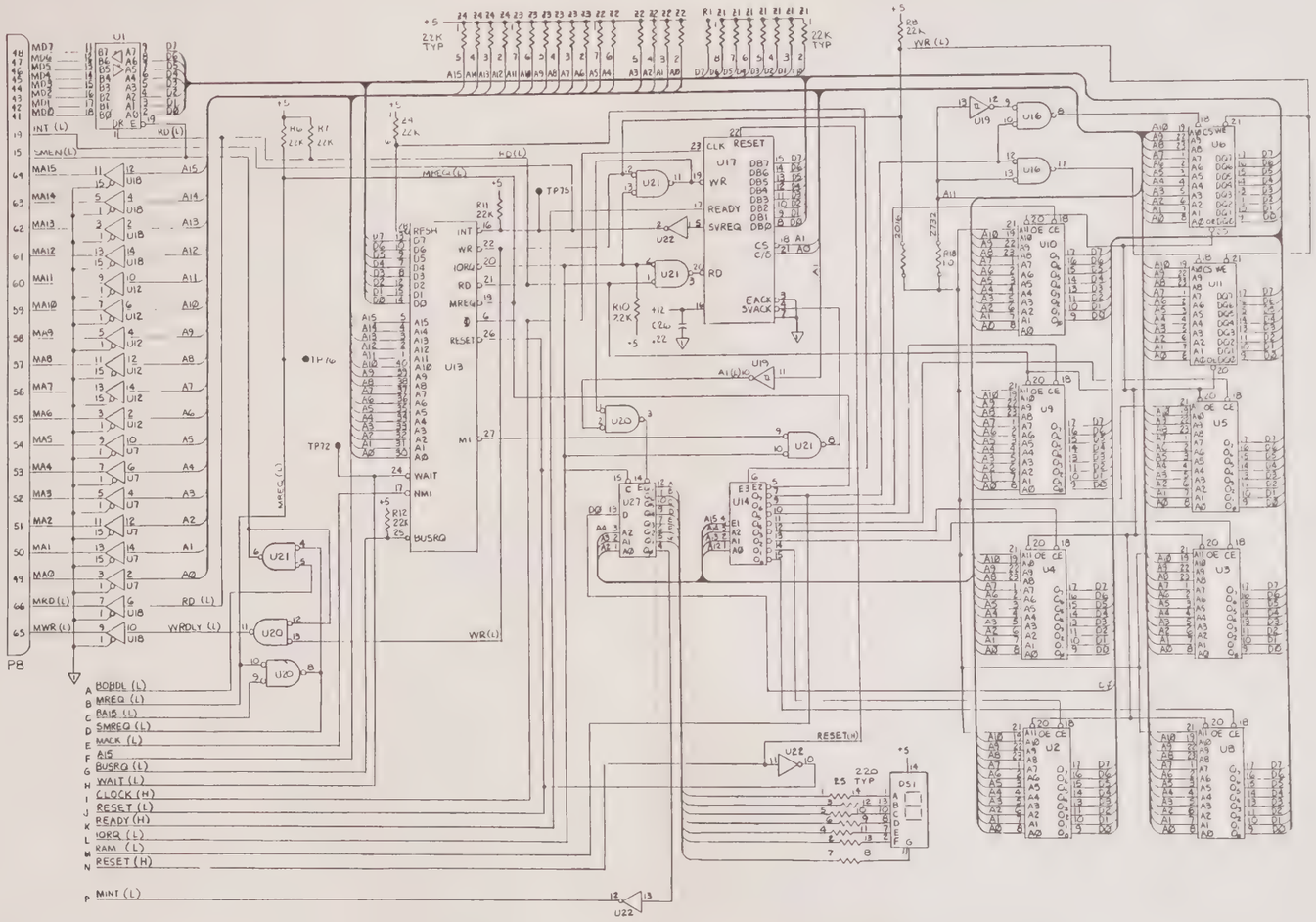


2280A-1011

Figure 211-4. Advanced Math Processor Schematic Diagram



2280A-1611



2280A-1011

Figure 211-4. Advanced Math Processor Schematic Diagram (cont.)

Option 2280A-214
Cartridge Tape Drive

DESCRIPTION

The Cartridge Tape Drive is an option that provides tape storage for data logger programs and data. It consists of two assemblies: the cartridge interface and the cartridge drive. The cartridge interface is a printed circuit board that controls the cartridge drive assembly, and the cartridge drive assembly moves the tape, writes to tape, and reads from tape.

WHERE TO FIND ADDITIONAL INFORMATION

In this subsection, the Cartridge Tape Drive (Option 2280A-214) theory of operation, general maintenance, performance tests, calibration procedures, a parts list, and a schematic diagram are given. Installation and system configuration instructions are given in the 2280 Series System Guide, and operation and programming instructions are given in the 2280 Series User Guide.

Test equipment required to perform the procedures in this subsection is listed in Table 214-1. A summary of test equipment required to perform all procedures in this manual is given in Table 1-1 in Section 1 of this manual.

Table 214-1. Required Test Equipment

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
Digital Extender	---	Fluke Part #486910
Digital Voltmeter or Multimeter	---	Fluke 77
Oscilloscope	---	Tektronix 2215

THEORY OF OPERATION

The following theory of operation discussion begins with an overall functional description of the Cartridge Tape Drive. Following this is a block diagram description that identifies and briefly describes the function of each major circuit block on the Cartridge Tape Drive. The next three sections present the general algorithms or sequence of events involved in writing information to the tape, reading from the tape, and moving or positioning the tape. A detailed circuit analysis then describes how each major circuit block on the Cartridge Tape Drive assembly works. Where necessary, block diagrams and simplified schematics are included with the text. Schematic diagrams for the Cartridge Tape Drive Option are at the end of this option subsection.

Overall Functional Description

The DC100 Cartridge Tape Drive provides logging data and program storage for the 2280 Series Data Logger. It consists of a printed circuit board assembly, referred to as the Cartridge Interface, and a tape drive, referred to as the Cartridge Drive. The Cartridge Interface is connected to the Cartridge Drive unit by two cables.

The Cartridge Interface assembly is a microprocessor controlled intelligent subsystem of the 2280. It receives commands from the mainframe using an instrument internal bus called the PIO bus. The microprocessor on this assembly controls and supervises all details regarding cartridge tape recording and playback. It develops and maintains a complete file system on the tape. The mainframe can ask the Cartridge Interface to open a file for reading or writing, erase the tape, send the directory of the installed tape, and selectively delete files on the tape. The mainframe can also command the Cartridge Interface to perform several functional tests of the Cartridge Drive option hardware to verify proper performance and assist in calibration and troubleshooting.

Block Diagram Analysis

- Microprocessor

  A 4-MHz Z-80 microprocessor is used to provide local control functions for the Cartridge Tape Drive option. The firmware for the

processor is stored in an EPROM and 2 K-bytes of RAM is available for local data buffering and firmware program variable storage.

- Memory and Input/Output Decoding and Control Logic

  The firmware executed by the microprocessor is located in a single EPROM, and a single RAM chip provides the temporary storage required for program variable storage and data buffering.

  Generation and sensing of various control signals is provided by a Z-80-PIO chip and several latched registers.

- Interrupt Generation and Acknowledgement

  Several real-time events occur periodically within the cartridge tape subsystem that cause to microprocessor firmware to temporarily stop what it is doing, take care of the real time event, and then resume what is was doing.

- PIO Bus Communication

  The PIO Bus is a parallel interface through which all communication between the Cartridge Interface assembly and the controller assembly takes place. In addition to the eight-bit bus to transfer data, there are two signals that address the Cartridge Interface, two that identify the type of PIO Bus transaction, an interrupt line, and a few handshake signals.

- Tape Drive

  A Qantex Model 200 MiniDrive is used within the Data Logger. It records data at 1600 bits per inch on two tracks. The drive has minimal electronics located on two small printed circuit assemblies: the read/write and status drive. The read/write portion of the drive electronics allows the 2280 Cartridge Interface assembly to select track A or B, enable writing, send write data, and receive read data. The drive's status assembly allows the interface assembly to sense the motion of the motor, determine the speed of the tape, select tape direction, determine whether a cartridge is installed, and sense whether the installed cartridge is write protected.

- Tape Write

  Data or programs are written to tape in blocks of 1024 bytes. Each of these blocks consists of a preamble, data bytes, error check code, and postamble. Blocks of data are separated from one another on tape by gaps which are areas on tape where no flux transitions are present. Data is recorded on tape in a format known as Manchester Phase Encoded. The collection of hardware in the tape write block consists primarily of a shift register to convert the parallel data from the microprocessor to serial form and a phase encoder to convert the simple serial data bit sequence into a manchester format.

- Tape Read

- CRC Generator and Checker

  A Cyclic Redundancy Check code is recorded at the end of each block of data. This polynomially generated code is used to validate the correct writing and reading of data.

- Motor Speed Control

  The motor speed control circuitry maintains tape speed at read or write speeds of 30 inches per second and fast forward or rewind speeds of 77 inches per second. This involves generating an error signal by comparing the actual tape speed versus a reference value and sending this signal to control circuitry on the tape drive.

- Motor Power Supply

  Power for the Cartridge Drive motor is generated by a step-down, switching power supply driven from the +24V supply.

- Power Supply Arbitration Logic

  To reduce instrument power consumption, the cartridge tape is not allowed to move tape (read or write) when the printer is printing. This logic allows the printer and cartridge tape subsystems to coordinate power supply usage.

- Test Status Indicator

  Four LED's on the frontmost edge of the Cartridge Interface assembly indicate the assemblies self test results status. They indicate the viability of the microprocessor, ROM, RAM, and data encoding and decoding circuitry.

WRITING THE TAPE

Data is written to the tape in blocks surrounded by gaps. Each block consists of a preamble, followed by data, CRC (cyclic redundancy check), and postamble fields.

Writing is done with a different gap on the tape head than the one used for reading. When reading old tape information, the write gap is de-energized. While writing to the tape, the WRT (Write) signal energizes the write gap. Tape travels past the write head, picks up the new information, then travels a short distance and passes over the read gap. This signal is recovered by the read electronics to perform a "read-after-write". The success of the write operation is verified by comparing the bytes read to the bytes written.

When confronted with the task of writing a block of data to the tape, the end of the last block written is searched for (unless the destination is the beginning of the tape, where the load point hole is searched for instead). Next, the tape is backed up three inches (into the middle of the previous block) in order to get a running start. The tape is started running forward, and one of two cases ensues:

1. If the block about to be written is the first block on tape, then the tape is advancing toward the load point. The WRT signal is set to energize the write gap, and the ENPE (Enable Phase Encode) signal is kept cleared to disable the phase encoder (in order to write a gap). The block is written a short distance after the load point.

2. If the block about to be written is not the first block on tape, then the WRT signal is kept cleared until the gap marking the end of the previous block is detected. When this happens, the WRT signal is set and the ENPE signal kept cleared to write the gap between the two blocks. After the tape has moved the distance allotted for gaps, the block is written.

To start writing the block, the ENPE signal is set, allowing the phase encoder to generate transitions. This signal takes effect when the next output byte is loaded into the write shift register. The control signals ENPE (Enable Phase Encode), CRCGEN (CRC Generate), and CRCOUT (CRC Output) all take effect on byte boundaries as the bytes are shifted out to the tape, and are manipulated by the interrupt routine to guarantee that switching between modes is synchronized with particular bytes. The following sequence is executed during a block write sequence:

1. Synchronization is achieved by writing some dummy bytes under the write data interrupt, then loading the first preamble byte under the interrupt and setting ENPE.

2. Under the second interrupt, the second preamble byte is loaded.

3. Under the third interrupt, the first data byte is loaded and the CRCGEN signal is set. This signal will enable CRC generation starting with the first bit of the first data byte.

4. For the next 1023 interrupt cycles, the next data byte in the block is loaded.

5. Under the next interrupt, the CRCOUT signal is set and a dummy byte is loaded. The source of output to the tape is switched (when the byte now being shifted out is exhausted) to the CRC generator (U62). CRCOUT causes CRC generation to cease, and the contents of the 16-bit CRC register in the CRC generator to be shifted out. The dummy byte is written to prevent ERROR from being set by a write under-run.

6. Under the next interrupt, another dummy byte is loaded.

7. Under the next interrupt, the first postamble byte is loaded and the signals CRCGEN and CRCOUT are cleared. These signals will take effect after the last CRC bit is shifted out. Clearing CRCGEN resets the CRC generator, and clearing CRCOUT switches the source of output back to the byte loaded by software.

8. Under the next interrupt, the second postamble byte is loaded.

9. Under the next interrupt, the phase encoder is disabled by clearing the signal ENPE (which, of course, takes effect after the last bit of the postamble is shifted out). A dummy byte is loaded.

10. A calibrated number of interrupts are allowed to occur to write the terminating gap and to allow the read-after-write to finish. Note that reading and writing are skewed due to the physical separation of the read and write gaps. Dummy bytes are loaded under all of these interrupts. When the allotted number of interrupts have occurred, a flag is set informing the non-interrupt firmware that the block write has completed.

After the block write finishes, tape motion is stopped and the result of the attempt examined. If the read failed to match what was written, or if the ERROR signal was set (indicating either a read over-run or a write under-run error), then the tape is backed up to the beginning of the block and the firmware tries again (up to a specified maximum number of retries).

READING THE TAPE

Data stored on the tape is read while moving the tape forward at slow speed. The data format closely follows the standard for DC300 tapes (ANSI X3.56-1977); however, at the time of this writing there is no explicit standard for DC100 tapes. Data is stored as magnetic flux transitions in block form; e.g., sections of data separated by erased sections called gaps.

A block of data is always nestled between two gaps and consists of four fields: preamble, data, CRC, and postamble. The preamble is used for synchronization, the data is the information stored, the CRC is used for error checking, and the postamble can be used as a preamble going the opposite direction (though this is not done in the 2280). Each field contains an integral number of eight-bit bytes recorded in serial fashion using Manchester phase encoding.

Manchester phase encoding is a "self-clocking" coding scheme. This means that both the data and the data-rate information can be recovered from the read signal as it comes off the tape. Ideally, bit-to-bit spacing is constant with this method; however, in reality spacing between adjacent bits varies slowly from bit to bit and can vary widely (as motor speed changes) between different blocks or drive units. One bits are always recorded as positive transitions, while zero bits are always recorded as negative transitions. Since bit-to-bit spacing is constant, extra transitions have to be inserted between adjacent zero bits or adjacent one bits. Figure 214-1 illustrates the encoded bit sequence 011001 using Manchester phase encoding.

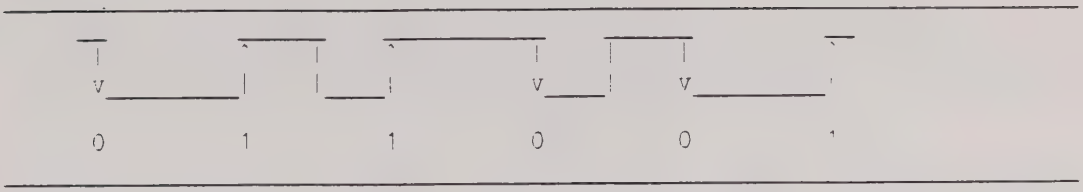


Figure 214-1. Manchester Phase Encoding

The encoded format of a recorded block is illustrated in Figure 214-2. Immediately following the gap is the preamble, which always contains fifteen zero bits followed by a single one bit. The preamble's purpose is to allow the hardware to sort out which transitions are significant--this is done by synchronizing the decoder hardware with the negative transitions; e.g., getting "on track" with the known fifteen zero bits. The trailing one bit is there to mark the end of the preamble--by the time it arrives, the hardware must have extracted data rate information. After the trailing one bit arrives, the decoder runs into the data field, which is essentially a pseudo-random stream of ones and zeros. To maintain synchronism, a device known as a 2/3-cell timer is employed (see Figure 214-3). With this scheme, each bit is timed to determine inter-bit spacing. After detecting a significant transition, the 2/3-cell timer ignores any transitions that occur before 2/3 of the estimated bit time has elapsed. It then opens a "window", forcing the next transition to be interpreted as significant.

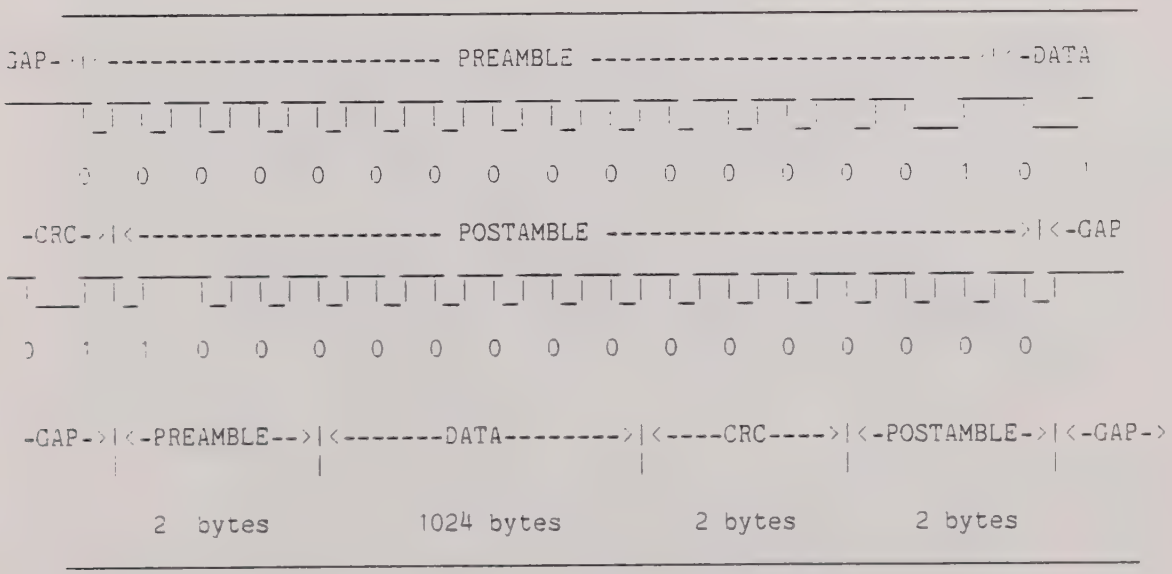


Figure 214-2. Recorded Block Format

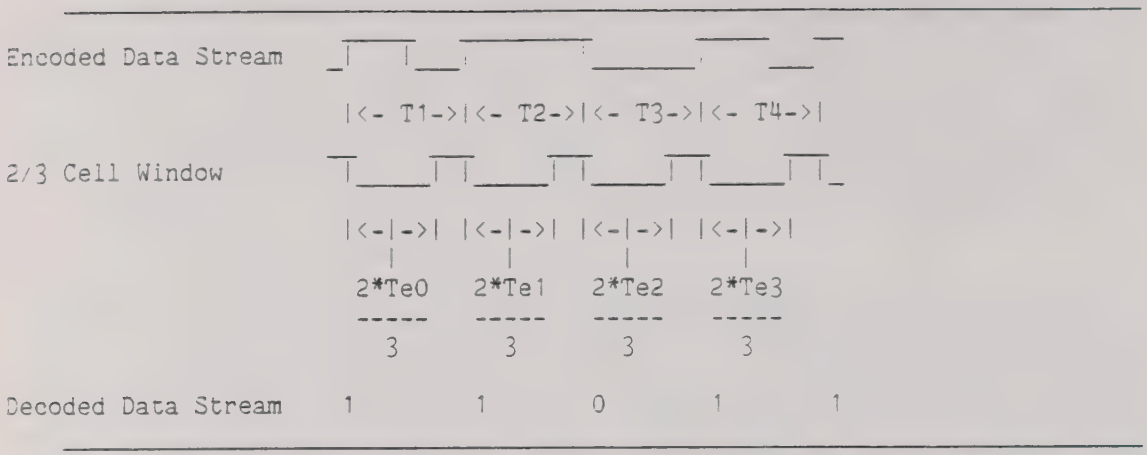


Figure 214-3. 2/3-Cell Timer Operation

After the end of the preamble, every eight significant transitions are formed into eight-bit bytes and sent to the processor. As soon as a new byte is available, it is loaded into a holding register and the processor is informed by the INRDY (Input Ready) signal going high. The processor then reads the byte, which forces INRDY low again.

If a new byte becomes available before the processor has read the last one (that is, INRDY is still high), then an input overrun error has occurred. When this happens, the last byte received is lost. This event causes the ERROR signal to go high.

The data field of the block consists of a fixed number of bytes, after which comes the two-byte CRC (cyclic redundancy check). This code checks the integrity of the data, and it is explained in greater detail later. Cyclic redundancy checking begins with the first byte of the data field, and stops immediately after the second CRC byte--preamble and postamble bytes are not checked. (The processor counts the number of bytes received, and disables checking when it has received the requisite number.) For the vast majority of possible errors, the CRCERR (CRC Error) signal will be high after the second CRC byte is received; otherwise, if CRCERR is low the data was either received correctly or an extremely unlikely pattern of errors occurred.

MOVING THE TAPE

Tape motion is controlled by the signals RT (Run Tape), FAST, and FWD (Forward). When RT is high, the drive motor runs in the direction specified by FWD at the speed specified by FAST. Speed feedback is provided by an optical tachometer on the drive which generates the SYNC signal. One SYNC cycle corresponds to a tape travel of 0.0076 inches.

The nominal slow (FAST = 0) tape speed is 30 ips (inches per second). At this speed, the SYNC period is about 250 microseconds. This speed is set during calibration by adjusting R53 on the Cartridge Interface assembly.

This adjustment provides the reference input to the Motor Speed Reference Amplifier. Speed is controlled by comparing the output of the Motor Speed Reference Amplifier with the output of the Motor Speed Frequency-to-Voltage Converter and automatically adjusting the motor drive voltage accordingly. The output of the Motor Speed F-to-V Converter varies linearly with SYNC frequency.

Switching between fast (FAST = 1) and slow (FAST = 0) tape speed is done by the Motor Speed F-to-V Converter. Fast speed is 2.57 times slow speed (about 77 ips). With a 140-foot tape, rewinding takes about 22 seconds.

Since tape length is not "infinite" (as in an 8-track tape), holes punched near the ends of the tape are detected and used to inform the microprocessor that the end is near. Tape motion must be stopped before the end is reached, since (unlike cassette tapes) the tape ends are not attached to the reels and it is therefore possible (in a fault situation) to wind the tape off the end. If this should happen, the tape cartridge would have to be taken apart and re-threaded.

The configuration of holes in the tape is shown in Figure 214-4. The BOT (Beginning of Tape) holes can be distinguished from the EOT (End of Tape) holes by the processor, since BOT holes come in pairs. When confronted with the problem of finding the beginning of the tape, the firmware causes tape to wind forward in search of a hole. If tape travels 36 inches without finding one, it concludes that the tape is positioned between the LP (Load Point) hole and the EW (Early Warning) hole, and rewinds the tape to just before the LP hole. If a hole is encountered, the firmware determines whether the hole detected was of the single or double (BOT) hole variety. If a double hole was detected, the LP hole is searched for in the forward direction and the tape is left parked just before it. Otherwise, a single hole was detected, and repetitive hole searches in reverse commence until either 36 inches elapse without finding a hole or a double hole is found.

Holes are detected by a light sensor on the drive which is normally blocked by the presence of opaque tape between it and an LED. A tape hole moving past allows light to impinge on it momentarily, which in turn sets a flip-flop that drives the TMSL (Tape Mark Sense Latched) signal high. After recognizing this signal, the processor resets the flip-flop by pulsing RESET TMS(L) low.

Before trying to move tape, the processor needs to see if any tape is installed. This is indicated by the IRDY(L) (Interface Ready) signal. IRDY(L) is low only if a tape cartridge is installed and the tachometer system is functional. In addition, the signal TMS SAFE(L) indicates whether the tape mark sensor system is alive and well. Signal TMS SAFE(L) will be low only if the TMS system is functional and tape is present between the LED and the sensor.

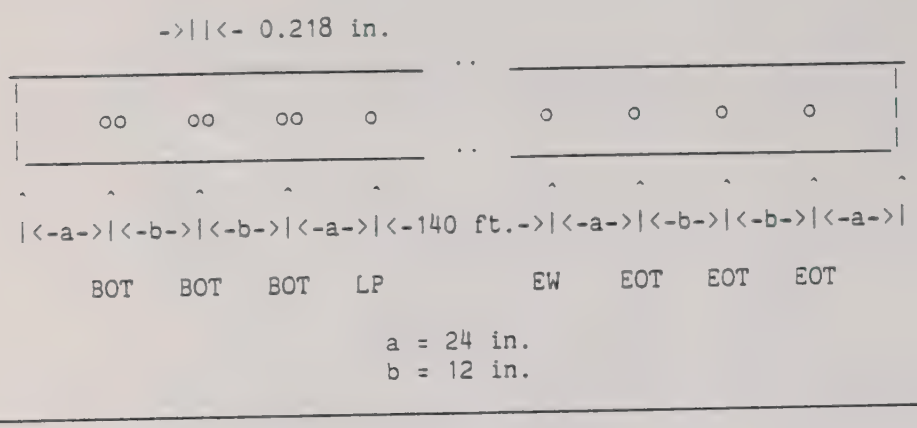


Figure 214-4. Tape Holes

Detailed Circuit Description

MICROPROCESSOR

The Z-80 microprocessor (U33) running at 4-MHz provides the local processing required to drive the cartridge interface electronics and interface with the controller assembly. An 8-MHz clock is provided by U21 and then divided by two using U22. An active pull-up to the +5 volt supply is provided by U31, Q3, R21 through R24, and C28.

The processor communicates with all other components of the assembly using the address bus to select the source or destination of information, the data bus to either send or receive information, and several control signals to synchronize the operations.

MEMORY AND INPUT/OUTPUT DECODING AND CONTROL LOGIC

Memory And I/O Accesses

The Z-80 microprocessor on the Cartridge Interface has two distinct address spaces: Memory Space and I/O Space. The type of access being performed is determined by the signals MREQ(L) (Memory Request), IORQ(L) (Input or Output Request), M1(L) (Machine Cycle One), RFSH(L) (Refresh), RD(L) (Read), and WR(L) (Write) (see Table 214-2). Timing diagrams for each type of access are given in Figures 214-5 through 214-9.

The RAM, ROM, and the memory-mapped write-only control and read-only status registers lie in memory space, while the Z-80-PIO chip resides in I/O space. The same address and data busses are used for both I/O and memory accesses, but the address decoding is different. The results of the two separate decoding paths are given in Figure 214-10, the Memory Space Map, and Figure 214-11, the I/O Space Map.

Large portions of Memory and I/O space are unused. Consequently, not all of the address lines are used to accomplish full decoding (a technique known as "sparse mapping"). Since addresses are sparsely mapped, more than one address can be used to access the same physical hardware. For simplicity, the Memory and I/O Space Maps shows only one of these addresses.

Table 214-2. Cycle-Type Coding Signals

MREQ(L)	IORQ(L)	M1(L)	RFSH(L)	RD(L)	WR(L)	Cycle Type
0	1	0	1	0	1	Instruction Fetch
0	1	1	1	0	1	Memory Read
0	1	1	1	1	0	Memory Write
0	1	1	0	1	1	Memory Refresh
1	0	1	1	0	1	I/O Input
1	0	1	1	1	0	I/O Output
1	0	0	1	1	1	Interrupt Acknowledge

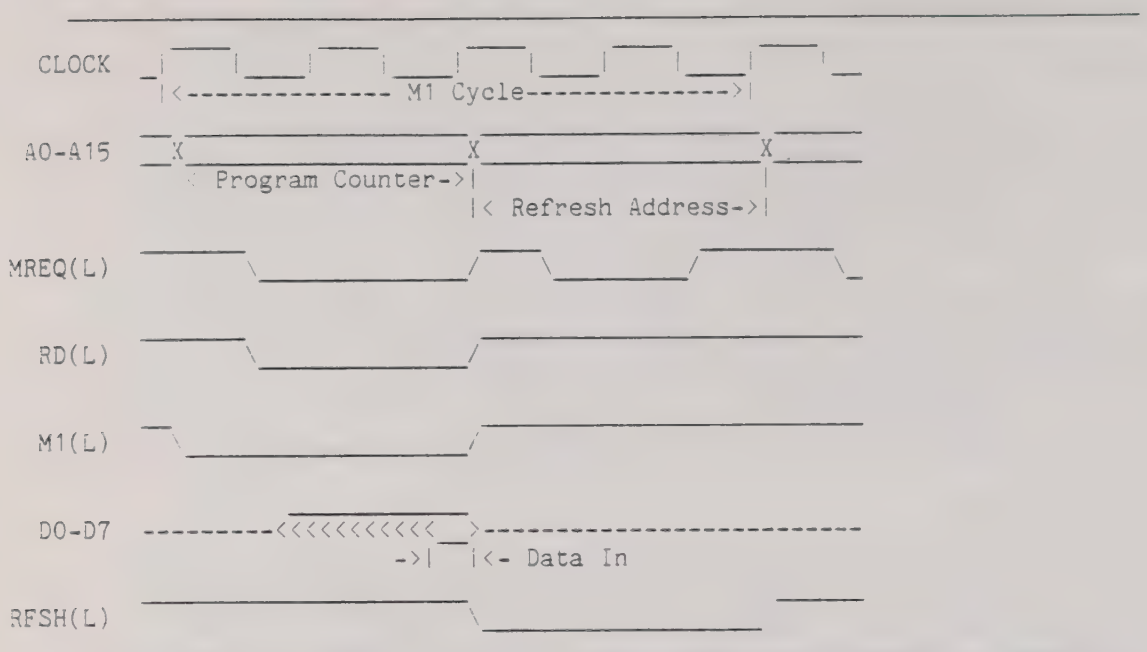


Figure 214-5. Instruction Opcode Fetch

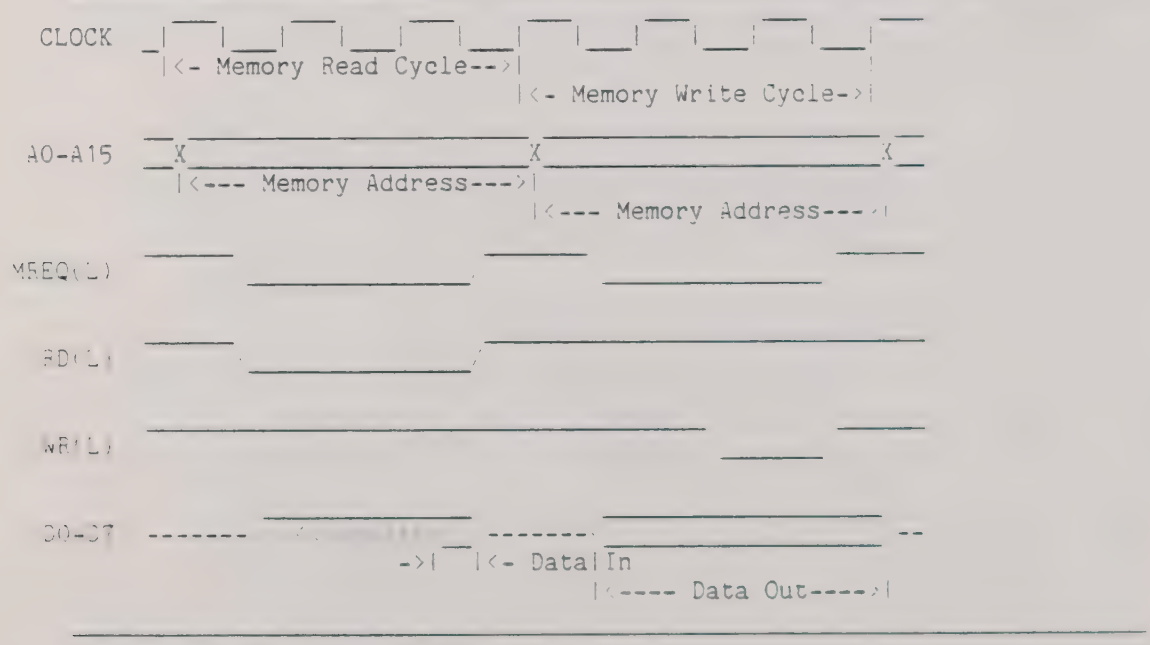


Figure 214-6. Memory Read or Write Cycles

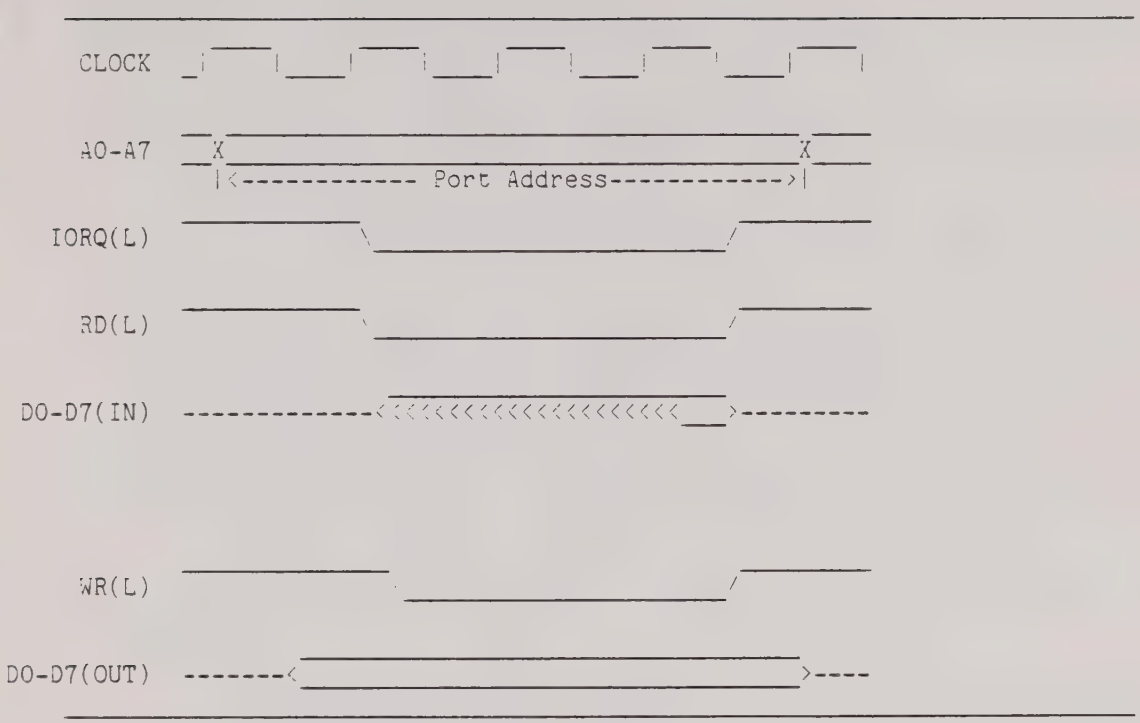


Figure 214-7. Input or Output Cycles

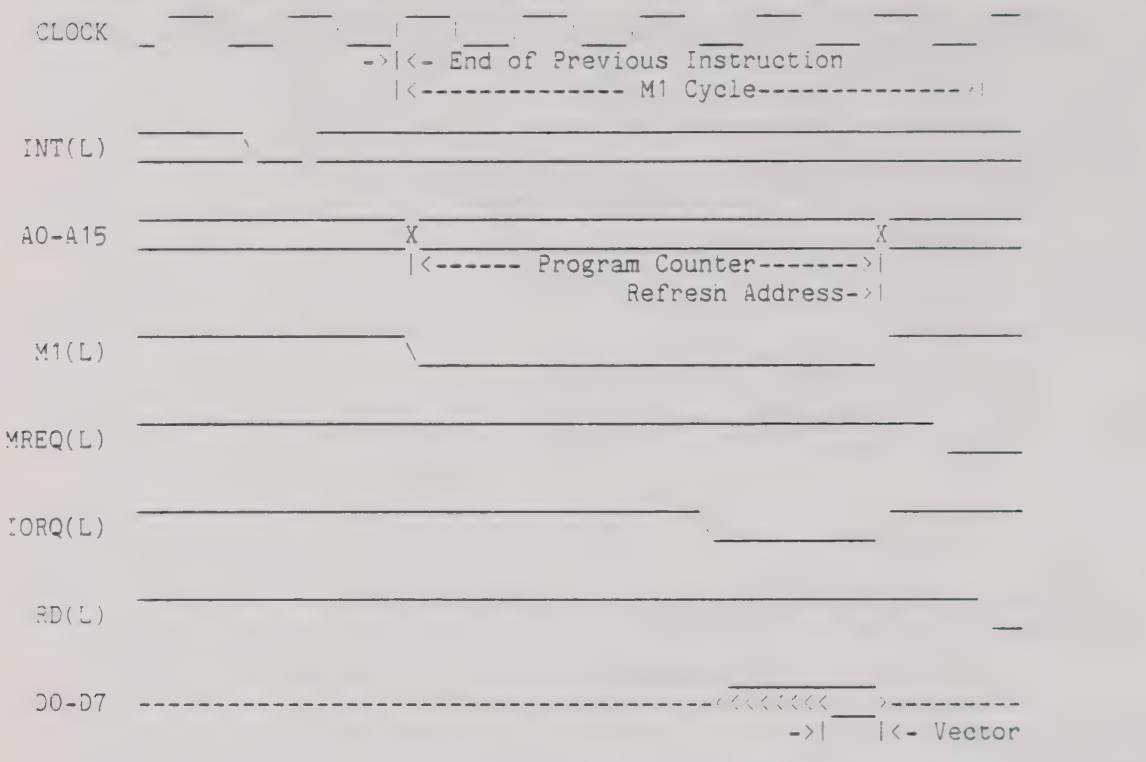


Figure 214-8. Interrupt Request / Acknowledge Cycle

Read		Write	
	FFFF	FFFF	
Unused			Unused
	C800	C800	
	C7FF	C7FF	
2k x 8 RAM			2k x 8 RAM
	C000	C000	
	BFFF	BFFF	
Unused			Unused
	A004	A004	
Read Register 3	A003	A003	Write Register 3
Read Register 2	A002	A002	Write Register 2
Read Register 1	A001	A001	Write Register 1
Read Register 0	A000	A000	Write Register 0
	9FFF	9FFF	
Unused			Unused
	2000	2000	
	1FFF	1FFF	
Two 8k x 8 ROM Banks			Unused
	0000	0000	

Figure 214-9. Memory Space Map

Read		Write	
	FFFF	FFFF	
Unused			Unused
	8004	8004	
Unused	8003	8003	Command, Port B
Unused	8002	8002	Command, Port A
Data, Port B	8001	8001	Data, Port B
Data, Port A	8000	8000	Data, Port A
	7FFF	7FFF	
Unused			Unused
	0000	0000	

Figure 214-10. I/O Space Map

Address Decoding

The Address Decoding block implements the Memory Space Map (Figure 214-9) and the I/O Space Map (Figure 214-10). Address lines A0 to A15 and control signals MREQ(L), IORQ(L), and M1(L) select a location in memory or I/O space. The memory cycle is qualified by mutually exclusive control signals RD(L) and WR(L), which determine a read or write cycle, respectively.

The system elements that interchange information via the address bus, data bus, and control signals are the Z-80 microprocessor, a Z-80-PIO chip, a 16k by 8 ROM, a 2k by 8 RAM, three 8-bit write-only control registers, one 8-bit write-only communication data register, two 8-bit read-only status registers, one 8-bit read-only communication data buffer, and one 8-bit read-only cartridge read data register. Address decoding is sparsely mapped, so it is important to note that processor accesses of certain forbidden addresses can cause bus conflicts.

Mutually Exclusive Address Bits

All read and write bus elements are in Z-80 memory space except the Z-80-PIO chip, which is in I/O space. For all accesses (including I/O cycles), address bits A15(L), A14, and A13 are mutually exclusive. Thus, valid combinations of A15, A14, and A13 are 000, 110, and 101.

For Z-80-PIO accesses, this implies that the processor register mapped to the high-order address byte is not arbitrary and must have the correct upper three bits. To accomplish this, the Z-80 instructions

```
out (c),r
in  (c),r
```

are used. These instructions map the register pair bc onto the address bus.

The actual mapping that occurs in both memory and I/O space is:

```
A15 = 0   =>   ROM
A14 = 1   =>   RAM
A13 = 1   =>   Memory-mapped Registers
```

For an I/O access; e.g., the Z-80-PIO:

```
A15 = 1
A14 = 0
A13 = 1
A2  = 0
```

Z-80-PIO CHIP

The Z-80-PIO chip (U32) has two 8-bit ports (port A and port B) that can be configured to operate in various modes. Each port is operated in only one of the possible modes: port B in the "control mode", and port A in the "output mode."

Port A

This port is used only for sending bytes to the tape while writing. When a byte is written to this port, the OUTRDY (Output Ready) signal goes high (U32-18). This is the signal to the Byte Serializer that a new byte is available. When the byte being shifted out is exhausted, a new byte is obtained from the output of port A, (the OUTPUT BUS signals 00 through 07) and the signal OUTSTB(L) (Output Strobe) is pulsed low to acknowledge receipt of the new byte. If the byte being shifted out is exhausted and OUTRDY has not yet gone high again (e.g., a new byte was not loaded in port A), an under-run error occurs. Pulsing OUTSTB(L) low forces OUTRDY low and causes an interrupt to occur.

Port B

The control mode allows any of the signals connected to port B to be used as interrupts (ERROR, TMS SAFE(L), IRDY(L), INRDY, TACH, GAP, and TMSL). In practice, only two of the above signals are ever used as interrupts (INRDY and TACH); the rest are simply polled. In addition, no more than one port B interrupt is enabled at a time; e.g., TACH and INRDY are forced to be mutually exclusive. TACH is used when positioning tape, while INRDY is used when reading the tape. INRDY is not used as an interrupt while performing a read-after-write; instead, all port B interrupts are disabled and INRDY is polled.

INTERRUPT GENERATION AND ACKNOWLEDGEMENT

Interrupts in program execution are requested when the IRQ(L) (Interrupt Request) input to the Z-80 microprocessor is low. The Z-80 has three possible ways it can respond to IRQ(L); however, only one is used on the Cartridge Interface. The method used requires the source of the interrupt to place the lower half of an interrupt vector on the data bus during an interrupt acknowledge cycle (see Table 214-2 and Figure 214-8).

Note

A vector is a 16-bit address pointing to a location in memory containing the address of the beginning of the interrupt service routine.

The upper half of the vector is contained in a dedicated Z-80 register. After the interrupt acknowledge cycle, the Z-80 pushes the current program counter on the stack. It then reads the interrupt service routine starting address from the 2-byte location pointed to by the interrupt vector, and branches to that address.

The Z-80-PIO chip (U32) is the only source of interrupts to the Cartridge Interface. After the Z-80-PIO chip has supplied an interrupt vector during an interrupt acknowledge cycle, the Z-80-PIO chip enters the "under service" state and the interrupt request line (IRQ(L)) is reset. While being serviced, the Z-80-PIO chip monitors the data bus, resetting the "under service" state when it detects a Z-80 "return from interrupt" instruction. It does not request another interrupt until service of the current interrupt is completed.

PIO BUS COMMUNICATION

The 2280 Series Data Logger contains a parallel bus called the PIO Bus that allows communication between the controller assembly (i.e., the main microprocessor in the 2280) and all logging and interface devices. To the Cartridge Interface, the PIO Bus is seen as address lines IA1 and IA2 (Interface Address), control lines IC5 and IC6 (Interface Control), BUSY(H), RDRDY(H) (Read Ready), RDSTB(L) (Read Strobe), WRRDY(H) (Write Ready), and WRSTB(L) (Write Strobe), data lines ID0 to ID7 (Interface Data), and interrupt line TPINT(L) (Tape Interrupt). A complete discussion of PIO Bus communication is contained in Section 3 of this manual.

The Cartridge Interface polls the state of the PIO Bus by reading Read Register 1 (U3) (see Figure 214-9), which accesses PIO Bus signals ADDRESSED(L) (a combination of IA1 and IA2), RDRDY, WRRDY, IC5, and IC6. In normal operation, this register is read several times before any action is taken, in order to guarantee that the values read are valid.

PIO Bus handshake and status signals from the Cartridge Assembly, including RDSTB(L), WRSTB(L), and BUSY, are latched in U5 and buffered to the Controller Assembly through U4.

The data lines ID0 through ID7 are read through buffer U13, which is enabled by the RS0(L) (Read Strobe 0) signal. These same data lines can be driven by U12 when enabled by information latched in U5.

TAPE DRIVE

The read/write portion of the drive electronics allows the 2280 cartridge interface assembly to select track 1 or 2, enable writing, send write data, and receive read data. The drive's status assembly allow the interface assembly to sense the motion of the motor, determine the speed of the tape, select tape direction, determine whether a cartridge is installed, and sense whether the installed cartridge is write protected.

The status assembly generates and receives several signals that deal with tape motion. The output signals from this assembly are:

TMS	Positive pulses at least 40 microseconds long are present while a hole is present at the tape mark sensor.
TMSL	A positive level appears when a hole in the tape is first detected by the tape mark sensor. This signal is latched and is reset by the RESET TMS(L) signal.
TMS SAFE	A positive level indicates that there is power on the tape mark sensor LED and tape (not a hole) is present between the LED and the sensor.
FP(L)	This signal is low when the installed cartridge has the file protect in the write protect position.
IRDY	A positive level indicates that the cartridge is in place and the optical tachometer LED is functioning.
SYNC	This signal is a series of pulses from the optical tachometer. The frequency of the pulse train is proportional to the speed of the motor and therefore the tape. The tape travels 0.0076 inches for each pulse.

The signals received by the status assembly are:

RESET TMS(L)	A low going pulse used to reset the latched TMS signal.
FSD	Forward servo drive is an analog voltage, which, when varied from 0 to +12 volts will drive the motor in the forward direction. The magnitude of the voltage will determine the speed of the motor. This signal is used in conjunction with the FWD signal.
FWD SW	This input is pulled low when forward motion is required. It allows current to flow through the motor from the FSD signal.
RSD	Reverse servo drive is an analog voltage, which, when varied from 0 to +12 volts will drive the motor in the forward direction. The magnitude of the voltage will determine the speed of the motor. This signal is used

in conjunction with the REV SW signal.

REV SW	This input is pulled low when reverse motion is required. It allows current to flow through the motor from the RSD signal.
+5	Regulated +5 volt power supply.
+12VS	Regulated +12 volt power supply. This voltage drives the motor.
+12	Voltage to drive the Tape Mark Sensor and associated circuits.
MOT RET	Ground connection for the motor power.
GROUND	Connection for signal ground.

The read/write assembly sources the following signals:

ANRD(L), ANRD	Analog filtered differential read signals from the read head. Levels are from 750 millivolts to 1.5 volts peak-to-peak around a reference voltage to 6.0 volts.

The read/write assembly accepts the following input signals:

TK SEL(L)	The track select signal is held low to select track 1 and high for track 2.
WRITE(L)	The write signal is driven low to enable writing.
WRITE DATA	This signal contains the encoded data to be written on tape.
WRITE PWR	A low level on this signal enables current to the write head.
GROUND	Write ground.
+12	+12 volt power.
+6	Regulated +6 volt power.
+5	Regulated +5 volt power.
READ GROUND	This ground is returned separately to the read amplifier on the cartridge interface assembly.

TAPE WRITE

Byte Serializer

The Byte Serializer takes parallel data from Port A of the Z-80-PIO Interface on lines 00-07 and converts it to a serial bit stream. In addition, it handles the handshake signals OUTRDY and OUTSTB(L), and provides the signals the Error Detector needs to detect write under-run errors.

Bytes are loaded into a shift register (U43), and shifted out at 47.6 kHz. Bit count and strobe generation are handled by a presettable counter (U9) and a strobe generator (U10, U11-1,2,3). See Figure 214-11 for timing details.

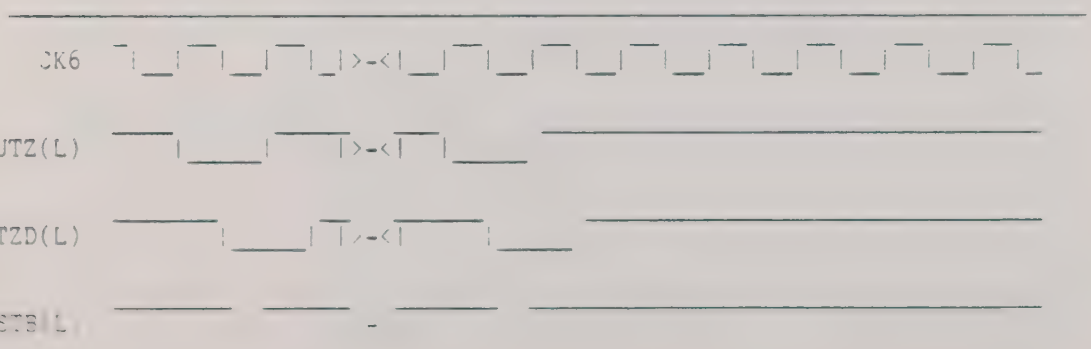
CRC/Serial Data Output Selector

Data written serially to the tape comes from either the Byte Serializer or the CRC Generator. Selection is controlled by the CRCOUT signal, which is synchronized to take effect between bytes by a D-type flip-flop (U18-13,15). This flip-flop controls a 2-input data selector (U20-8,9,10,11,12,13; U2-11,12,13), whose output is routed to the Phase Encoder and the CRC Generator. (Note: The CRC Generator only uses this output when the Byte Serializer is selected as the source of bits--see the section on the CRC Generator.)

Phase Encoder

The Phase Encoder uses Manchester phase encoding to encode the serial bit stream supplied by the CRC / Serial Data Output Selector. Two clocks are used: CK6, which runs at the bit rate (47.6 kHz); and CK5, which runs at twice the bit rate (95.2 kHz) (See Figure 214-12). The output WRITE DATA is sent to the drive, where it directly controls the write gap driver.

The Phase Encoder is asynchronously reset when WRT is low, which forces WRITE DATA high. If WRT is high, the Phase Encoder is enabled/disabled by ENPE (Enable Phase Encoder), whose action is synchronized to byte boundaries by two D-type flip-flops (U18-4,2; U38-9,12). When the Phase Encoder is disabled, WRITE DATA is forced high.



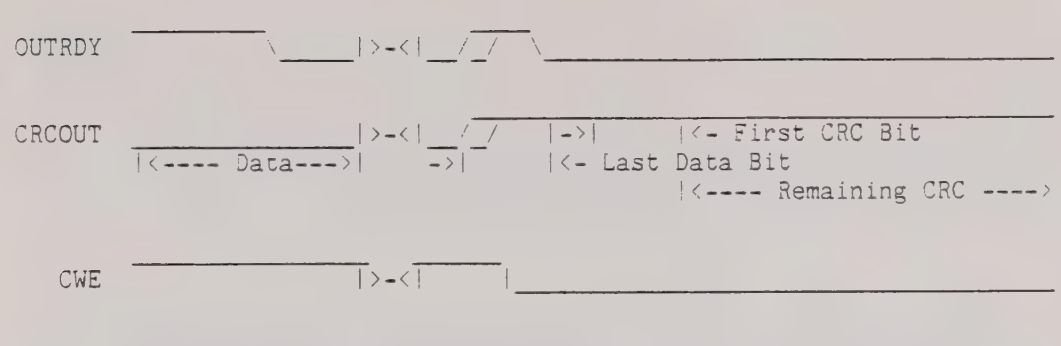


Figure 214-11. Byte Serializer Timing, CRC/Data Selector Timing

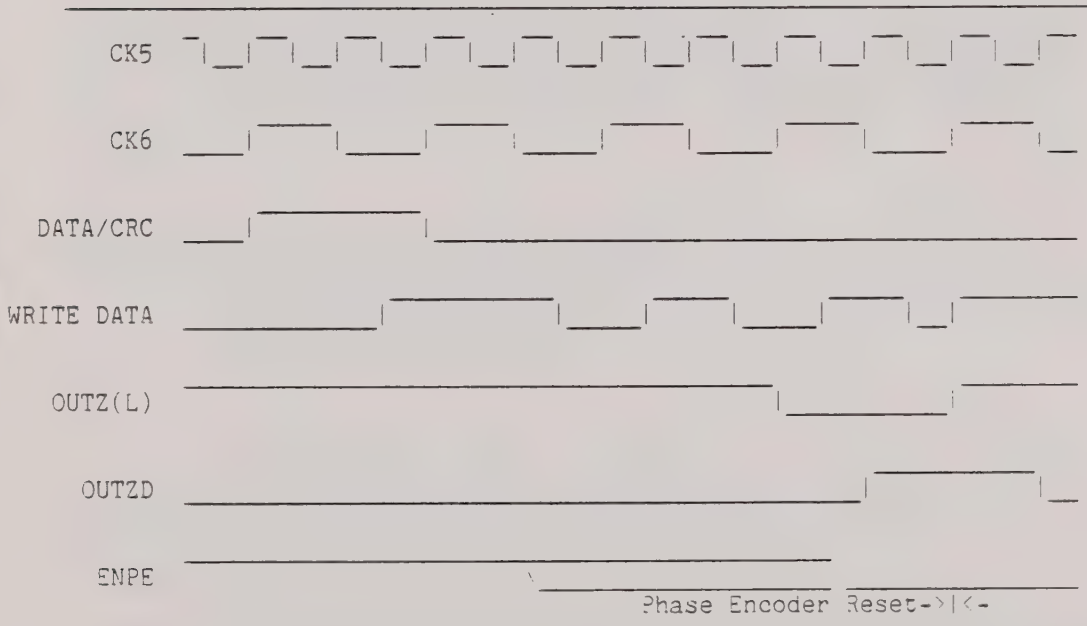


Figure 214-12. Phase Encoder Timing

TAPE READ

Read Amplifier

The Read Amplifier (U11) converts the differential signal supplied by the drive electronics to a single-ended signal, with a gain of approximately 12. This signal is then filtered and routed to the Read Data Comparator (U1) and the Read Clock Comparator (U2).

Read Data Comparator

The Read Data Comparator converts the analog signal supplied by the Read Amplifier to the digital signal DATA by comparing it to a programmable threshold. The threshold is controlled by signals PDRST(L) (Preamble Detector Reset) and WRT. Three threshold values are significant:

Gap Searching Threshold (PDRST(L) = 0)

Gap Searching threshold is set when positioning to a particular block on a pre-recorded tape. In this mode, the threshold has a considerable offset from the average value of the Read Amplifier output--this facilitates discrimination between the silence of gaps and the noise of data blocks.

Read Threshold (PDRST(L) = 1, WRT = 0)

Read threshold is set during an attempt to read a block that was written previously. The threshold has a slight offset from the average value of the Read Amplifier output, in order to decrease the probability of triggering on gap noise while approaching the beginning of the block.

Read-After-Write Threshold (PDRST(L) = 1, WRT = 1)

Read-after-write threshold is set during an attempt to read a block while it is being written. The threshold has a greater offset from the average value than that used during subsequent read attempts, in order to help assure future readability.

For all three thresholds, the Read Data Comparator employs a large amount of hysteresis to combat signal droop. This causes a delay after the signal passes the threshold before the DATA output signal changes. The Read Clock One-Shot compensates for this delay.

Read Clock Comparator

The Read Clock Comparator is essentially a zero-crossing detector designed to extract edge information with a minimal amount of jitter. It converts the output of the Read Amplifier to a digital signal by comparing it to its average value, and routes the result to the Read Clock One-Shot.

Read Clock One-Shot

A transition in the output of the Read Clock Comparator triggers the Read Clock One-Shot. The Read Clock One-Shot generates a pulse [illegible]

CLOCK signal) whose trailing edge captures the output of the Read Data Comparator. The duration of this pulse is about one-quarter of the nominal bit time, or one-half of the nominal duration of a pulse caused by the insertion of an insignificant transition (see the section that describes Manchester phase encoding). Validating the output of the Read Data Comparator with the trailing edge of the output of the Read Clock One-Shot helps guarantee that the information captured is valid, since the sampling is done where the signal swing is the largest.

The Read Clock One-Shot consists of a state machine (U6; U4-8,9,10; U5-13,12,11; U9) which detects transitions (in either direction) of the Read Clock Comparator and uses an embedded counter (U9) to generate a calibrated pulse. Edge jitter contribution is minimized by using the fastest available clock (8 MHz).

Read Clock Selector

The DATA signal supplied by the Read Data Comparator can be used for two purposes: positioning tape and reading tape. When positioning a pre-recorded tape, the DATA signal is sampled at a high rate to detect the presence of gaps or blocks. When reading tape, the DATA signal is sampled by the CLOCK output of the Read Clock One-Shot to form the recovered (still Manchester phase encoded) digital version of the read signal.

Clock selection by the Read Clock Selector (U35-1,12,13,9,10,11,8) is controlled by the signal PDRST(L). Signal PDRST(L) is low when positioning tape, and high when reading tape. The output is routed to the clock input of a D-type flip-flop (U16-2,6), which samples the DATA output of the Read Data Comparator.

Read Data Selector

The input to the Manchester phase decoding circuitry can be either the signal read from the tape or the signal generated by the Phase Encoder (to perform a "local loop-back" test). The Read Data Selector (U35-3,2,4,5,6; U39-5,6) is controlled by the signal EDTEST (encode/decode test).

Read Transition Detector

Significant positive and negative transitions of the Read Data Selector output are detected separately by the Read Transition Detector (U25-13,15,4,2; U49-1,2,13,12,3,4,5,6). Significant positive transitions cause a positive pulse on one output (U49-12); significant negative transitions cause a positive pulse on another output (U49-6). The duration of a pulse is one CK1 cycle; i.e., about 125 nanoseconds.

Interpretation of transitions as either significant or insignificant is controlled by either the Preamble Detector or the Bit Timer. During the process of preamble detection, the Preamble Detector may force the Read Transition Detector to interpret all transitions as significant (U53-1,2,3). When this is the case, the Preamble Detector is in charge of sorting out which transitions are significant. After the preamble has been detected and reading from tape commences, the Bit Timer takes over

the task of discriminating between significant and insignificant transitions.

Preamble Detector

The tasks of getting the Bit Timer synchronized to significant transitions and the Byte Deserializer synchronized to byte boundaries are handled by the Preamble Detector. When a preamble is detected successfully, the final preamble bit (the one bit) forces the Preamble Detector into a quiescent state; from then on, it has no effect on the timing.

Preamble detection is split into four distinct phases which are controlled by a 4-bit synchronous counter (U51). When the PDRST(L) (Preamble Detector Reset) signal is low, the content of the preamble counter is forced to three, and the DATOK (Data OK) signal is forced low. Preamble detection begins when PDRST(L) is taken high.

- Phase 1

  The first phase of preamble detection covers the range of preamble counter values 3 through 7, and it exists to synchronize the Bit Timer. Note that the preamble counter will never contain the values 0 through 2. During this phase, the Read Transition Detector is forced to interpret all transitions as significant (by reading the msb of the preamble counter, U51-11). The preamble counter will increment (controlled by U56-10,9,8) when the Read Transition Detector detects a negative transition, corresponding to one of the leading zero bits in the preamble. Also, a negative transition causes the Preamble Detector to send a control pulse (from U25-7) to the Bit Timer, which marks the end of a bit interval and is used by the Bit Timer to achieve synchronization.

- Phase 2

  The second phase of preamble detection covers the range of preamble counter values 8 through Hexadecimal E, and serves to reject false preambles. During this phase, significant/insignificant transition discrimination is controlled by the Bit Timer. If a positive significant transition is detected before the preamble counter reaches the next phase (i.e., the value Hexadecimal F), the Preamble Detector aborts and goes back to the beginning of the first phase.

- Phase 3

  Preamble detection enters the third phase when the preamble counter reaches the Hexadecimal value F. When this happens, the RCO (Ripple Carry Out) output of the preamble counter goes high, and is used to inhibit further counting. From that point, the preamble counter value will not change until it is reset by PDRST(L) going low. During normal preamble detection, this phase is entered a few bits before the last bit (a one bit) of the preamble arrives (since the preamble counter was pre-loaded with a value slightly greater than zero). The purpose of this phase is simply to wait for the trailing

one bit.

- Phase 4

  The fourth and final phase commences when the trailing one bit is detected. When this happens, the pulse provided by the Read Transition Detector (indicating a significant positive transition) anded with the RCO output of the preamble counter (U56-4,5,6) sets a J/K flip-flop (U42-5,6), which in turn drives the DATOK signal high. This action enables the Byte Deserializer and the Bit Strobe Generator, so that future bits are collected and sent to the processor. At this point, the Preamble Detector becomes idle and has no further significant role.

Bit Timer

The Bit Timer implements the 2/3-cell timer discussed earlier. Essentially, two simultaneous counting operations are going on for each bit: the current bit time is being measured, and 2/3 of the estimated bit time is allowed to elapse before a significant transition is expected to arrive. The ratio is achieved by running two 8-bit counters at different speeds--4 MHz and 6 MHz. The 4 MHz counter (hereafter called the MX counter) measures the current bit time counting up, while the 6 MHz counter (hereafter referred to as the ET counter) times out 2/3 of the estimated bit time counting down. The entire scheme is slaved to the pulse that occurs when a significant transition is detected (from U25-7).

When a significant transition is detected, a pulse ripples through a simple chain of 4 D-type flip-flops (U24) and a J/K flip-flop (U42-2,3). The outputs of these flip-flops control the loading, clearing, and enabling of the two counters (U29; U28, U30). The sequence that occurs is as follows (see Figure 214-13):

1. The EBT (Enable Bit Timers) signal (U42-3) signal goes low, which disables the clocks to both counters.

2. The LBT(L) (Load Bit Timers) signal (U24-6) pulses low, loading the estimated bit time from an 8-bit register (U64) into the ET counter (U28, U30) simultaneously with loading the next estimate into the 8-bit register (U64). The next estimate is generated by summing (U65, U66) half the previous estimate and half the bit time measured by the MX counter.

3. The CBT (Clear Bit Timer) signal (U24-14) pulses high, clearing the MX counter (readying it for the next bit).

4. Finally, the EBT signal goes back high, and we're off and running.

When the ET counter reaches zero (e.g., a borrow occurs from both 4-bit stages; U28-13 and U30-13) a J/K flip-flop (U8-3,2) is set. This forms the signal to the Read Transition Detector to interpret the next transition as significant.

The 6 MHz clock to the ET counter is generated from the 8 MHz clock by

dropping every fourth pulse. The pulse dropper operation is controlled by a 4-bit counter running at 8 MHz; when this counter's two least significant bits are zero, the output pulse is suppressed.

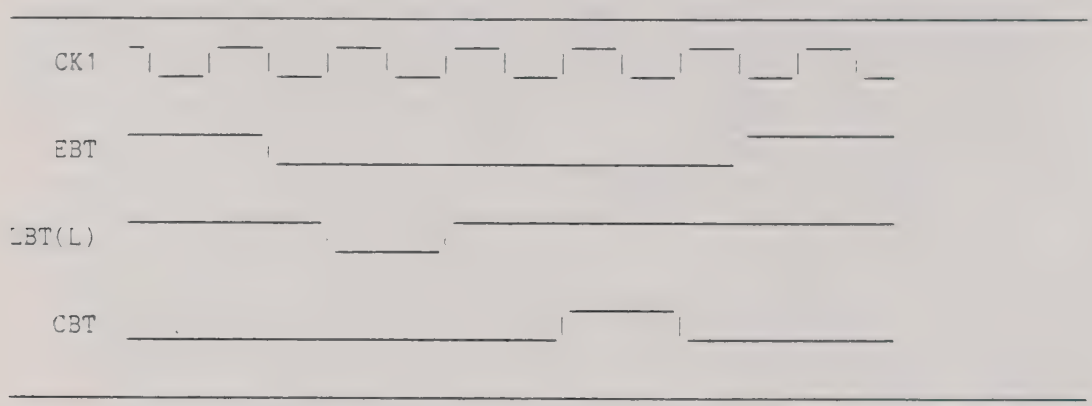


Figure 214-13. Bit-Timer Sequencing

Gap Detector

The Gap Detector (U7-1, 2, 6; U8-5, 8, 9, 11; U11-11, 12, 13,; U54-11, 12, 13) uses the outputs of the Read Transition Detector to form a partial determination of the existence of a gap. Any significant transition asynchronously resets the Gap Detector, forcing the GAP signal low. However, the Gap Detector requires silence for about 190 microseconds before it allows GAP to go high.

The GAP signal is normally used when positioning tape. When doing this, the firmware holds PDRST(L) low, thus forcing the Read Transition Detector to interpret all transitions as significant. This also sets the gap searching threshold for the Read Data Comparator. In this mode, the GAP signal is quite reliable when it is true (high), and not as reliable when it is false, since any noise in a gap may accidentally reset the GAP signal. This is because the GAP signal is essentially the result of a uni-directional debounce of read transition signals. The other half of the debouncing algorithm is implemented in firmware.

Bit Strobe Generator

When a significant transition is detected that corresponds to valid data (when DATOK is high), the Bit Strobe Generator generates the strobes the Byte Deserializer and the CRC Checker need to obtain the new bit. The Bit Strobe Generator consists of three D-type flip-flops (U22-12,9; U59-4,2,13,15) and generates signals STB and DATSTB.

Byte Deserializer

The Byte Deserializer assembles bytes from incoming bits and ships them

off to the processor. Bit count is maintained by a synchronous counter (U61). When the bit counter indicates that the shift register (U37) is full, the shift register contents are transferred to a holding register (U47). This holding register is an octal tri-state latch that interfaces to the processor data bus.

The shift register and bit counter are both clocked by DATSTB (Data Strobe), which is supplied by the Bit Strobe Generator. When the bit counter reaches zero, indicating that the shift register contains a full byte, a small state machine consisting of two D-type flip-flops (U59), two 2-input AND gates (U58-4,5,6,8,9,10), and a J/K flip-flop (U57-10,15) strobes the contents of the shift register into the holding register before the next bit arrives, then sets INRDY (Input Ready) high to inform the processor of the availability of a new byte. If the previous byte wasn't read yet when this happens, then INERROR goes high for one clock cycle, allowing the Error Detector to flag a read over-run error.

Error Detector

The Error Detector detects both read over-run errors and write under-run errors. The Error Detector is synchronous with both the state machine which strobes the new byte to be written into the write shift register and the state machine which strobes the byte just read into the read holding register. It consists of a 2-input OR gate (U2-8,9,10) and a J/K flip-flop (U57-6,1). The flip-flop is set when either error occurs, driving the ERROR signal high. The flip-flop (U57) is reset when the ERRCL (Error Clear) signal is high--note that ERRCL is the logical inverse of PDRST(L).

CRC GENERATOR AND CHECKER

A Cyclic Redundancy Check (CRC) code is recorded at the end of each block of data. This polynomially generated code is used to validate correct data write and read.

The CRC chip (U62) serves to check the CRC when reading a pre-recorded tape, and to generate the CRC when writing to tape. A quad 2-input data selector (U50) selects the inputs to the CRC chip. U50 is controlled by the WRT signal (which is low when reading, high when writing).

CRC Generation

CRC generation is controlled by the signals CRCGEN (CRC Generate) and CRCOUT (CRC Output). Both signals are synchronized by D-type flip-flops (U18-13,14; U18-12,11) to take effect on byte boundaries as data is written to the tape. When low, CRCGEN holds the CRC chip in the reset state. When CRCGEN is high and CRCOUT is low, the CRC chip calculates the CRC polynomial x^16 + x^15 + x^2 + 1 on the incoming data (on the D input, U62-11). When CRCGEN is high and CRCOUT is low, the CRC chip shifts out the contents of the internal 16-bit CRC register on the Q output (U62-12).

CRC Checking

CRC checking is controlled by the signal CRCCHK (CRC Check). CRCCHK is synchronized by a D-type flip-flop (U60-5,2) to take effect on byte boundaries. The CRC chip is held reset by the DATOK signal, thus, when the preamble has been successfully detected, the CRC chip is automatically enabled for the first bit of the first byte. The data bits are clocked into the chip by the STB signal, which is generated by the Bit Strobe Generator. The CRCCHK signal is taken low by the software just before the last CRC byte is read, so that the clock input to the CRC chip is disabled (U58-11,12,13) after the last CRC bit is checked. If the block read succeeded, the contents of the CRC register will be zero at this point, driving the CRCERR (CRC Error) signal low; otherwise, CRCERR will be high.

MOTOR SPEED CONTROL

The motor speed control circuitry maintains tape speed at read or write speeds of 30 inches per second and fast forward or rewind speeds of 77 inches per second. This involves generating an error signal by comparing the actual tape speed to a reference value and sending the error signal to control circuitry on the tape drive.

Motor Speed Frequency-To-Voltage Converter

The Motor Speed frequency-to-voltage converter consists of a programmable digital one-shot (U10; U3; U5-1,2,3; U4-4,5,6) and a low-pass filter. The digital one-shot converts each SYNC transition to a programmable width pulse. SYNC pulses are caused by the optical timing wheel on the drive--each pulse corresponds to a tape travel of .0076 inches. The pulse width is set by the signal FAST; when FAST is low, a tape travel speed of 30 ips (inches per second) is selected--when FAST is high, a tape travel speed of 77 ips is selected.

The digital one-shot consists of essentially the same circuit described in the section on the Read Clock One-Shot. The effect FAST has on the circuit is to select the count loaded into the embedded counter.

The low-pass filter is a simple level-shifter (Q1, Q2) followed by an R-C filter and a gain stage (U8-5,6,7). The output is one of the inputs to the Motor Speed Error Amplifier (TP84).

Motor Speed Reference Amplifier

The Motor Speed Reference Amplifier allows calibration of nominal tape speed, and it provides some acceleration and deceleration profile generation. Nominal tape speed is controlled by adjusting R53. (Acceleration and deceleration profiles are generated by the circuit containing U13-5,6,7; U13-2,3,1.) The output of the Motor Speed Reference Amplifier is one of the inputs to the Motor Speed Error Amplifier (TP81).

Motor Speed Error Amplifier And Direction Control

The Motor Speed Error Amplifier (U13-12, 13, 14) compares the output of the Motor Speed F/V Converter (which is proportional to tape speed) to the output of the Motor Speed Reference Amplifier (which is proportional to the desired tape speed) and generates an error signal. This signal is applied to either the FSD (Forward Servo Drive) signal or the RSD (Reverse Servo Drive) signal. The selection is controlled by the signals REV SW(L) (Reverse Switch) and FWD SW(L) (Forward Switch), whose low states are mutually exclusive.

MOTOR POWER SUPPLY

The power to drive the motor is generated by a step-down switching power supply. This supply is controlled by a special power-supply control chip (U1). Current limiting is provided by sensing current flow in a printed circuit board trace on an inner layer (U1-4,5). The output voltage is adjusted with R5. Voltage feedback is provided by R9 and R10. The main switching components are CR1 and Q1, while L1 and C5 provide the main output filtering.

POWER SUPPLY ARBITRATION LOGIC

The output of the +24V supply is shared by the Printer and Cartridge interfaces. Because of the heavy current demand created by these two sub-systems, only one can be operated at a time. In the case of the Cartridge Interface, the power demand is generated by the drive motor when tape is in motion.

Access to the +24V supply is controlled by the arbitration signals PRON(L) (Printer On) and CTON (Cartridge On). Signal PRON(L) is active (low) when the Printer is either requesting or using the supply; likewise, CTON is active (high) when the Cartridge is either requesting or using the supply. Neither sub-system is allowed to initiate the use of the supply if the other's arbitration signal is active.

Deadlock is avoided by permanently assigning higher priority to the Cartridge Interface. If the Cartridge Interface desires access to the supply, it sets CTON and waits for PRON(L) to become inactive. The Printer will not re-assert PRON(L) until CTON becomes inactive. Of course, this system works only if the Printer is either not installed or is functioning properly.

TEST STATUS INDICATOR

Four LED's (DS1-DS4) provide various indications of Cartridge Interface status. At power-up, they display the results of the Cartridge Interface self-tests as follows:

The first thing the microprocessor firmware does after coming out of reset is to turn off the topmost LED on the assembly (DS1). This provides some immediate indication about the viability of the processor, ROM, and memory-mapped write-only registers. If the LED remains on, the processor or the ROM has probably failed.

Second, the ROM self-test is executed. This self-test computes the ROM checksum and turns off the second LED (DS2) if the unit passed the test. If the unit does not pass the test, the led stays on and the remaining tests are skipped.

Third, the RAM self-test is executed. If the unit passes this test, the third LED (DS3) is turned off; otherwise, it stays on and the remaining tests are skipped.

Finally, the digital section of the Manchester phase encoding and decoding circuitry is tested. The signal EDTEST goes high, and an entire block of data (complete with preamble, data, CRC, and postamble) is run through the encoder to U35, then is sent back from U35 through the decoder, and is read by the processor. If the data is not returned, or if the returned data does not match the data written, then the last LED (DS4) stays on. After the self-tests are run, the self-test result is sent to the Controller. The self-test result is displayed only if the test result indicates a failure. If no self-test result is sent to the Controller (i.e., no Cartridge Interface response), the Controller assumes that no Cartridge Tape option is installed.

MAINTENANCE

The following paragraphs provide maintenance information for Option 2280A-214, the Cartridge Tape Drive. Maintenance procedures include: cleaning instructions, tape packing instructions, tape rethreading instructions, performance test procedures, calibration adjustment procedures, a list of replaceable parts, and a schematic diagram.

Cleaning

Tape drive components require periodic cleaning to ensure proper operation. The tape head and drive capstan should be cleaned after 8 hours of tape motion, and the tachometer and tape mark sensor should be cleaned monthly. Use the procedures given in the following paragraphs to clean the tape drive components.

TAPE HEAD CLEANING

The tape head and capstan should be cleaned after each eight hours of tape motion. Use the following procedure to clean the tape head and capstan.

CAUTION

Do not use magnetic devices near the tape head. Do not touch the tape head with metal objects or other hard objects. Doing so may damage the head, resulting in tape cartridge damage.

1. Inspect the tape head by shining a small light, such as a penlight, at an angle across the head surface. Look for accumulated foreign matter or head damage.

2. Inspect the drive capstan for accumulated foreign matter or damage.

3. If the tape head or capstan is damaged, replace the defective part.

4. To clean oxide and accumulated foreign matter from the head surface or the capstan, use a cotton swab moistened in isopropyl alcohol. Heavy or long-term accumulations may require repeated cleaning using a clean swab each time.

5. After cleaning all accumulated material from the head, use a clean, dry swab to remove the residue and polish the head.

TACHOMETER CLEANING

Once a month, visually inspect the optical tachometer. If the disk shows dirt or fingerprints, it should be cleaned with a soft, moist cloth. If the unit has a stainless steel tachometer disk instead of a nylon disk, it should be cleaned by brushing or blowing air across the surface where the slots are located. Remove all accumulated dust or dirt from the open areas; accumulated dust and dirt will cause speed stability problems.

TAPE MARK SENSOR CLEANING

Visual inspection of the emitter and sensor on the TMS assembly should be performed monthly. Use a soft brush or cotton swab to clean any accumulated dust or dirt from the lenses of there devices.

Packing Tapes

Tape should be cycled (wind and rewind) periodically. This packs the tape to maintain even tape tension and to prevent irregular stacking. Tape packing is especially important if the tape has been dropped or has undergone a significant temperature change, or if only a portion of the tape is used repeatedly.

Cartridge Tape Rethreading

Under unusual circumstances of drive failure or cartridge mishandling, the tape might come free of the hub. The tape is not fastened to the hub, but is held in place by the elastomer belt and by the tape's wrap around itself. The procedures for looping the tape back onto the hub help prevent important data loss, but they are no substitute for proper handling and customary back-up copying.

Two tools are required to rethread the cartridge tape: a number

Phillips head screwdriver and a small probe (a straightened paper clip can be used as a probe). Use the following procedure to rethread the cartridge tape:

CAUTION

Do not use magnetized tools; they will destroy the data on the tape (if staples or paper clips stick to the tool, it is magnetized). Also, do not touch the tape surface except at the end. Fingerprints cause errors.

1. Open the cartridge by removing the four baseplate Phillips head screws (see Figure 214-14), and set the cartridge upright on the work surface with the cover on.

2. Lift the cover free and set it aside.

NOTE

To remove the head gate, swing it out to clear the tape before lifting it up. It is not necessary to remove the head gate to perform this procedure.

3. Thread the end of the tape around the tape guides as shown in Figure 214-15.

4. Moisten the end of the tape with water to get it to stick to the hub.

5. With a small amount of slack at the free end, insert the end of the tape between the hub and belt. Turn the drive roller with a finger to take up the tape. When the tape is gripped between the hub and belt, maintain some tension on the tape so it feeds straight on the hub.

6. If the loose end of the tape separates from the hub as you continue to wind, tuck the end of the tape under the next turn of tape using the probe.

7. Hold the takeup hub and drive roller fixed, and rotate the supply reel to take up the slack.

8. Continue winding the tape about 20 turns before reassembling. Watch the tape holes and corner rollers so that they do not ride up the shaft and fall off.

9. To reinstall the tape head gate, perform the following steps:

   a. Align the long and short ends of the spring with the long and short ends of the gate (see Figure 214-16).
   b. Drop the spring into the well in the gate.
   c. Hold the spring down with the probe, and rotate the long end of the spring around to the slot that is at a right angle to the long dimension of the gate.
   d. Push the end of the spring into the slot; it should remain

there.

e. Hold the gate halfway out so that the gate and the spring end do not touch the tape. Slowly press the gate down onto its pin on the cartridge baseplate.

f. Reach in with the probe and press the spring down. It will clear its holding slot and snap into position, closing the gate.

10. Carefully lower the cartridge into place and reinstall the screws.

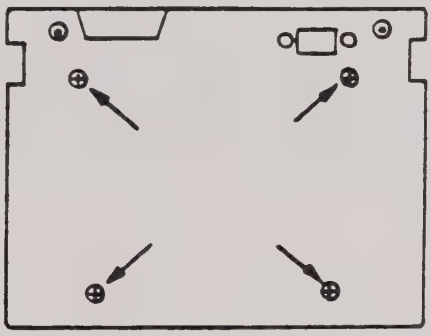


Figure 214-14. Cartridge Tape Screw Locations

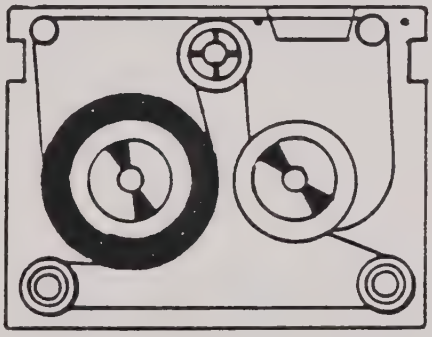


Figure 214-15. Cartridge Tape Threading

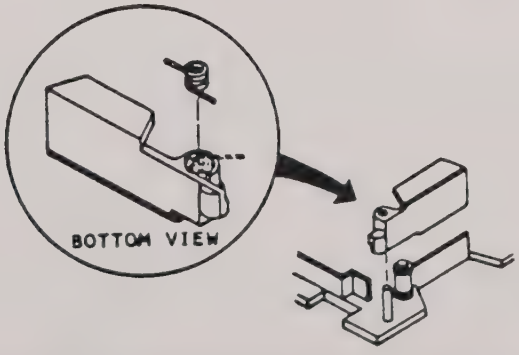


Figure 214-16. Catridge Tape Spring Installation

Performance Test

ENTERING AND RUNNING SYSTEM TESTS

1. Enter the System Test Menu from the Main Menu by pressing the "S" key. The Data Logger acknowledges with the prompt:

   <S> SYSTEM DIAGNOSTICS

2. Press the ENTER key. The prompt becomes:

   S: DEVICE TO TEST <1-7>? 1

   Now, the system is ready for you to choose a test from the System Test Menu. The seven system tests as they are shown on the Data Logger display are:

   S<1> CONTROLLER AND MEMORY
   S<2> KEYBOARD AND DISPLAY
   S<3> PORT A
   S<4> PORT B
   S<5> CARTRIDGE TAPE
   S<6> ADVANCED MATH PROCESSOR
   S<7> SERIAL LINK

3. Select the Cartridge Tape test by pressing the 5, followed by the ENTER key. Several test functions can be performed on the Cartridge Tape Drive. The prompt becomes:

   TEST <1-n>? 1

   The following tests may be run after selecting the Cartridge Tape Drive test (selection 5) from the test menu:

   <1> DEVICE/CONTROLLER I/F TEST

   This tests the internal communications between the Cartridge Tape Drive board and the Controller board.

   <2> ROM CHECKSUM

   This checks the ROM to see if the information contained in it is still correct.

<3> RAM TEST

This ensures that the cartridge interface RAM is completely functional by performing a sequential read after write at every RAM location.

<4> ENCODE/DECODE TEST

This verifies the operation of the encoding and decoding circuitry by routing the output of one into the input of the other and checking the result.

<5> TAPE DRIVE READ/WRITE

A tape cartridge must be inserted for this test. This test writes known blocks of data to the tape, reads the data from the tape, and compares the data read to the original data.

NOTE

The Tape Drive Read/Write test takes about 80 seconds to complete.

4. Select, by number, a particular test to be performed. When the selection has been made and ENTER is pressed, the prompt TEST IN PROGRESS is displayed. The test results are then displayed on the front panel, indicating that either the test was successful (TEST PASSED) or that it has failed (TEST FAILED). Some tests also provide other helpful prompts. To step through and acknowledge these results, press ENTER successively to view each test result response until there are no more. Press EXIT twice to return to the system test menu and obtain the following prompt:

S: DEVICE TO TEST <1-7>? _

5. If you do not wish to test another device, press the EXIT key. The Data Logger will execute a power-on sequence and return to the Main Menu.

Calibration Adjustment

INTRODUCTION

The following paragraphs contain calibration instructions for the Cartridge Tape Drive. Test equipment required for these procedures is listed in Table 214-1. In addition, at least one cartridge tape is required.

+12V POWER SUPPLY CALIBRATION

1. Open the data logger front panel and remove the Cartridge Interface PCA (refer to the access procedures in Section 4 of this manual).

2. Install the Cartridge Interface PCA on the Digital Extender PCA in the first slot to the left of the Controller PCA.

3. Connect the positive test lead of the DVM to TP16, and the negative lead to TP7.

4. Switch on data logger power, and adust R5 until the DVM reads +12.1 volts plus or minus 0.1000 volt. If R5 fails to adjust properly, repair the power supply before proceeding.

ADJUST TAPE TRAVEL SPEED

1. Connect the Cartridge Tape Drive cables to the Cartridge Interface PCA. (It may be necessary to remove the drive from the data logger to allow cables to reach.)

2. Put the write-protect tab on the tape cartridge is in the un-protected (record) position, and insert the tape cartridge in the tape drive.

3. Connect the oscilloscope to TP81. (Use TP1 as common.)

4. Turn on the data loger, and press the DATA TRANSFER key.

5. Select the cartridge as the source device, enter &#;%@&#;%@ as the file name, and enter 01 as the doy of the month for the start date selection (all other date parameters can be set to arbitrary values). Select an appropriate destination device.

6. The tape will be oriented to the load point and will wind foreward at a slow speed writing a continuous series of blocks on Track 1 until the end of the tape is reacned. It will then rewind at high speed to the load point and repeat the test.

7. Set the oscilloscope sweep speed at 50 microseconds per division.

8. Adjust R53 (located on the piggyback board) until the period of the displayed square wave is 250 microseconds plus or minus 20 microseconds.

9. The signal may display about 30 microseconds of edge jitter - this is acceptable. However, if the period varies much more than this or fails to adjust properly, then the speed control circuit on the Cartridge Interface is defective and needs to be repaired.

CHECK READ GAIN

1. Connect the scope probe to TP90 on the piggyback board of the Cartridge Interface PCA.

2. Set the sweep speed to 10 microseconds per division, and set the vertical amplifier to 2 volts per division, ac coupled.

3. The signal displayed should have a peak-to-peak amplitude of at least 7 volts. Some clipping is allowable.

4. You will notice two kinds of signal lobes - one about 10 microseconds wide (measured between zero crossings) with a slightly higher peak than the other, which is about 20 microseconds wide. The optimal

read gain is set when the 20 us lobe is just on the verge of clipping.

5. Read gain is adjusted with the variable resistor located on the lower board on the tape drive unit.

6. When the read gain adjustment has been made, eject the tape to shut down the test. This terminates the data transfer and should return the 2280A to the main menu.

7. Now, re-insert the tape and start a data transfer as before, except use "02" as the day-of-month for the start date. The cartridge will repeat the above test, except that now it will write blocks on Track 2. Verify that the signal at TP90 is approximately the same magnitude as it was on Track 1. Again, terminate this phase of the test by ejecting the tape.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the Cartridge Tape Drive is given in Table 214-3. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the Cartridge Tape Drive is given in Figure 214-17.

TABLE 214-3. 2280A-214 DC-100 CARTRIDGE TAPE DRIVE

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
		DC-100 TAPE DRIVE	646620	89536	646620	1		
A 9		CARTRIDGE TAPE I/F ASSEMBLY	737388	89536	737388	1		

TABLE 214-4. A9 CARTRIDGE TAPE I/F ASSEMBLY
(SEE FIGURE 214-20.)

REFERENCE DESIGNATOR A->NUMERICS---)	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOT -E
		CARTRIDGE ANALOG ASSEMBLY	753079	89536	753079	1		
C 1, 4, 6,		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	25		
C 10- 27, 29-			519157					
C 33, 35			519157					
C 2		CAP,AL,330UF,+100-10%,25V	614404	89536	614404	1		
C 3		CAP,CER,5000PF,+-20%,100V,Z5V	175232	56289	C023B101H253M	1		
C 5		CAP,AL,270UF,+100-10%,20V	602656	89536	602656	1		
C 7		CAP,CER,3300PF,+-5%,50V,COG	528554	89536	528554	1		
C 8		CAP,POLYES,0.047,+-10%,250V	162008	73445	C280MAE/A47K	1		
C 9		USE P/N 234492	357954	89536	357954	1		
C 23		CAP,AL,10UF,+-20%,35V	643296	74840	RLR-PX	1		
C 28		CAP,CER,33PF,+-2%,100V,COG	513226	51406	RPE121	1		
C 34		CAP,AL,47UF,+-20%,16V	643304	89536	643304	1		
CR 1	*	DIODE,SI, 50 PIV, 1.0 AMP	379412	04713	1N4933	1		
DS 1- 4	*	LED,RED,90 LEAD PREP,LUM INT=2MCD	604884	89536	604884	4	1	
‡J 38		CONN,POST,PWB,.025SQ,NON-INSUL,GOLD30	543538	00779	543538	1		
J 46		HEADER,DUAL ROW,.100 CTRS,26 POS	603662	89536	603662	1		
L 1		CHOKE	490870	89536	490870	1		
MP 1		EJECTOR,PCB .062,	706879	89536	706879	1	1	
MP 2		BAG,SHIELDING,TRANSPARENT,12"X16"	680983	89536	680983	1		
MP 3		SPACER,PWB,SNAP-IN,PLASTIC,0.500	655076	89536	655076	4		
MP 4		HEATSINK	428805	13103	6046P8	1		
Q 1	*	SILICON, NPN, FAST SWITCHING D44H11	535542	89536	535542	1	1	
Q 2, 3	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	195974	64713	2N3906	2	1	
R 1		RES,CF,160,+-5%,0.25W	441410	80031	CR251-4-5P160E	1		
R 2		RES,CF,51,+-5%,0.25W	414540	80031	CR251-4-5P51E	1		
R 3		RES,CF,68,+-5%,0.25W	414532	80031	CR251-4-5P68E	1		
R 4, 8		RES,MF,3.01K,+-1%,0.125W,100PPM	312645	91637	CMF553011F	2		
R 5		RES,VAR,CERM,1K,+-10%,0.5W	285155	71450	360S102A	1		
R 6		RES,MF,7.15K,+-1%,0.125W,100PPM	260356	91637	CMF557151F	1		
R 7		RES,CF,3K,+-5%,0.25W	441527	80031	CR251-4-5P3K	1		
R 9		RES,MF,3.92K,+-1%,0.125W,100PPM	294801	91637	CMF553921F	1		
R 10		RES,MF,1.02K,+-1%,0.125W,100PPM	223545	91637	CMF551021F	1		
R 11		RES,CF,100K,+-5%,0.25W	348920	80031	CR251-4-5P100K	1		
R 12		RES,CF,3.9K,+-5%,0.25W	342600	80031	CR251-4-5P3K9	1		
R 13- 15, 19,		RES,CF,22K,+-5%,0.25W	348870	80031	CR251-4-5P22K	9		
R 25, 31, 32,			348870					
R 34, 35			348870					
R 16, 32		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	2		
R 20		RES,CF,2K,+-5%,0.25W	441469	80031	CR251-4-5P2K	1		
R 21		RES,CF,22,+-5%,0.25W	381145	80031	CR251-4-5P22E	1		
R 22		RES,CF,220,+-5%,0.25W	342626	80031	CR251-4-5P220E	1		
R 23		RES,CF,1.2K,+-5%,0.25W	441378	80031	CR251-4-5P1K2	1		
R 24, 33		RES,CF,10,+-5%,0.25W	340075	80031	CR251-4-5P10E	2		
R 26		RES,CF,1K,+-5%,0.25W	343426	80031	CR251-4-5P1K	1		
R 27- 30		RES,CF,510,+-5%,0.25W	441600	80031	CR251-4-5P510E	4		
‡T 1, 7, 10,		CONN,TAB,FASTON,PRESS-IN,0.110 WIDE	512889	02660	62395	20		
‡T 12, 16, 17,			512889					
‡T 70- 82			512889					
U 1	*	IC,REGULATING PULSE WIDTH MODULATOR	454678	01295	SG3524N	1	1	
U 2	*	IC,CMOS,QUAD 2 INPUT OR GATE	408393	02735	CD4071BE	1	1	
U 3, 13	*	IC,LSTTL,OCTL BUFFER W/3-ST&NOR ENABL	429902	12040	DM81LS95N	2	1	
U 4	*	IC,LSTTL,OCTAL INV BFR W/3-STATE OUT	453324	12040	DM81LS98N	1	1	
U 5, 45, 46,	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,W/CLEAR	454892	01295	SN74LS273N	4	1	
U 64	*		454892					
U 6, 39	*	IC,CMOS,HEX INVERTER	404681	02735	CD4069BE	2	1	
U 7, 29	*	IC,DUAL DIV BY 16 BINARY COUNTER	483578	01295	SN74LS393N	2	1	
U 8, 36, 42	*	IC,LSTTL,DUAL JK F/F,W/SEP CLKS&CLRS	393157	01295	SN74LS107N	3	1	
U 9, 61	*	IC,CMOS,8STAGE SYNC PRSET DWN BIN CNT	508689	02735	CD40103BE	2	1	
U 10, 19, 38,	*	IC,CMOS,DUAL D F/F,+EDG TRG W/SET&RST	536433	04713	MC4013BCP	5	1	
U 41, 60	*		536433					
U 11, 53	*	IC,LSTTL,QUAD 2 INPUT NAND GATE	393033	01295	SN74LS00N	2	1	
U 12, 47	*	IC,TTL,OCTAL D F/F,+EDG TRG	473223	01295	SN74LS374N	2	1	
U 14	*	IC,LSTTL,HEX INVERTER W/SCHMT TRIG	483180	01295	SN74LS14N	1	1	
U 15	*	IC,LSTTL,DUAL 2-4 LINE DCDR/DRVR	393199	01295	SN74LS155N	1	1	
U 16, 22, 67	*	IC,LSTTL,DUAL D F/F,+EDG TRG,W/CLR	393124	01295	SN74LS74N	3	1	
U 17	*	IC,LSTTL,QUAD 2 INPUT NOR GATE	393041	01295	SN74LS02N	1	1	
U 18, 59	*	IC,CMOS,QUAD D F/F,+EDG TRG	536292	04713	MC14175B	2	1	
U 20, 58	*	IC,CMOS,QUAD 2 INPUT AND GATE	408401	02735	CD4081BE	2	1	
U 21		OSCILLATOR,8MHZ,TTL CLOCK	584169	09969	X0-33D-15-8-MHZ	1	1	
U 23, 55	*	IC,LSTTL,DUAL J-K F/F,+EDG TRIG	412999	01295	SN74LS109N	2		
U 24, 25	*	IC,LSTTL,QUAD D F/F,+EDG TRG,W/CLR	393215	01295	SN74LS175N	2	1	
U 26	*	IC,LSTTL,QUAD 2 INPUT OR GATE	393108	01295	SN74LS32N	1	1	
U 27	*	IC,CMOS,PRESETTABLE DIV BY N COUNTER	478313	02735	CD4018BE	1	1	

TABLE 214-4. A9 CARTRIDGE TAPE I/F ASSEMBLY
(SEE FIGURE 214-20.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOT -E
U 28, 30	*	IC,LSTTL,SYNC DIVIDE BY 16 BIN CNTR	393231	01295	SN74LS193N	2	1	
U 31	*	IC,FTTL,HEX INVERTER	634444	07235	74F04PC	1	1	
U 32		IC,NMOS,PARALLEL I/O CONTROLLER	536920	89536	536920	1		
U 33	*	IC,NMOS,8 BIT MICROCOMPUTER	478073	50088	MK3880-4CPU	1	1	
U 34		IC,16K X 8 EPROM (PROGRAMMED)	753087	89536	753087	1		
U 35	*	IC,LSTTL,2 2-IN/3 3-IN AOI GATES	412981	01295	SN74LS51N	1	1	
U 37	*	IC,CMOS,DUAL 4BIT SER-IN,PAR-OUT SHFT	340125	04713	MC14015CP	1	1	
U 40	*	IC,TTL,HEX INVERTER W/OPEN COLLECTOR	288605	01295	SN7416N	1	1	
U 43	*	IC,CMOS,8BIT PAR/SER-I/O SHIFT RGS	380766	02735	CD4021AE	1	1	
U 44		IC,2K X 8 STAT RAM	584144	89536	584144	1		
U 48	*	IC,LSTTL,TRIPLE 3 INPUT NAND GATE	393074	01295	SN74LS10N	1	1	
U 49	*	IC,LSTTL,TRIPLE 3 INPUT AND GATE	393082	04713	SN74LS11N	1	1	
U 50	*	IC,CMOS,QUAD AND-OR SELECT GATE	419010	02735	CD4019AE	1	1	
U 51	*	IC,LSTTL,SYNC DIV BY 16 BINARY COUNTR	495598	01295	SN74LS163N	1	1	
U 52, 56	*	IC,TTL,QUAD 2 INPUT AND GATE	393066	01295	SN74LS08N	2	1	
U 54	*	IC,TTL,QUAD 2 INPUT XOR GATE	408237	01295	SN74LS86N	1	1	
U 57	*	IC,CMOS,DUAL JK F/F,+EDG TRIG	355230	02735	CD4027AE	1	1	
U 62		IC,TTL,CRC GENERATOR/CHECKER	605287	89536	605287	1		
U 63	*	IC,VOLT REG,FIXED,+12 VOLTS,1.5 AMPS	428854	04713	MC7812CT	1	1	
U 65, 66	*	IC,LSTTL,4 BIT BINARY FULL ADDER	408740	01295	SN74LS283N	2	1	
XU 32, 33		SOCKET,DIP,0.100 CTR,40 PIN	429282	09922	DILB40P-108	2		
XU 34		SOCKET,DIP,0.100 CTR,28 PIN	448217	91506	328-AG39D	1		
XU 44		SOCKET,DIP,0.100 CTR,24 PIN	376236	91506	324-AG39D	1		
XU 47, 62		SOCKET,DIP,0.100 CTR,14 PIN	370304	09922	DILB14P-108	2		
Z 1		RES,NET,DIP,14 PIN,7 RES,1K,+-5%	407445	01121	314	1		
Z 2		RES,NET,DIP,16 PIN,8 RES,1K,+-5%	358119	01121	314	1		
Z 3- 8		RES,NET,SIP,10 PIN,9 RES,22K,+-2%	574442	89536	574442	6		
Z 9		RES,NET,SIP,8 PIN,7 RES,22K,+-2%	500041	89536	500041	1		

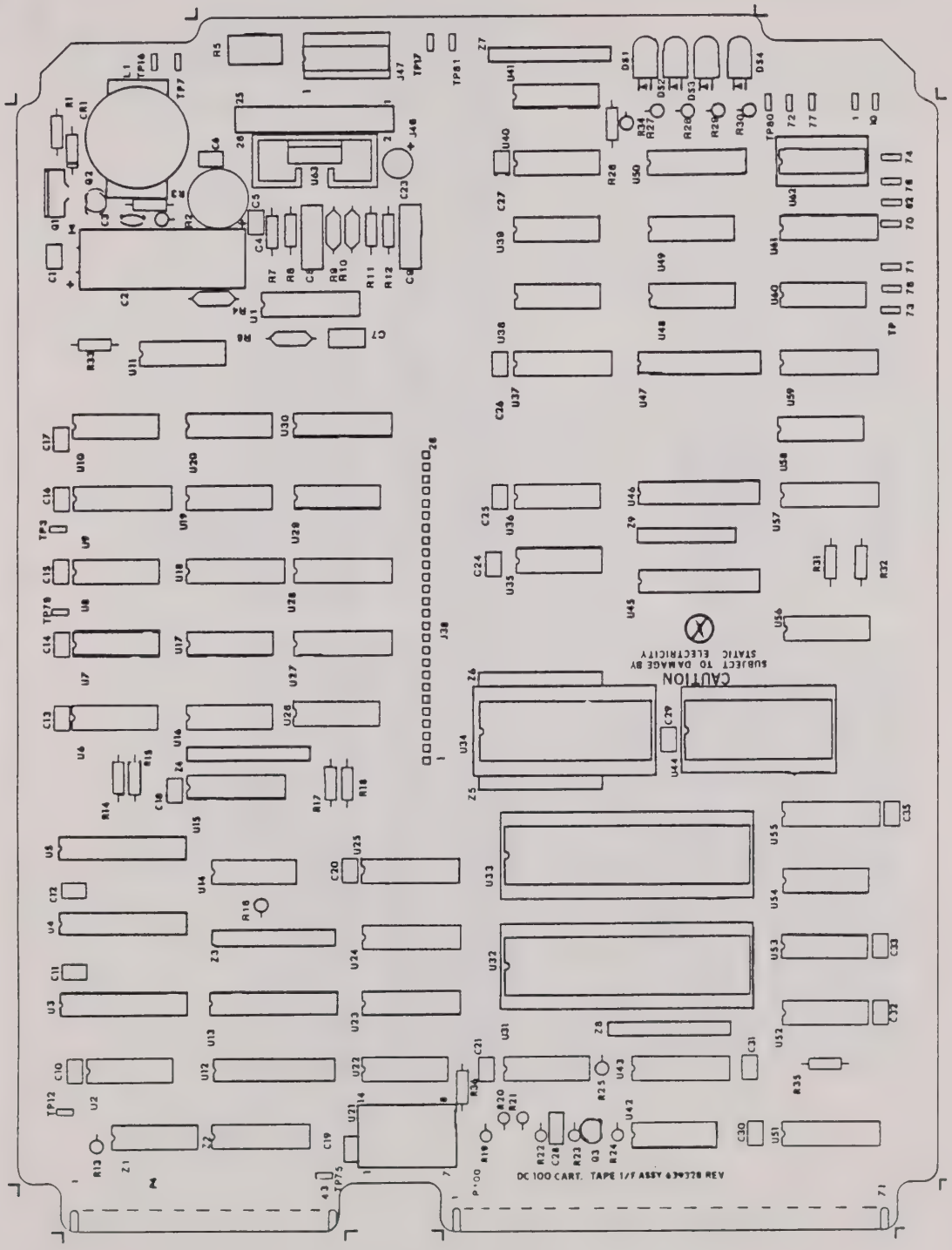
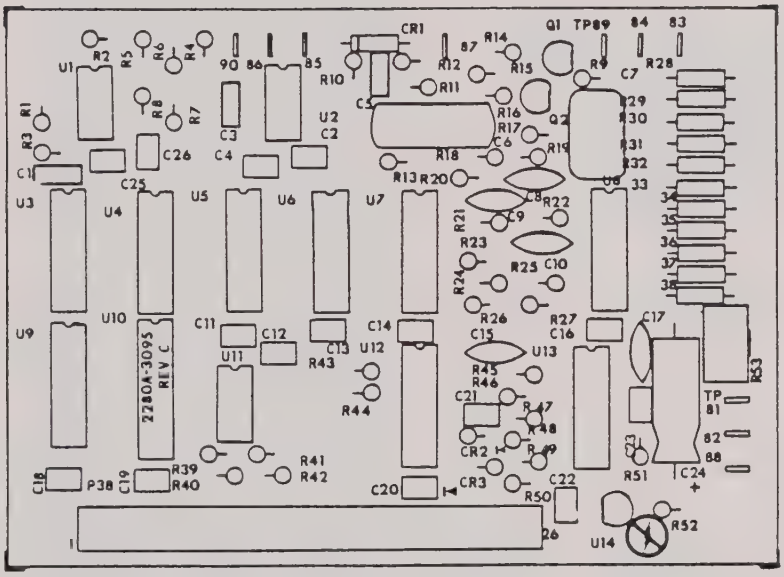


Figure 214-20. A9 Cartridge Tape I/F Assembly

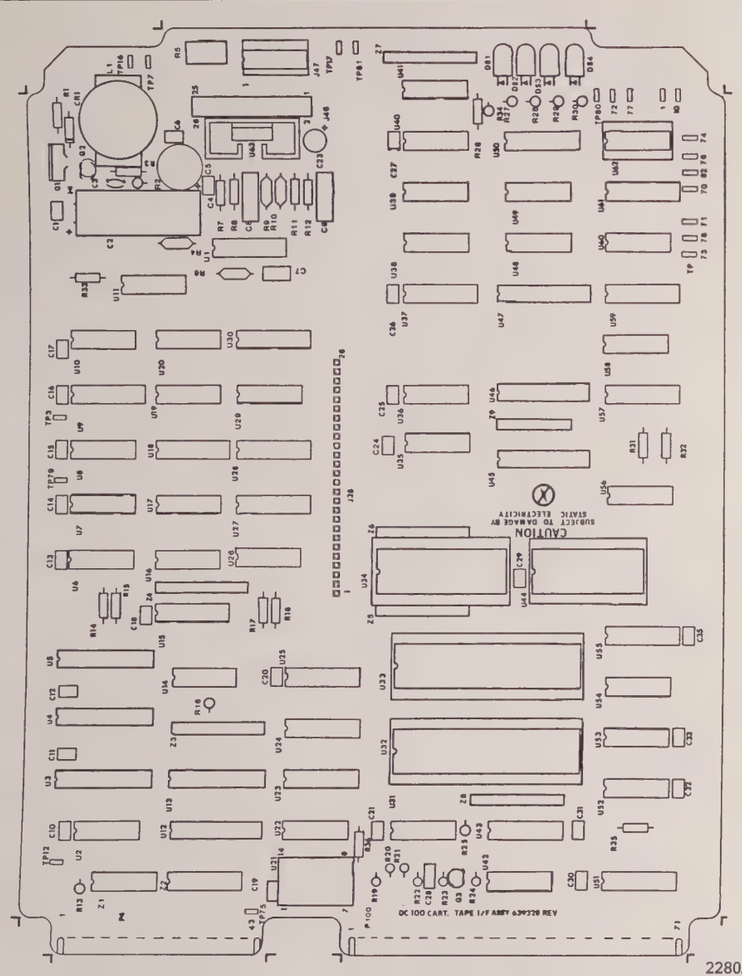
TABLE 214-5. CARTRIDGE ANALOG PCA
(SEE FIGURE 214-21.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOT -E
C 1, 5		CAP,CER,150PF,+-2%,100V,COG	512988	89536	512988	2		
C 2, 4, 11-		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	15		
C 14, 16, 18-			519157					
C 23, 25, 26			519157					
C 6		CAP,POLYES,0.47UF,+-10%,100V	369124	89536	369124	1		
C 7		CAP,POLYES,0.1UF,+-10%,200V	271973	89536	271973	1		
C 8, 10, 15,		CAP,CER,0.01UF,+80-20%,25V,Y5U	335786	72982	5835-000Y5-U103Z	4		
C 17			335786					
C 9		CAP,CER,500PF,+-10%,1000V,X5R	105692	71590	2DDH60N501K	1		
C 24		CAP,AL,47UF,+75-20%,25V	655191	89536	655191	1		
CR 1	*	DIODE,GER,BV=100.0V,IO= 80MA,80 MW	149187	93332	1N270	1	1	
CR 2, 3	*	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	2		
P 38		SOCKET,1 ROW,PWB,0.100CTR,13 POS	513390	27264	22-17-2132	2	1	
Q 1	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	1	1	
Q 2	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	195974	64713	2N3906	1	1	
R 1		RES,CF,62K,+-5%,0.25W	348904	80031	CR251-4-5P62K	1		
R 2, 50		RES,CF,20K,+-5%,0.25W	441477	80031	CR251-4-5P20K	2		
R 3		RES,CF,3.9K,+-5%,0.25W	342600	80031	CR251-4-5P3K9	1		
R 4		RES,CF,39K,+-5%,0.25W	442400	80031	CR251-4-5P39K	1		
R 5, 10, 44,		RES,CF,1K,+-5%,0.25W	343426	80031	CR251-4-5P1K	4		
R 46			343426					
R 6		RES,CF,3K,+-5%,0.25W	441527	80031	CR251-4-5P3K	1		
R 7		RES,CF,510K,+-5%,0.25W	442491	80031	CR251-4-5P510E	1		
R 8		RES,CF,2.2K,+-5%,0.25W	343400	80031	CR251-4-5P2K2	1		
R 9, 14, 15		RES,CF,5.1K,+-5%,0.25W	368712	80031	CR251-4-5P5K1	3		
R 11		RES,CF,11K,+-5%,0.25W	441360	80031	CR251-4-5P11K	1		
R 12		RES,CF,1.2K,+-5%,0.25W	441378	80031	CR251-4-5P1K2	1		
R 13		RES,CF,7.5K,+-5%,0.25W	441667	80031	CR251-4-5P7K5	1		
R 16, 17		RES,CF,680,+-5%,0.25W	368779	80031	CR251-4-5P200E	2		
R 18- 20		RES,MF,10K,+-1%,0.125W,100PPM	168260	91637	CMF551002F	3		
R 21		RES,MF,56.2K,+-1%,0.125W,100PPM	271346	91637	CMF555622F	1		
R 22, 24, 26,		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	7		
R 37, 38, 43,			348839					
R 45			348839					
R 23, 36		RES,CF,22K,+-5%,0.25W	348870	80031	CR251-4-5P22K	2		
R 25, 27		RES,MF,1K,+-1%,0.125W,100PPM	168229	91637	CMF551001F	2		
R 28- 33		RES,CF,2.4K,+-5%,0.25W	441493	80031	CR251-4-5P2K4	6		
R 34, 35		RES,CF,51K,+-5%,0.25W	376434	80031	CR251-4-5P51K	2		
R 39		RES,MF,11.3K,+-1%,0.125W,100PPM	293639	91637	CMF551132	1		
R 40		RES,MF,1.87K,+-1%,0.125W,100PPM	267229	91637	CMF551871F	1		
R 41		RES,MF,143,+-1%,0.125W,100PPM	192906	91637	CMF551430F	1		
R 42		RES,MF,866,+-1%,0.125W,100PPM	248641	89536	248641	1		
R 47		RES,CF,47K,+-5%,0.25W	348896	80031	CR251-4-5P47K	1		
R 48		RES,CF,300K,+-5%,0.25W	441535	80031	CR251-4-5P300K	1		
R 49		RES,CF,1.5M,+-5%,0.25W	349001	80031	CR251-4-5P1M5	1		
R 51		RES,CF,200,+-5%,0.25W	441451	80031	CR251-4-5P200E	1		
R 52		RES,CF,30K,+-5%,0.25W	368753	80031	CR251-4-5P30K	1		
R 53		RES,VAR,CERM,20K,+-10%,0.5W	291609	89536	291609	1		
TP 81- 90		TERM,FASTON,TAB,SOLDR,0.110 WIDE	512889	02660	62395	10		
U 1, 2	*	IC,COMPARATOR,8 PIN DIP	352195	01295	SN72311P	2	1	
U 3	*	IC,LSTTL,DUAL JK F/F,W/SEP CLKS&CLRS	393157	01295	SN74LS107N	1	1	
U 4	*	IC,TTL,QUAD 2 INPUT XOR GATE	408237	01295	SN74LS86N	1	1	
U 5	*	IC,TTL,QUAD 2 INPUT AND GATE	393066	01295	SN74LS08N	1	1	
U 6	*	IC,TTL,DUAL JK F/F W/SEP CLKS & CLRS	293043	01295	SN74107N	1	1	
U 7	*	IC,CMOS,QUAD BILATERAL SWITCH	605329	04713	MC14016BCP	1	1	
U 8, 13	*	IC,OP AMP,QUAD,14 PIN DIP	402669	12040	LM324N	2	1	
U 9	*	IC,DUAL DIV BY 16 BINARY COUNTER	483578	01295	SN74LS393N	1	1	
U 10	*	IC,LSTTL,SYNC DIV BY 16 BINARY COUNTR	495598	01295	SN74LS163N	1	1	
U 11	*	IC,OP AMP,JFET INPUT,8 PIN DIP	472779	12040	LF386N	1	1	
U 12	*	IC,TTL,HEX BUFFER W/OPEN COLLECTOR	328021	01295	SN7417N	1	1	
U 14	*	IC,VOLT REG,FIXED,+6 VOLTS,0.1 AMPS	507434	12040	LM78L6.0ACZ	1	1	

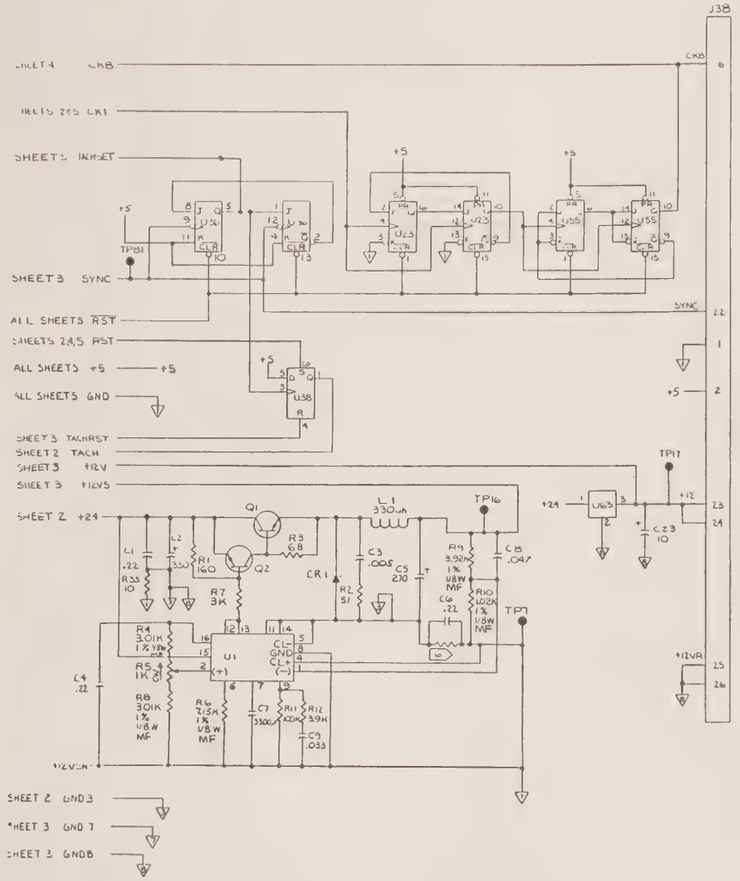


2280A-1695

Figure 214-21. Cartridge Analog PCA



2280A-1614

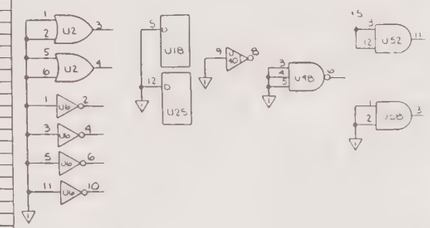


POWER & GROUND TABLE		
REF DES	GND	+5
U1	—	—
U2	7	14
U3	10	20
U4	10	20
U5	10	20
U6	7	14
U7	7	14
U8	7	14
U9	8	16
U10	7	14
U11	7	14
U12	10	20
U13	10	20
U14	7	14
U15	8	16
U16	7	14
U17	7	14
U18	8	16
U19	7	14
U20	7	14
U21	7	14
U22	7	14
U23	8	16
U24	8	16
U25	8	16
U26	7	14
U27	8	16
U28	8	16
U29	7	14
U30	8	16
U31	7	4
U32	11	20
U33	29	11
U34	14	1,26,27,28
U35	7	14
U36	7	14
U37	8	16
U38	7	14
U39	7	14
U40	7	14
U41	7	14
U42	7	14
U43	8	16
U44	12	24
U45	10	20
U46	10	20
U47	10	20
U48	7	14
U49	7	14
U50	8	16
U51	8	16
U52	7	14
U53	7	14
U54	7	14
U55	8	16
U56	7	14
U57	8	16
U58	7	14
U59	8	16
U60	7	14
U61	8	16
U62	7	14

NOTES. UNLESS OTHERWISE SPECIFIED

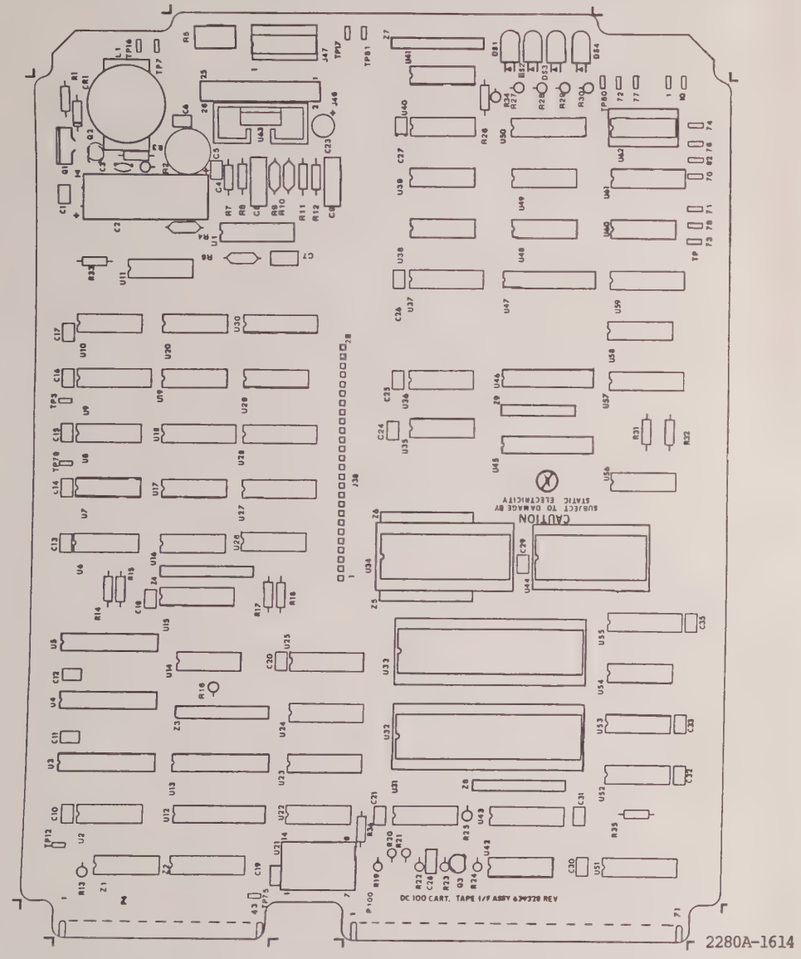
1. ALL RESISTANCES ARE IN OHMS & ALL CAPACITANCES ARE IN MICROFARADS.
2. ALL RESISTORS ARE 1/4W, 5%.
3. ALL GRAPHIC SYMBOLS ARE IN ACCORDANCE WITH ANSI Y32.2 & Y32.14.

(6) THIS RESISTOR IS A TRACE ON PCB.

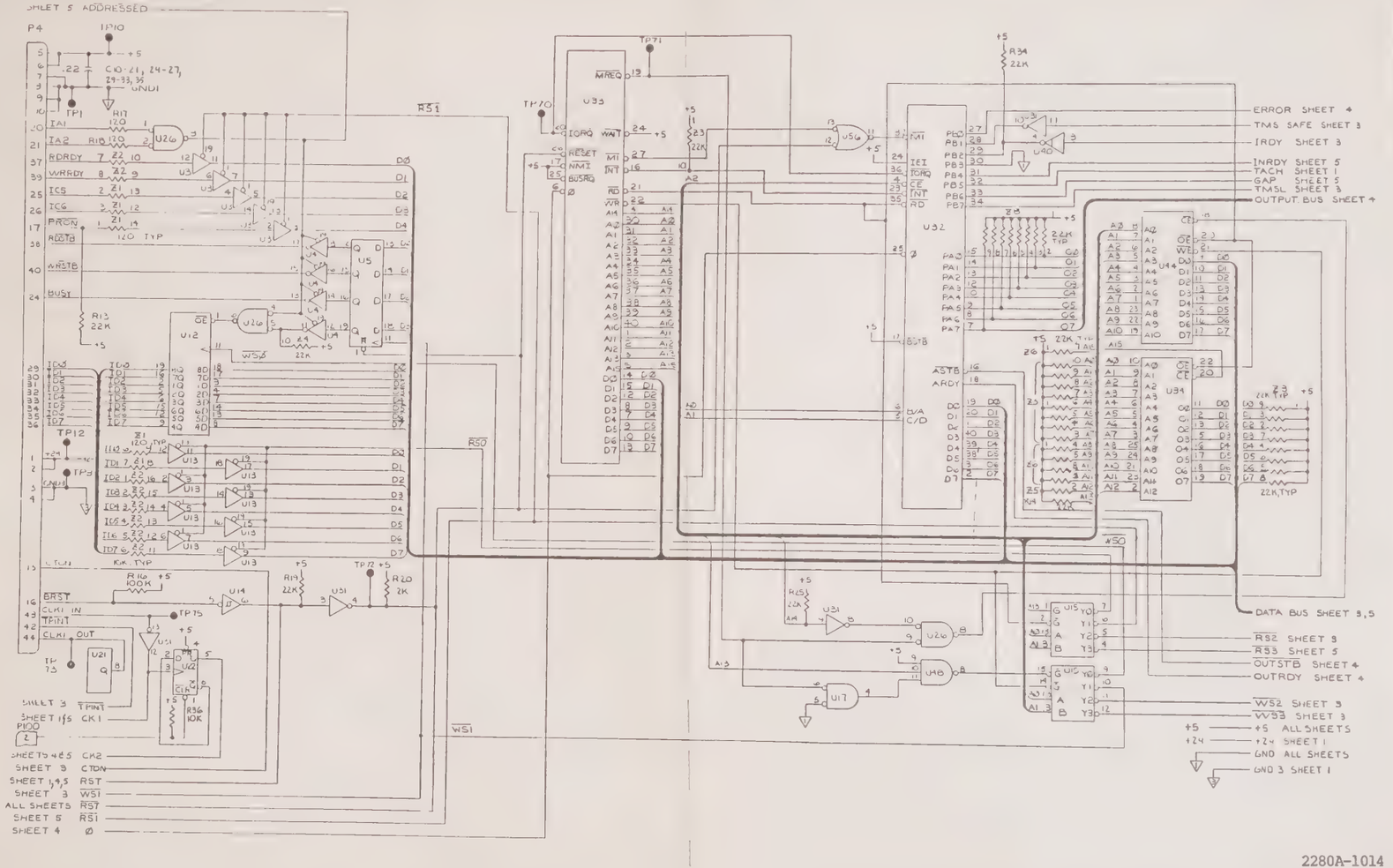


2280A-1014

Figure 214-20. Cartridge Tape Drive Schematic Diagram


CAUTION
SUBJECT TO DAMAGE BY STATIC ELECTRICITY
DC 100 CART. TAPE I/F ASSY 63W328 REV

2280A-1614


SHEET 5 ADDRESSED
P4
P100
U26
U12
U5
U32
U33
U34
U35
U36
U37
U39
U44
U56
U57
U58
U59
U60
U61
U62
U63
U64
U65
U66
U67
U68
U69
U70
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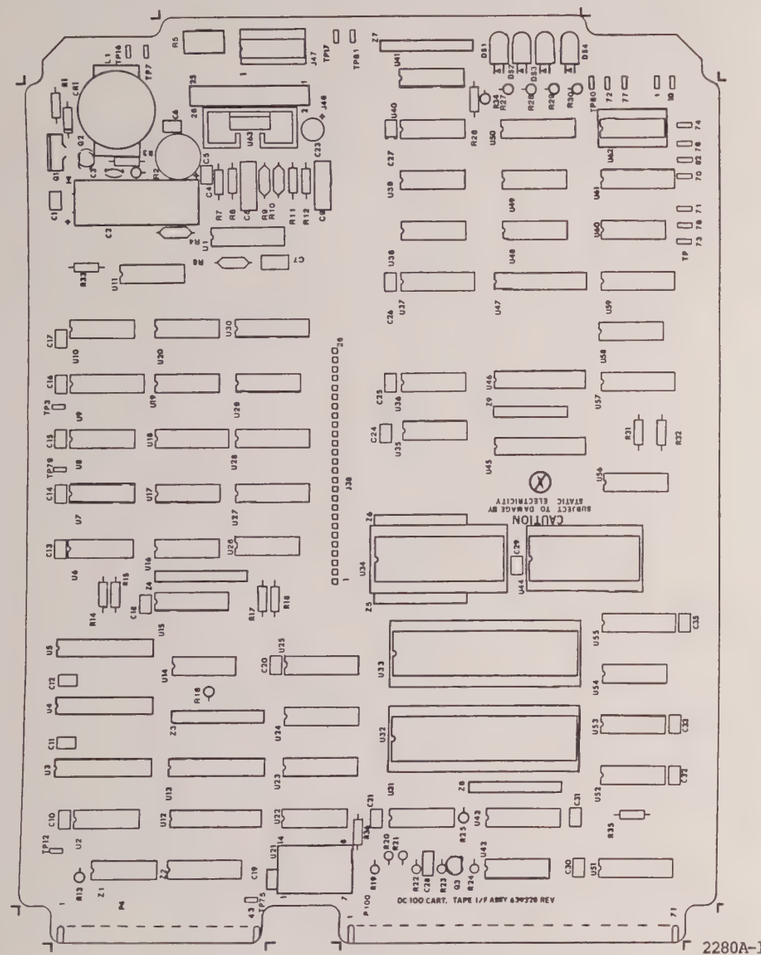
U86
U87
U88
U89
U90
U91
U92
U93
U94
U95



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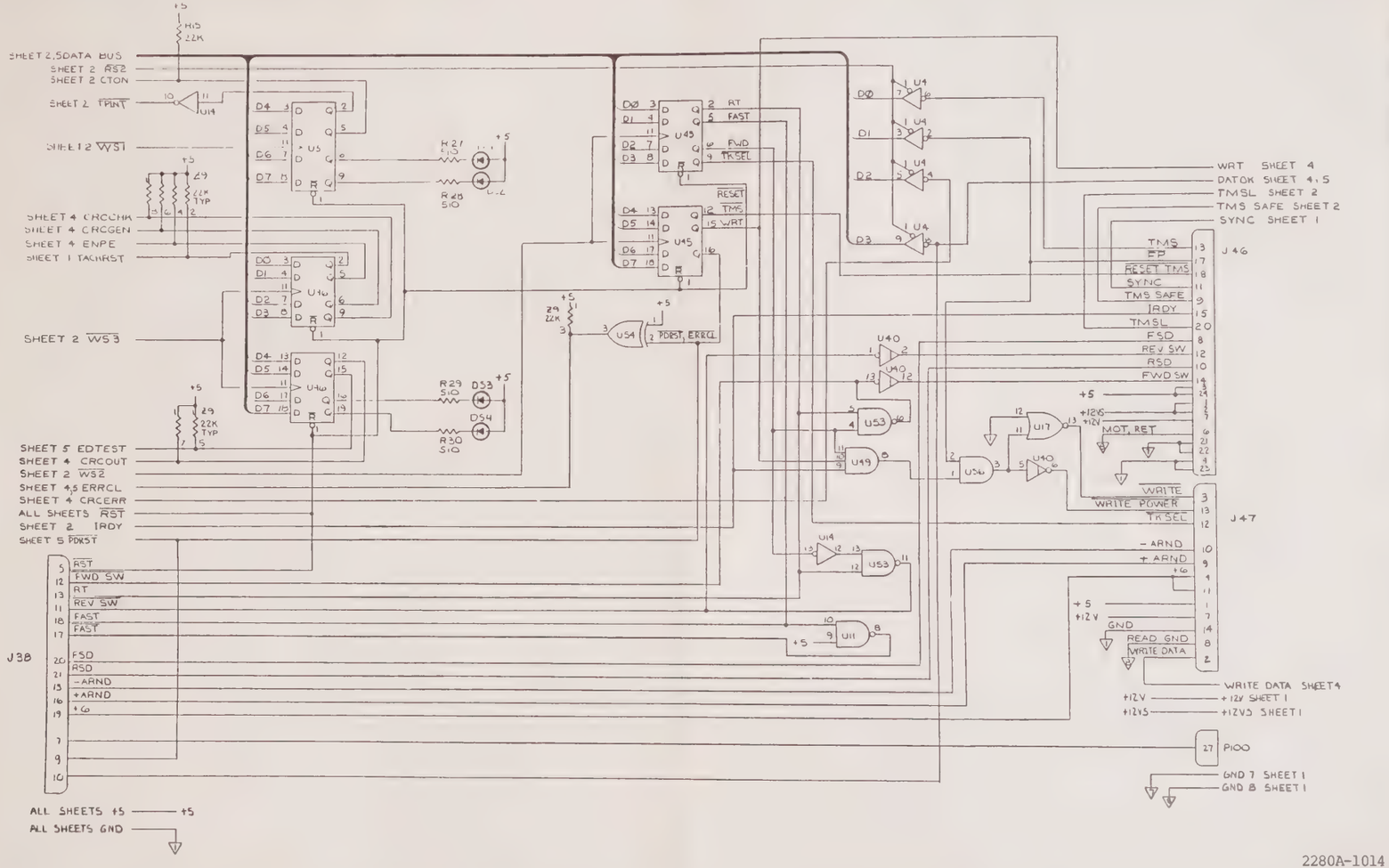
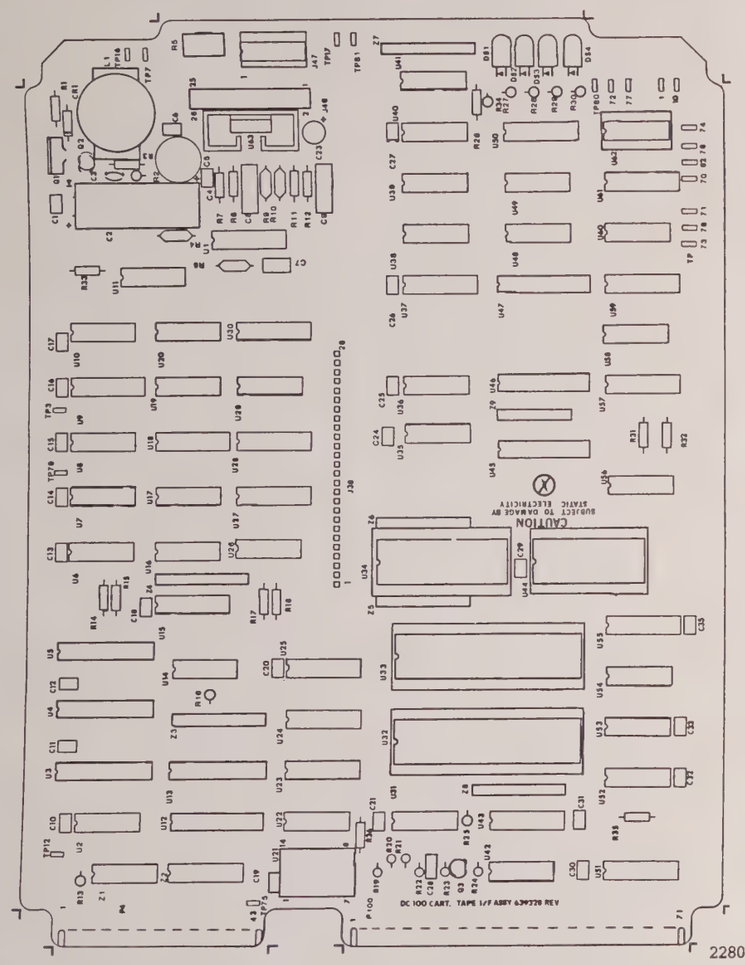


2280A-1014

Figure 214-20. Cartridge Tape Drive Schematic Diagram (cont.)



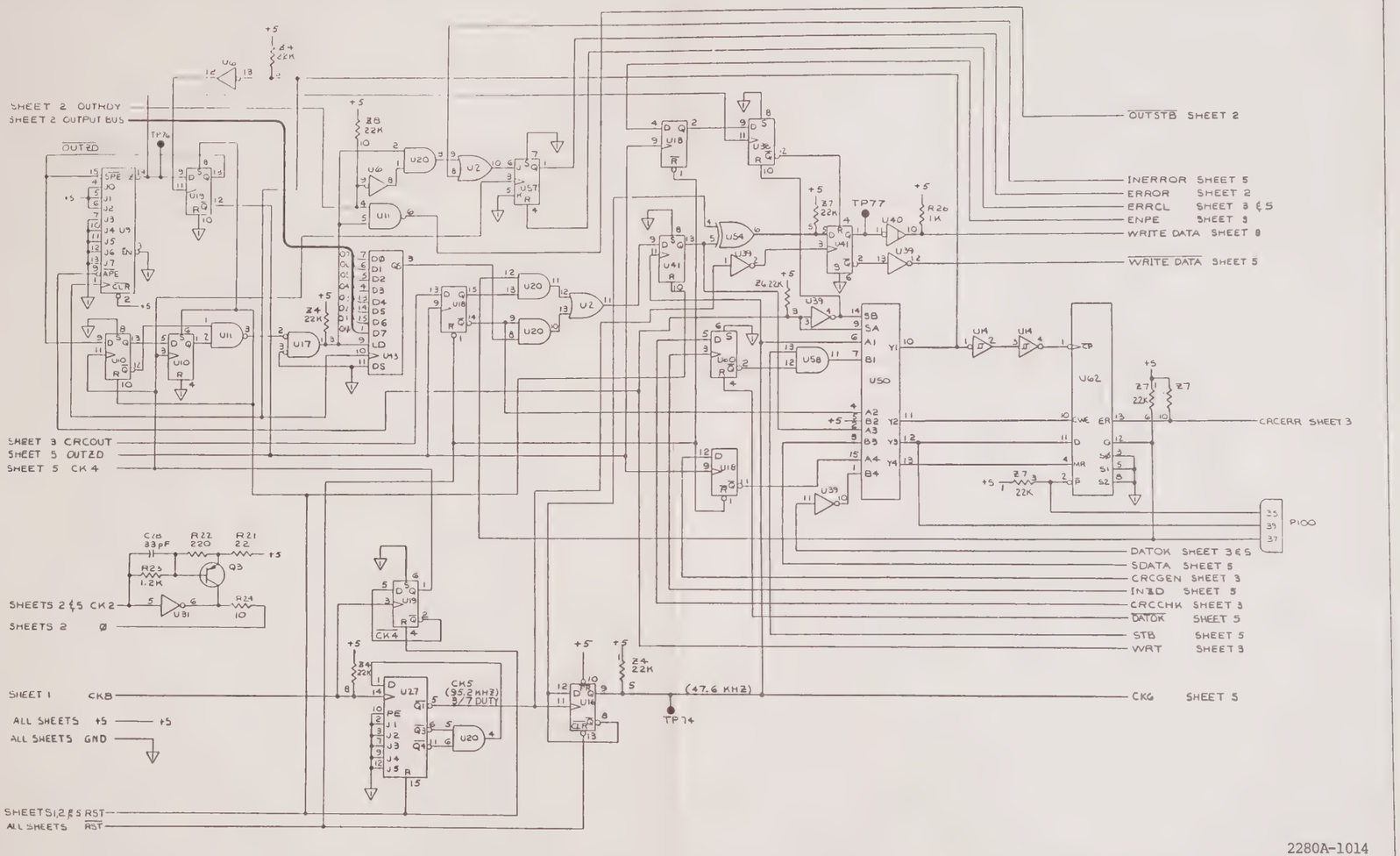
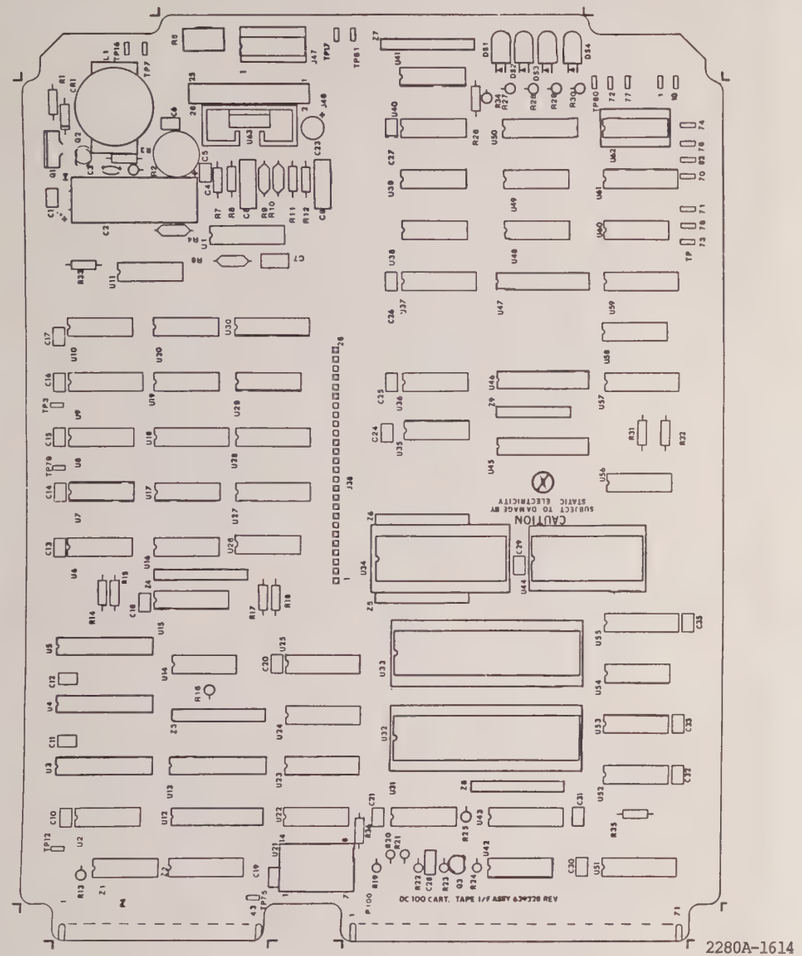
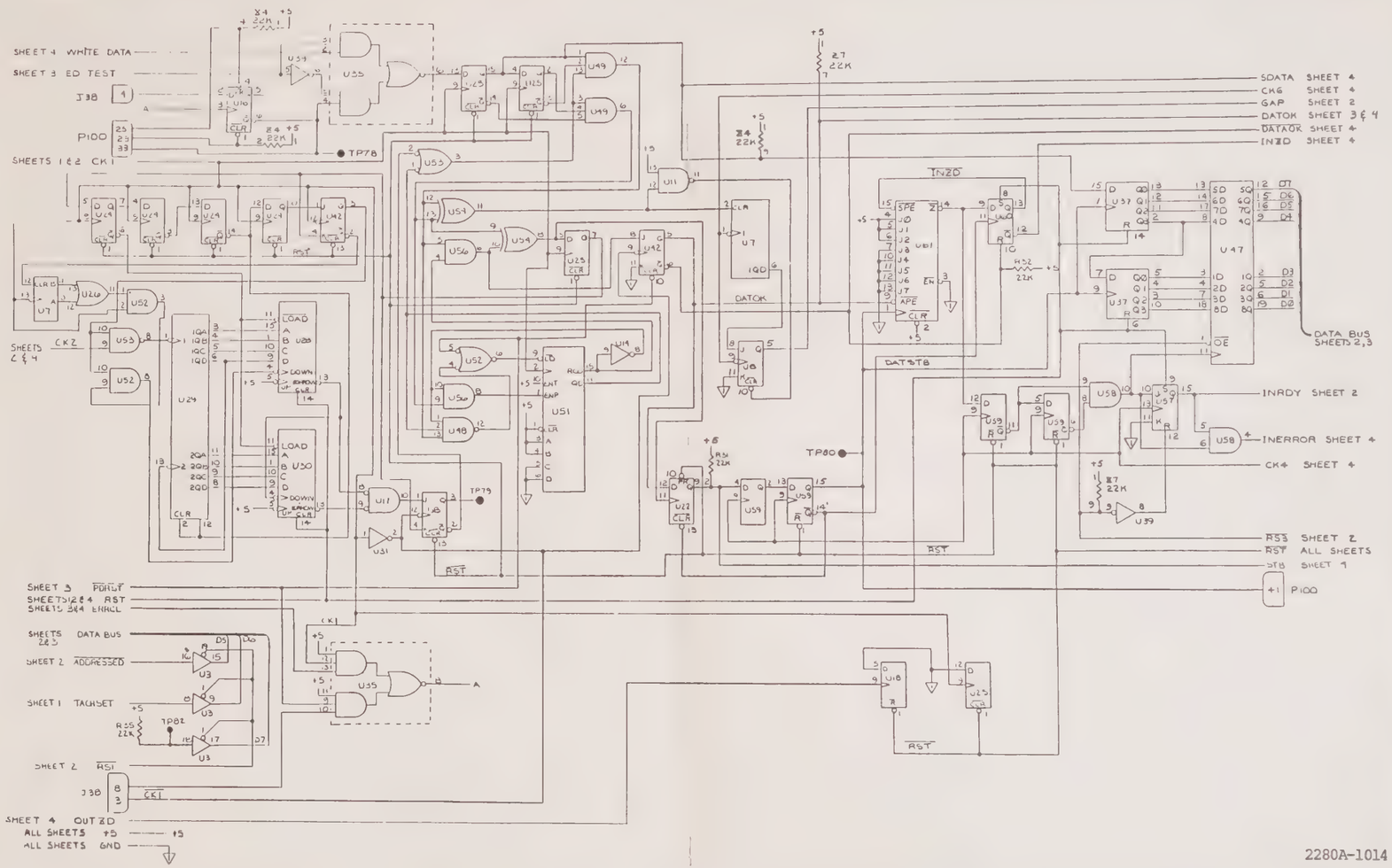


Figure 214-20. Cartridge Tape Drive Schematic Diagram (cont.)

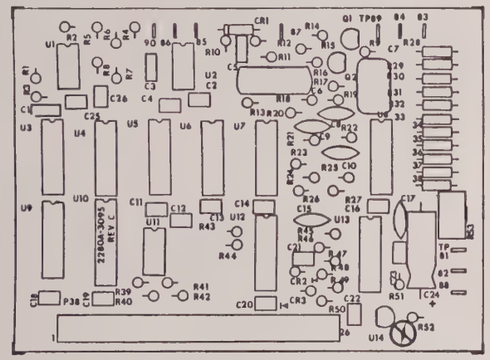


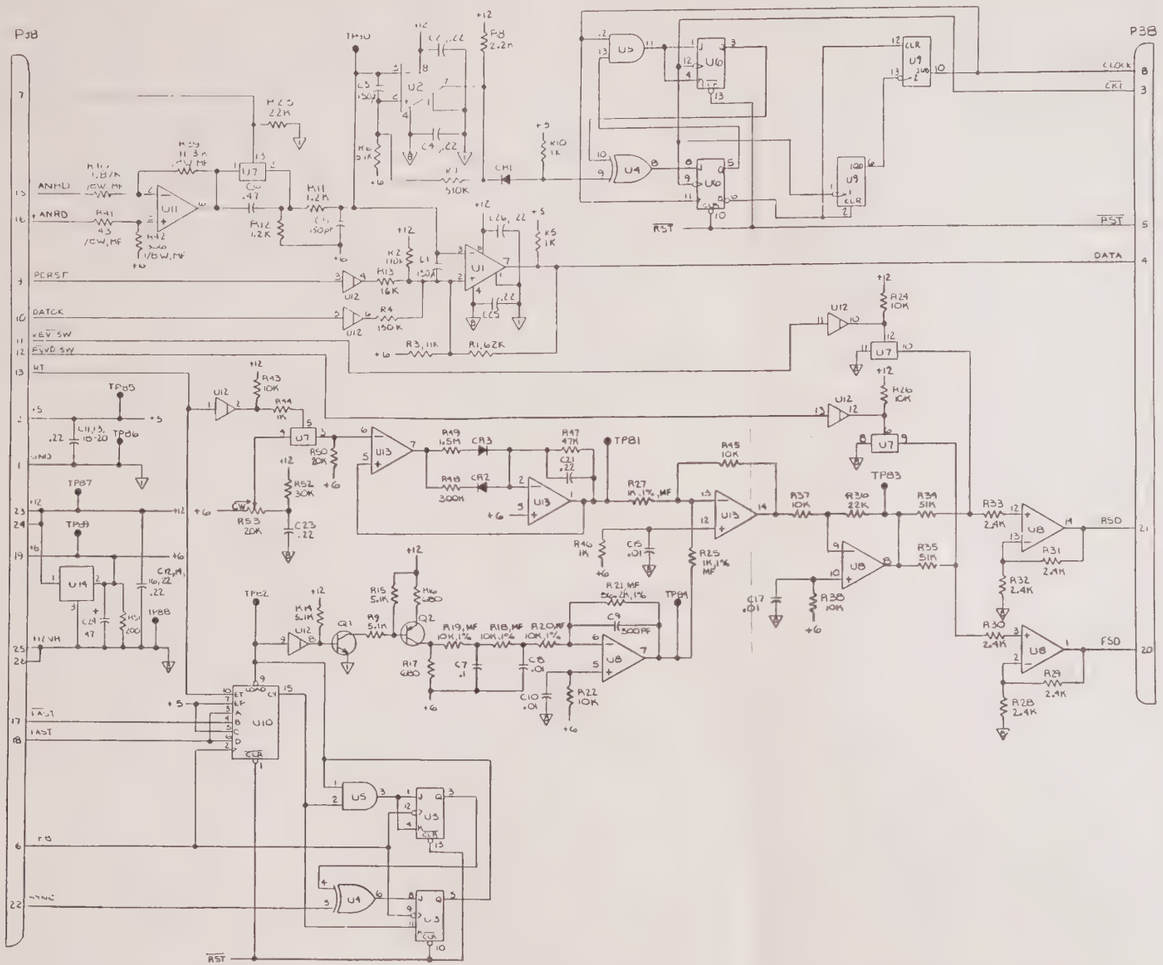
2280A-1614



2280A-1014

Figure 214-20. Cartridge Tape Drive Schematic Diagram (cont.)





I.C.	+5	+12	GND1	GND 8	NO. PIN
U1		5,6			8
U2		5,6			8
U3	14		7		14
U4	14		7		14
U5	14		7		14
U6	14		7		14
U7		14		7	14
U8		4		11	14
U9	14		7		14
U10	16		8		16
U11		7		4	8
U12	14		7		14
U13		4		11	14
U14					
U					

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE IS IN OHMS.
2. ALL RESISTORS ARE 1/4W, 5%.
3. ALL CAPACITANCES IS IN MICROFARADS.

Figure 214-20. Cartridge Tape Drive Schematic Diagram (cont.)

Option 2280A-341
RS-232-C Interface

DESCRIPTION

The RS-232-C Interface option provides a communications link between the Data Logger and another EIA Standard RS-232-C compatible device. The RS-232-C Interface can be installed in either the Port A or Port B position in the rear of the Data Logger mainframe.

When installed in Port A, the RS-232-C Interface provides a bi-directional communications link that allows remote programming and operation of the Data Logger. When the interface is installed in Port B, the Data Logger can only use it to output data. Figure 341-1 illustrates the RS-232-C Interface.

WHERE TO FIND ADDITIONAL INFORMATION

In this subsection are RS-232-C Interface theory of operation, general maintenance, performance tests, a parts list, and a schematic diagram. Installation and system configuration instructions are in the 2280 Series System Guide, and operation and programming instructions are in the 2280 Series User Guide. Option specifications are in the appendices in this manual and the System Guide.

The test equipment required to perform the procedures in this subsection is listed in Table 341-1. A summary of test equipment required for all procedures in this manual is given in Table 1-1 in Section 1 of this manual.

Table 341-1. Required Test Equipment

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
RS-232-C Terminal	Full Duplex Capability	Any
*Digital PCA Extender Fixture	.....	Fluke Part # 486910

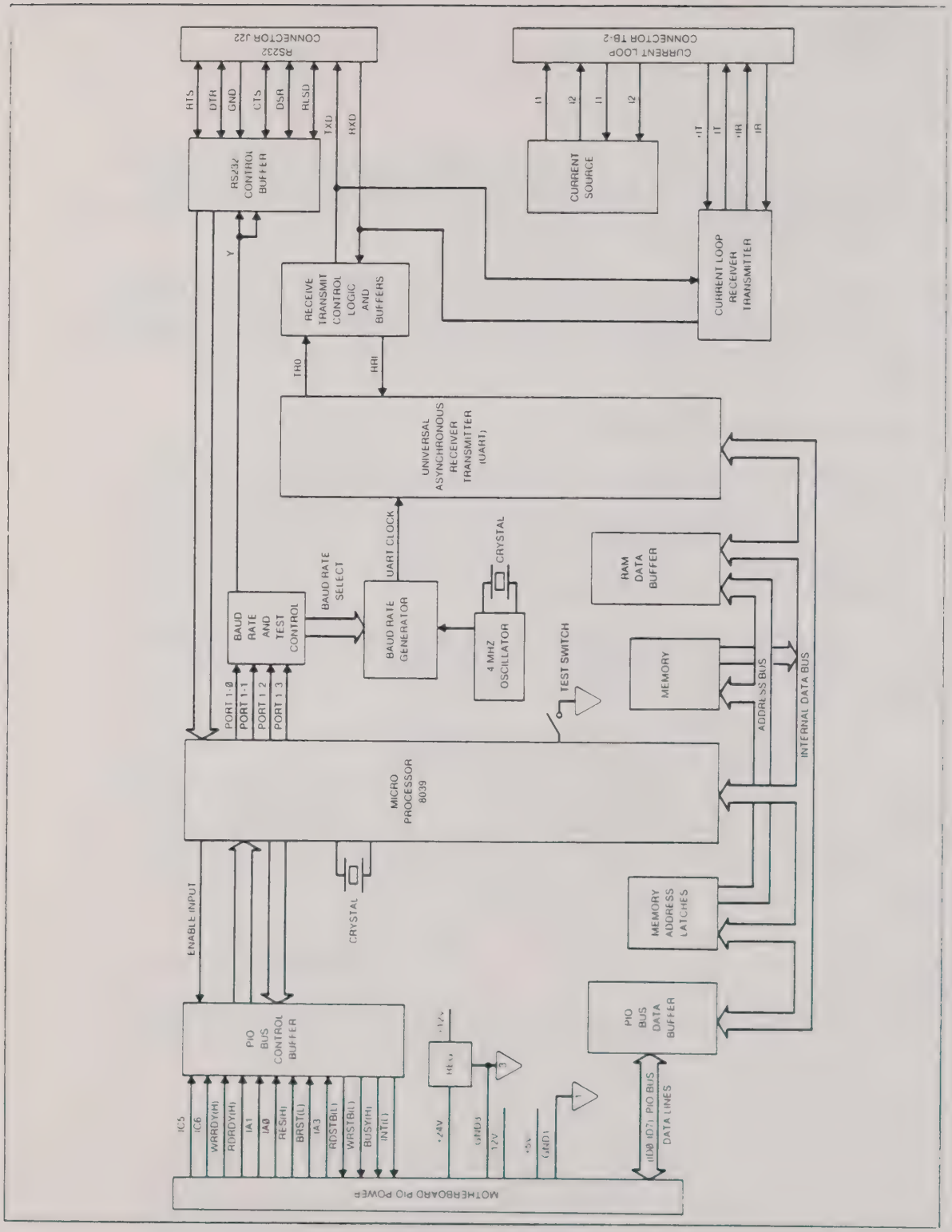


Figure 341-1. RS-232-C Interface

THEORY OF OPERATION

The following theory of operation discussion begins with a block diagram analysis that describes each major circuit block on the assembly. A detailed circuit analysis then describes how each major circuit block on the RS-232-C Interface assembly works. A schematic diagram for the RS-232-C Interface is located at the end of this option subsection.

Block Diagram Analysis

CONTROLLER

The controller portion of the circuitry performs the task of coordinating interactions between the 2280 controller assembly and the RS-232-C interface. It consists primarily of a microprocessor, ROM memory for storage of the microprocessor's program, RAM memory for buffering of transmit and receive characters, a crystal to derive the microprocessor's clock, and a latch to store part of the address for the ROM and RAM.

PIO BUS COMMUNICATION

The PIO Bus is a parallel interface though which all communication between the RS-232-C Interface assembly and the 2280 mainframe assembly takes place. In addition to the eight-bit bi-directional bus to transfer data, there are four signals that address the RS-232-C assembly, two that identify the type of PIO Bus transaction, an interrupt line, and a few handshake signals. The PIO Bus operation is completely described in section 3 of this manual.

BAUD RATE GENERATOR

The RS-232-C Interface communicates at one of eight front panel selectable baud rates from 110 through 19200 bits per second. This circuitry generates eight clocks at sixteen times the desired baud rate and selects one of them for use by the UART. The interface always transmits and receives at the same baud rate.

UART

The UART (Universal Asynchronous Receiver/Transmitter) provides the interface from the microprocessor to the serial RS-232-C or current loop drivers and receivers. The receiver portion of the UART converts serial start, data, parity, and stop bits to parallel data available for reading by the microprocessor. The transmitter portion converts parallel data from the microprocessor into a serial form and automatically adds start, parity, and stop bits.

RS-232-C CONTROL LINES

The RS-232-C Interface supports several interface control signals as described in the EIA RS-232-C Standard. All input signals to the assembly are biased to indicate a true status when they are left disconnected. This allows very easy connection between the 2280 and other RS-232-C devices.

CURRENT LOOP INTERFACE

The current loop interface circuitry provides an optically isolated current loop transmitter and receiver and two current sources that can be wired in series with the transmit or receive loop or both if the 2280 interface is required to provide the current for the loop.

Detailed Circuit Description

CONTROLLER

The microprocessor (U5) is driven by an internally generated clock derived from a 6MHz crystal (Y2). The processor executes a program stored in a ROM (U17) and can store data, primarily characters received or to be transmitted, in RAMs (U18 and U19). The lower bits of the address for the ROM and RAMs is latched in an eight bit latch (U28) that is gated by the address latch enable (ALE) signal from the microprocessor. The ROM is addressed using eight bits from the address latch and four bits provided by the microprocessor directly on port 2 bits 0 through 3. The lower seven bits of the RAMs address are from the address latch while the eight bit is provided by the bank select signal (BKS(H)). The microprocessor selects the state of BKS(H) by writing into the addressable latch U10. This allows the RAMs to be divided into two banks; one for input buffering and the other for output buffering. Gating provided by U23 and U24 is used to generate enabling signals and strobes for the PIO Bus and to communicate with the UART.

PIO BUS COMMUNICATION

The 2280 Series Data Logger contains a parallel bus called the PIO Bus that allows communication between the controller assembly and all logging and user interface devices. To the RS-232-C Interface Assembly, the PIO Bus is seen as address lines IA0, IA1 and IA3, (Interface Address) and RES (Remote Slot), control signals IC5 and IC6 (Interface Control), BUSY(H), RDRDY(H) (Read Ready), RDSTB(L) (Read Strobe), WRRDY(H) (Write Ready), and WRSTB(L) (Write Strobe), data lines ID0 through ID7 (Interface Data), and interrupt line RMINT(L) (Remote Interrupt).

The state of signal RES informs the RS-232-C interface assembly which position, port A or port B, it is installed. RES is connected to logic common (GND1) on the motherboard on the port A position connector and open, left floating, on the port B connector.

Signal RES along with the Interface Address signals IA0, IA1, and IA3 determine the PIO Bus Address for the assembly. Table 341-2 identifies the logic levels these signal must be in for the assembly to be addressed by the controller when installed in port A or B. The gating provided by U32 implements the necessary address decoding. When addressed, the assembly is allowed to drive the BUSY(H) signal back to the mainframe controller assembly.

Table 341-2. PIO Bus Address Decoding

Signal	Port A Logic State	Port B Logic State
RES	high	low
IA0	low	high
IA1	high	low
IA3	low	low

The microprocessor reads the PIO Bus control signals IC5, IC6, RDRDY(H), and WRRDY(H) buffered though U7 and U12 on port 1 bits 1 through 4. It drives the control signals back to the controller assembly through gating provided by U16 and buffers in U17. The PIO Bus data bits are buffered by U6, U7, U11 and U12.

BAUD RATE GENERATOR

The baud rate at which the interface receives and transmits data is selected from a set of eight available clocks through data selector U4. The clock at the output of the data selector is supplied to the UART at sixteen times the desired baud rate. The control signals supplied to the data selector are stored in addressable latch U10 which is written to by the microprocessor using port 1 bits 0 through 3.

The eight clock inputs to the data selector are derived from a 4 MHz crystal oscillator (Y1 and U9), dividers (U15 and U3), and a special divider for the 110 baud rate clock (U1 and U2)

UART

The UART (U22) provides parallel to serial and serial to parallel conversions of data between the microprocessor and the RS-232-C and current loop drivers and receivers. It is clocked at a frequency sixteen times the desired data rate. This clock is used for both transmitting and receiving.

The UART communicates with the microprocessor using a data bus, several handshake signals and two signals that generate interrupts.

Before characters can be transmitted or received the UART must be configured for proper parity, number of stop bits, and character length. This configuration information is presented to the UART using the microprocessor data bus on signal lines parity inhibit (PI), stop bit select (SBS), character length select (CSL1, CLS2), and even parity enable (EPE) and gated by the control register load (CRL) signal. The CRL signal can be monitored on test point TP87.

The character receiving process involves several operations between the microprocessor and the UART. First of all, serial data coming into the RS-232-C assembly is level shifted from a RS-232-C level to a TTL level in U8 and presented to the receive register input (RRI) of the UART. When a complete character is received, the UART generates a data received signal (DR), which in turn interrupts the microprocessor by setting the interrupt signal (INT) on U5 low. The microprocessor reads the received character by allowing the UART to place its receive buffer register contents (RBR1 through RBR8) onto the data bus. The enabling signal to accomplish this can be monitored on test point TP86. The microprocessor also checks to see if the UART detected any errors in receiving the character by gating the UART signals parity error (PE), framing error (FE), and overrun error (OE) onto the data bus through buffers in U6 and U11. This enabling signal is available on test point TP88.

The character transmitting process is less involved than the receive process. It begins with the microprocessor reading the transmitter buffer register empty (TBRE) signal from the UART to determine if the UART can accept a character to transmit. When the UART is ready to accept a character to transmit, the microprocessor presents a character to the UART transmit buffer register (TBR1 through TBR8) using the data bus and gates it into the UART by strobing the transmit buffer register load (TBRL) signal. This strobe can be monitored on test point TP85. Then the UART shifts the character out serially on the transmit register out (TRO) signal. This signal is then level shifted and buffered to provide either a EIA voltage-level signal and a 20-milliampere current loop signal. When the complete character has been transmitted, the UART generates the transmitter register empty (TRE) signal which in turn interrupts the microprocessor to indicate that the next character to be transmitted can be loaded into the UART.

RS-232-C CONTROL LINES

This section briefly describes the function of each signal implemented by the RS-232-C Interface Assembly. The output signals are buffered through EIA RS-232-C drivers in U14 and the input signals are received through U8.

- Protective Ground
  Direction: Not Applicable
  Pin Number: 1

- Transmit Data
  Direction: Output
  Pin Number: 2

  Serial data output from the RS-232-C Interface Assembly. Held in marking state (-3 to -12V) during intervals between characters. No data is transmitted unless the Request to Send, Clear to Send, Data Set Ready, and Received Line Signal Detect are true (+3 to +12V).

- Receive Data
  Direction: Input
  Pin Number: 3

  Serial data input to the RS-232-C Interface Assembly.

- Request to Send
  Direction: Output
  Pin Number: 4

- Clear to Send
  Direction: Input
  Pin Number: 5

  Must be in logic true state (+3 to +12V) for the RS-232-C Interface to transmit characters. This input is biased such it will be in the true state if left disconnected.

- Data Set Ready
  Direction: Input
  Pin Number: 6

  Must be in logic true state (+3 to +12V) for the RS-232-C Interface to transmit characters. This input is biased such it will be in the true state if left disconnected.

- Signal Ground
  Direction: Not Applicable
  Pin Number: 7

  Voltage reference level for all other input and output signals.

- Received Line Signal Detect
  Direction: Input
  Pin Number: 8

  Must be in logic true state (+3 to +12V) for the RS-232-C Interface to transmit characters. This input is biased such it will be in the true state if left disconnected.

- Data Terminal Ready
  Direction: Output
  Pin Number: 20

CURRENT LOOP INTERFACE

The 20 milli-ampere current loop circuit operates as either an active or passive current loop interface. The 20 milliampere current sources (Q1 with R5 and Q2 with R6) can optionally be connected in series with the passive current receive and current transmit circuitry if the 2280 interface is required to provide the current source for a loop.

The receive loop has reverse bias protection (CR2) and optical isolation from logic common (U21). The transmit loop has reverse bias protection (CR1) and isolation (U26). Q3 provides the 20mA drive requirement of the transmit loop.

GENERAL MAINTENANCE

The RS-232-C Interface PCA normally does not require cleaning, but if dirt, dust, or other contamination is visible on the surface, the PCA should be cleaned. Follow PCA cleaning instructions in Section 4 of this manual.

PERFORMANCE TEST

The following performance test may be used to verify that the RS-232-C Interface is functional. The performance test may also be used as an initial acceptance test.

WARNING

THE DATA LOGGER CONTAINS HIGH VOLTAGES WHICH CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE EQUIPMENT. TURN OFF THE DATA LOGGER AND REMOVE ALL POWER SOURCES BEFORE PERFORMING ANY OF THE PROCEDURES IN THIS SECTION.

1. Set the keyswitch to OFF, and disconnect the Data Logger power input.

2. If a Digital PCA Extender Fixture is available, install it in either the Port A or Port B position, then install the RS-232-C Interface on the extender. If a Digital PCA Extender Fixture is not available, install the RS-232-C Interface in either the Port A or Port B position (refer to the 2280B System Guide for installation instructions).

3. Connect the Data Logger power input, and turn the keyswitch to PROGRAM.

4. Remove any cables connected to the RS-232-C connector (J22) on the RS-232-C interface.

5. Execute the system system self test that verifies the ability of the mainframe controller to communicate with the RS-232-C interface assembly using the steps given in Table 341-3.

Table 341-3. Device/Controller Interface Test Programming Steps

KEYSTROKE (S)	DATA LOGGER PROMPT
S	<S> SYSTEM DIAGNOSTICS
ENTER	S: DEVICE TO TEST <1-7>? 1
*3 (or 4)	S<3or4> PORT A (PORT B)
ENTER	S3(or4): TEST <1-4>? 1
ENTER	

*Enter 3 if RS-232-C Interface is installed in Port A.
Enter 4 if RS-232-C Interface is installed in Port B.

6. The Data Logger should display either TEST PASSED or TEST FAILED. If the display indicates TEST FAILED, the interface is defective. If the display indicates TEST PASSED, execute the self test that verifies the RAM on the RS-232-C interface using the steps in Table 341-4.

Table 341-4. RAM Test Programming Steps

KEYSTROKE (S)	DATA LOGGER PROMPT
EXIT	S3(or 4): TEST <1-4>? 2
ENTER	

7. When the test is completed, the Data Logger will display either TEST PASSED or TEST FAILED. If the display indicates TEST FAILED, the interface is defective. If the display indicates TEST PASSED, execute the self test that verifies proper operation of the UART on the RS-232-C interface using the steps in Table 341-5.

Table 341-5. UART Test Programming Steps

KEYSTROKE (S)	DATA LOGGER PROMPT
EXIT	S3(or 4): TEST <1-4>? 3
ENTER	

8. When the test is completed, the Data Logger will display either TEST PASSED or TEST FAILED. If the display indicates TEST FAILED, the interface is defective. If the display indicates TEST PASSED, execute the self test that verifies proper operation of the RS-232-C control signals on the RS-232-C interface using the steps in Table 341-6.

Note

Performance of test number 4, the RS-232-C Control Line Test, requires the control lines on J22, the RS-232-C connector, be connected as shown in Table 341-7

Table 341-7. Control Line Test Connector Wiring

FROM		TO	
Pin	Signal Name	Pin	Signal Name
5	Clear to Send	4	Request to Send
6	Data Set Ready	20	Data Terminal Ready
8	Rec. Line Signal Detect	20	Data Terminal Ready

Table 341-6. RS-232-C Control Line Test Programming Steps

KEYSTROKE (S)	DATA LOGGER PROMPT
EXIT ENTER	S3(or 4): TEST <1-4>? 4

9. Remove the control line test connector from the rear panel of the RS-232-C assembly.

10. If the RS-232-C Interface is mounted on a Digital PCA Extender Fixture switch S1 is accessible. Set switch S1 to ON. If the RS-232-C Interface is not on an extender, turn the keyswitch to OFF, pull the RS-232-C Interface out to gain access to switch S1, set the switch to ON, then reinstall the RS-232-C Interface. Turn the keyswitch to PROGRAM.

11. If the LED on the RS-232-C Interface board remains off, continue this procedure. If it lights continuously, or flashes, the interface is defective.

12. Set switch S1 to OFF. (If a Digital PCA Extender Fixture is not in use, turn the keyswitch to OFF, pull the RS-232-C Interface out to gain access to the switch, set S1 to OFF, then reinstall the interface and turn the keyswitch to PROGRAM.

13. Connect an RS-232-C terminal to the RS-232-C Interface, switch on power to the terminal, and set the terminal for full duplex mode.

14. From the Data Logger front panel, program the RS-232-C Interface characteristics to be compatible with the terminal in use.

15. Set switch S1 to ON. (If a Digital PCA Extender Fixture is not in use, turn the keyswitch to OFF, pull the RS-232-C Interface out to gain access to the switch, set S1 to ON, then reinstall the interface and turn the keyswitch to PROGRAM.) Type random characters on the terminal. Verify that the characters typed are echoed back and displayed on the terminal CRT.

17. The RS-232-C Interface performance test is complete. Return the unit to normal service configuration. Make sure that switch S1 on the interface card is in the OFF position.

CALIBRATION

The RS-232-C Interface requires no calibration.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the RS-232-C Interface is given in Table 341-8. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the RS-232-C Interface is given in Figure 341-2.

TABLE 341-8. 2280A-341 RS-232-C INTERFACE PCA
(SEE FIGURE 341-2.)

REFERENCE DESIGNATOR A->NUMERICS--->	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	N O T -E
C 1, 11- 25		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	16		
C 2		CAP,CER,0.01UF,+80-20%,100V,Z5V	149153	56289	C0238101F103M	1		
C 3		CAP,CER,10PF,+-10%,3000V,Z5U	105536	56289	40C362A1	1		
C 4		CAP,CER,4.7PF,+-0.25PF,100V,COH	362772	89536	362772	1		
C 5		CAP,CER,0.05UF,+80-20%,25V,Y5U	148924	72982	5855-000-Y5U0-503Z	1		
C 6- 9		CAP,CER,1000PF,+-10%,500V,X5S	357806	56289	C016B102G102K	4		
C 10		CAP,CER,18PF,+-2%,100V,COG	512335	51406	RD870-100V	1		
C 27		CAP,AL,47UF,+-20%,16V	643304	89536	643304	1		
CR 1	*	DIODE,SI,BV= 75.0V,IO=150MA,500 MW	203323	07910	1N4448	1		
CR 2	*	LED,RED,POINT SOURCE,PCB MOUNT	385898	28480	5082-4487	1	1	
CR 3	*	LED,RED,90 LEAD PREP,LUM INT=2MCD	604884	89536	604884	1	1	
H 1		WASHER,LOCK,INTRNL,STEEL,#4	110403	89536	110403	2		
H 2		SCREW,MACH,FHUP,STL,6-32X3/8	271917	89536	271817	2		
H 3		WASHER,FLAT,BRASS,#4,0.025	110775	89536	110775	2		
H 4		NUT,PRESS,BROACH,STL,6-32	393785	89536	393785	2		
H 5		BROACHING TYPE, .375,4-40THRD,3/16HD	603894	89536	603894	2		
H 6		WASHER,LOCK,SPLIT,STEEL,#4	110395	89536	110395	2		
H 7		NUT,MACH,HEX,STL,4-40	184044	73734	8002A-NP	2		
J 22		CONN,D-SUB,PWB,R/A MOUNT,25 PIN	706218	89536	706218	1		
MP 1		COVER,RS232-C I/F	579169	89536	579169	1		
MP 2		CABLE TIE,4"L,0.100"W,0.75 DIA	172080	89536	172080	2		
MP 3		GROMMET, RUBBER	100073	83330	2149	1		
MP 4		BAG,SHIELDING,TRANSPARENT,12"X16"	680983	89536	680983	1		
Q 1, 2	*	TRANSISTOR,SI,PNP,SMALL SIGNAL	195974	64713	2N3906	2	1	
Q 3	*	TRANSISTOR,SI,NPN,SMALL SIGNAL	218396	04713	2N3904	1	1	
R 1, 2		RES,CF,1K,+-5%,0.25W	343426	80031	CR251-4-5P1K	2		
R 3		RES,CF,560,+-5%,0.25W	385948	80031	CR251-4-5P560E	1		
R 4		RES,CF,390,+-5%,0.25W	441543	80031	CR251-4-5P390E	1		
R 5, 6		RES,CF,270,+-5%,0.25W	348789	80031	CR251-4-5P270E	2		
R 7- 9, 18-		RES,CF,5.1K,+-5%,0.25W	368712	80031	CR251-4-5P5K1	6		
R 20			368712					
R 10		RES,CF,24,+-5%,0.25W	442210	80031	CR251-4-5P24E	1		
R 11		RES,CF,330,+-5%,0.25W	368720	80031	CR251-4-5P330E	1		
R 12- 14, 16		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	4		
R 15		RES,CF,1,+-5%,0.25W	357665	80031	CR251-4-5P1E	1		
R 17		RES,CF,47K,+-5%,0.25W	348896	80031	CR251-4-5P47K	1		
S 1		SWITCH,SLIDE,SPDT	429332	89536	429332	1	1	
TB 2		TERMINAL STRIP, 10 CIRCUITS	530089	89020	SS B 410	1		
TP 1, 3, 10,		CONN,TAB,FASTON,PRESS-IN,0.110 WIDE	512889	02660	62395	20		
TP 12, 13, 73-			512889					
TP 80, 84- 90			512889					
U 1, 2	*	IC,CMOS,DUAL JK F/F,+EDG TRIG	355230	02735	CD4027AE	2	1	
U 3	*	IC,CMOS,12STAGE RIPPLE CARRY BIN CNTR	429605	02735	CD4040AE	1	1	
U 4	*	IC,CMOS,8-INPUT MUX W/3-STATE OUTPUT	504647	04713	MC4512BCP	1		
U 5	*	IC,NMOS,8 BIT MICROCOMPUTER	504563	89536	504563	1		
U 6, 7, 11,	*	IC,CMOS,HEX BUFFER W/3-STATE OUTPUT	407759	12040	MM80C97N	4	1	
U 12	*		407759					
U 8, 27	*	IC,TTL,QUAD RS232C LINE RECEIVER	524850	04713	MS1489AP	2	1	
U 9	*	IC,LSTTL,QUAD 2 INPUT NAND GATE	393033	01295	SN74LS00N	1	1	
U 10	*	IC,LSTTL,8BIT ADDRSABLE LATCH,W/CLR	419242	01295	SN74LS259N	1	1	
U 13, 20	*	IC,TTL,QUAD BUFFER W/3-STATE OUTPUT	473728	12040	DM74125N	2	1	
U 14	*	IC,TTL,QUAD RS232C LINE DRIVER	414052	12040	LM1488	1	1	
U 15	*	IC,LSTTL,SYNC DIV BY 16 BINARY COUNTR	495598	01295	SN74LS163N	1	1	
U 16, 32	*	IC,CMOS,QUAD 2 INPUT NOR GATE	355172	02735	CD4001AE	2	1	
U 17	*	IC, 2K X 8 EPROM (PROGRAMMED)	655597	89536	655597	1		
U 18, 19	*	IC 256 X 4 STAT RAM	404558	89536	404558	2		
U 21, 26	*	ISOLATOR,OPTO,HI-SPEED,LED TO XSISTOR	407742	28480	HP5082-4351	2	1	
U 22	*	IC,CMOS,UNIV ASYNC RECEIVR/TRANSMITER	453464	32293	1M6402CPL	1	1	
U 23	*	IC,LSTTL,TRIPLE 3 INPUT NOR GATE	393090	01295	SN74LS27N	1	1	
U 24, 25	*	IC,LSTTL,QUAD 2 INPUT OR GATE	393108	01295	SN74LS32N	2	1	
U 28	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,W/CLEAR	454892	01295	SN74LS273N	1	1	
U 29	*	IC,LSTTL,HEX INVERTER	393058	01295	SN74LS04N	1	1	
U 30	*	IC,CMOS,HEX INVERTER	404681	02735	CD4069BE	1	1	
U 31	*	IC,VOLT REG,FIXED,+12 VOLTS,0.1 AMPS	408138	07263	A78L12WC	1	1	
XU 5, 22		SOCKET,DIP,0.100 CTR,40 PIN	429282	09922	DILB40P-108	2	1	
XU 17		SOCKET,DIP,0.100 CTR,24 PIN	376236	91506	324-AG39D	1		
XU 18, 19		SOCKET,DIP,0.100 CTR,18 PIN	418228	91506	318-AG39D	2		
Y 1	*	CRYSTAL,4MHZ,+-0.02%,HC-18/U	474072	89536	474072	1	1	
Y 2	*	CRYSTAL,6MHZ,+-0.01%,HC-18/U	461665	89536	461665	1	1	
Z 1- 4		RES,NET,SIP,8 PIN,7 RES,22K,+-2%	500041	89536	500041	4		
Z 5, 6		RES,NET,DIP,14 PIN,7 RES,10K,+-5%	364000	01121	314	2		

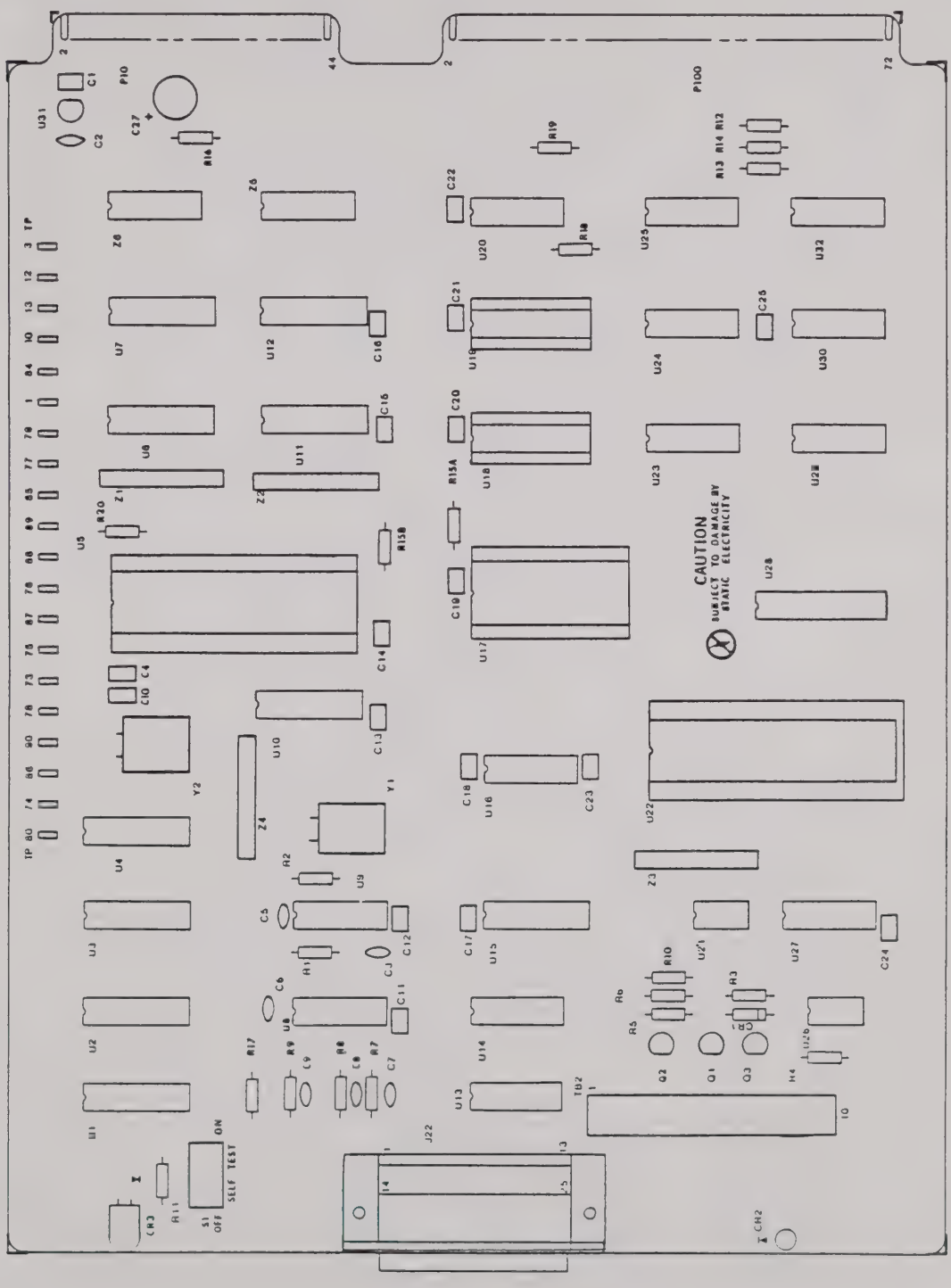
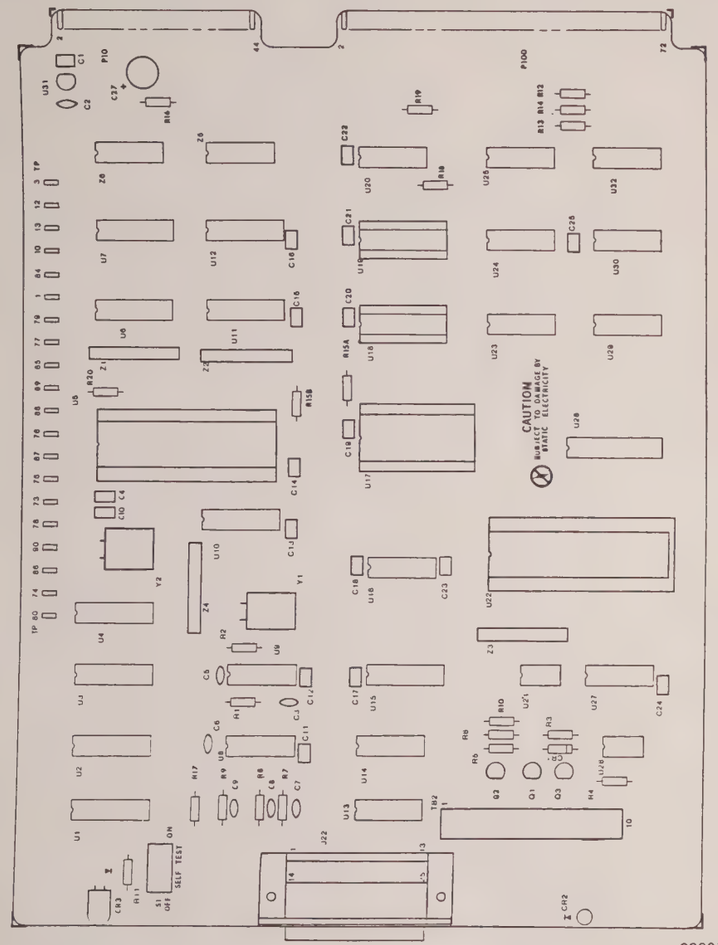
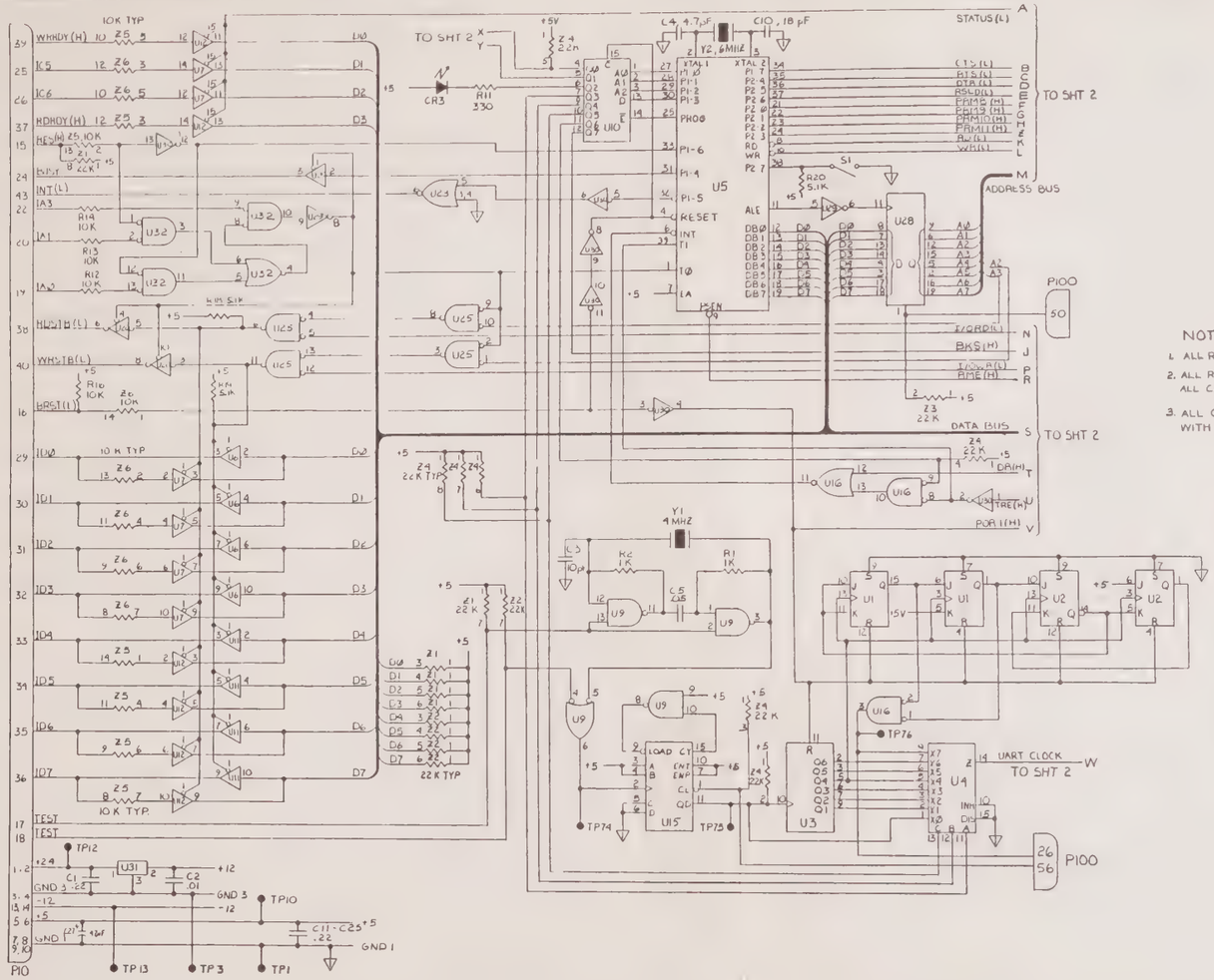


Figure 341-2. 2280A-341 RS-232-C Interface PCA



2280A-1641



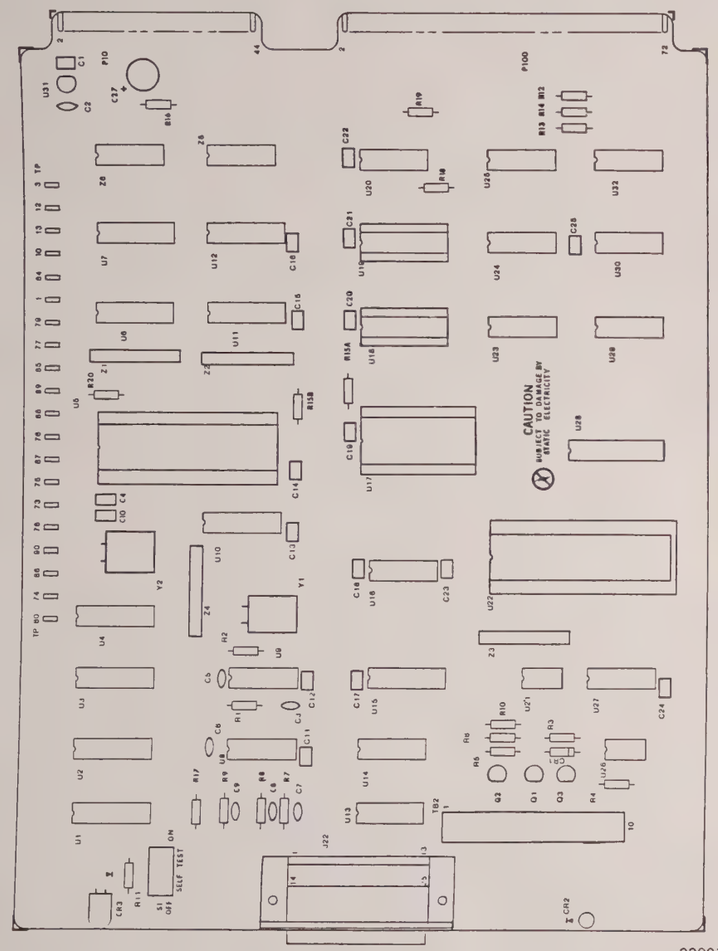
NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE ¼ W 5 %.
2. ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCE IS IN MICROFARADS.
3. ALL GRAPHIC SYMBOLS ARE IN ACCORDANCE WITH ANSI Y32.2 AND 32.14

REF DES	+5V	+12V	-12V	GND 1	GND 3
U1	5,16			7,8,9	
U2	8,16			7,8,9	
U3	16			8	
U4	16			8,10,12	
U5	7,26,40			20	
U6	16			8	
U7	16			8	
U8	13			7	
U9	9,14			7	
U10	16			8	
U11	16			8	
U12	16			8	
U13	14			7	
U14	10,12	14	1	7,8,9,12	7
U15	3,4,7,10,16			5,6,8	
U16	4			6,7	
U17	4			6,7	
U18	2,4			6,7	
U19	18			8,10	
U20	4			6,10	
U21		8		5	
U22	14			7	
U23	14			3,4,7	
U24	14			7	
U25	14			7	
U26	14			7	
U27	14			7	
U28	14			1,4,7,13	
U29	14			10	
U30	14			7	
U31	14			7	
U32	14			7	

2280A-1041

Figure 341-2. RS-232-C Interface Schematic Diagram



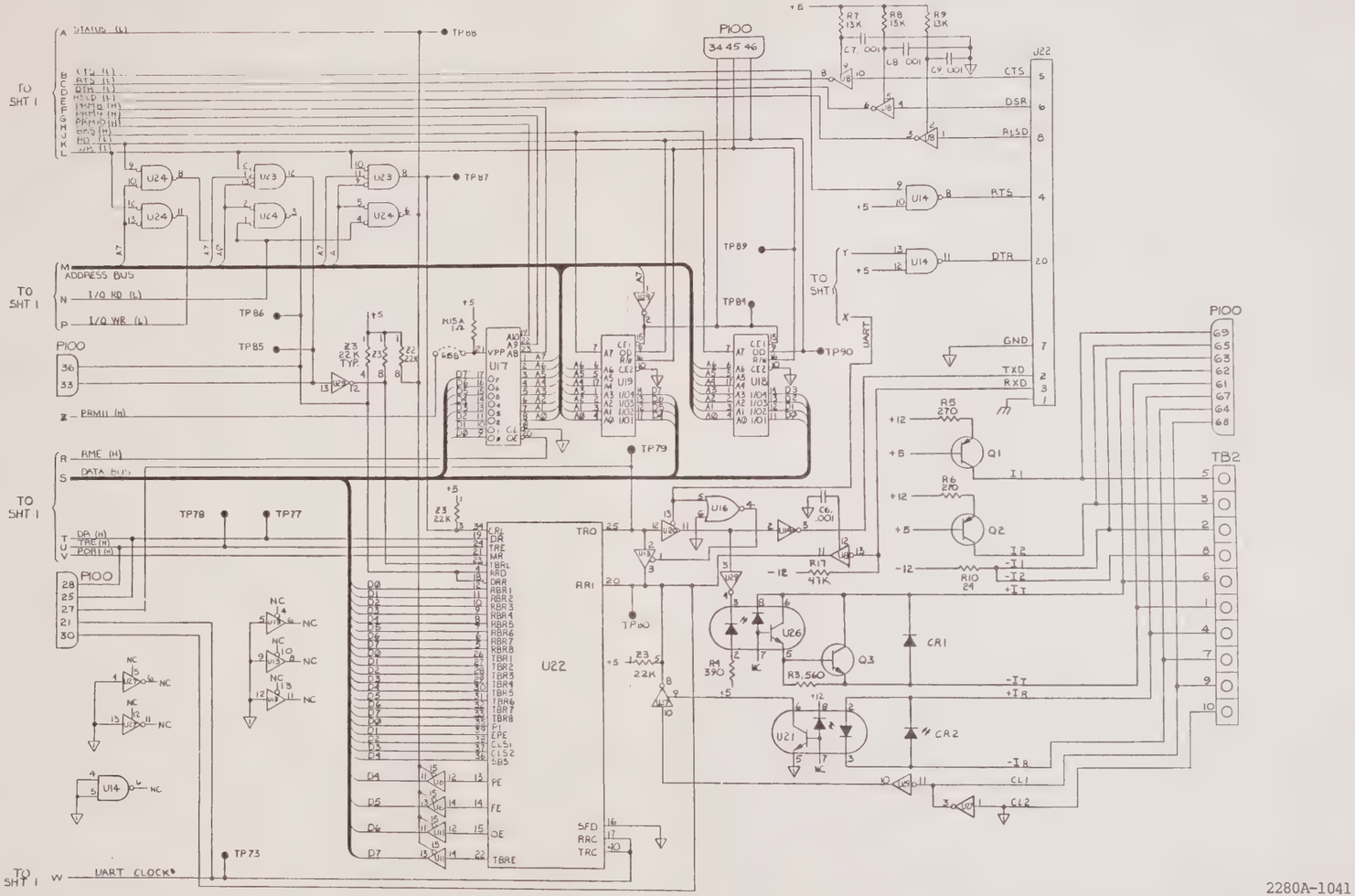


Figure 341-2. RS-232-C Interface Schematic Diagram (cont.)

Option 2280A-342
IEEE-488 Interface

DESCRIPTION

The IEEE-488 Interface provides the communication link between the Data Logger and an IEEE-488-compatible device. The IEEE-488 Interface is illustrated in Figure 342-1. The interface installs in either Port A or Port B of the Data Logger.

When the IEEE-488 Interface is installed in Port A, the Data Logger can be programmed and operated from an IEEE-488 bus controller. When the interface is installed in Port B, it provides output capability only.

The IEEE-488 Interface consists primarily of LSI chips, a microprocessor, read only memory, an IEEE-488 talker/listener chip, and some random logic chips to connect them together. The microprocessor executes firmware stored in the ROM that coordinates communication between the 2280 controller assembly and the IEEE-488 bus. The talker/listener takes care of the details of IEEE-488 protocol.

WHERE TO FIND ADDITIONAL INFORMATION

In this subsection are IEEE-488 Interface theory of operation, general maintenance, performance tests, calibration procedure, a parts list, and a schematic diagram. Installation and system configuration instructions are in the 2280 Series System Guide, and operation and programming instructions are in the 2280 Series User Guide. Option specifications are in the appendices in this manual and the System Guide.

Test equipment required to perform the procedures in this subsection is listed in Table 342-1. A summary of test equipment required for all procedures in this manual is given in Table 1-1 in Section 1 of this manual.

Table 342-1. Required Test Equipment

INSTRUMENT	REQUIRED SPECIFICATIONS	RECOMMENDED MODEL
IEEE-488 Bus Controller	.....	Fluke 1722A

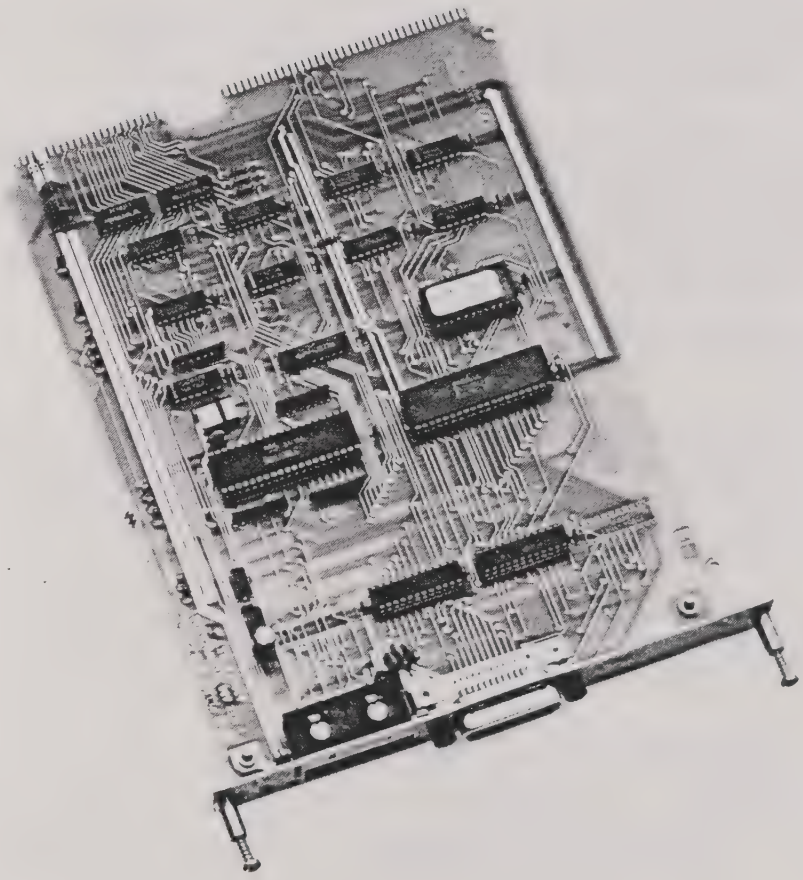


Figure 342-1. The IEEE-488 Interface

THEORY OF OPERATION

The following theory of operation discussion begins with a block diagram analysis that describes each major circuit block on the assembly. A detailed circuit analysis then describes how each major circuit block on the IEEE-488 Interface assembly works. Refer to Figure 342-2, the IEEE-488 Interface Block Diagram. Schematic diagrams for the IEEE-488 Interface are at the end of this option subsection.

Block Diagram Analysis

CONTROLLER

The controller portion of the circuitry performs the task of coordinating interactions between the 2280 controller assembly and the IEEE-488 bus interface. It consists primarily of a microprocessor, ROM memory for the microprocessor's program, a crystal to derive the microprocessor's clock, and a latch to store a portion of the address to the ROM.

PIO BUS

The PIO Bus is a parallel interface though which all communication between the IEEE-488 Interface assembly and the 2280 mainframe controller assembly takes place. In addition to the eight-bit bi-directional bus to transfer data, there are two signals that address the IEEE-488 assembly, two that identify the type of PIO Bus transaction, an interrupt line, and a few handshake signals. The PIO Bus operation is completely described in section 3 of this manual.

IEEE-488 ADDRESS SWITCH

Two thumbwheel switches are accessable through the rear panel of the assembly. These switches allow the IEEE-488 Bus address to be selected. Addresses of 00 through 30 are valid IEEE-488 Bus addresses; an address of 31 puts the interface in talk only mode.

IEEE-488 INTERFACE

The IEEE-488 interface portion of the circuit consists of a single chip that performs the detail aspects of IEEE-488 communication and two chips that drive the control and data signals that are available on the rear panel connector.

Detailed Circuit Description

CONTROLLER

The microprocessor (U2) is driven by an internally generated clock derived from a 6 MHz crystal (Y1). The processor executes a program stored in a ROM (U15). The lower eight bits of the address for the ROM are latched in an eight bit latch (U7) that is gated by the address latch enable (ALE) signal from the microprocessor. The upper 4 bits of the ROM address is provided by P2-0 through P2-3 which is part of one of the two 8-bit processor input/output ports.

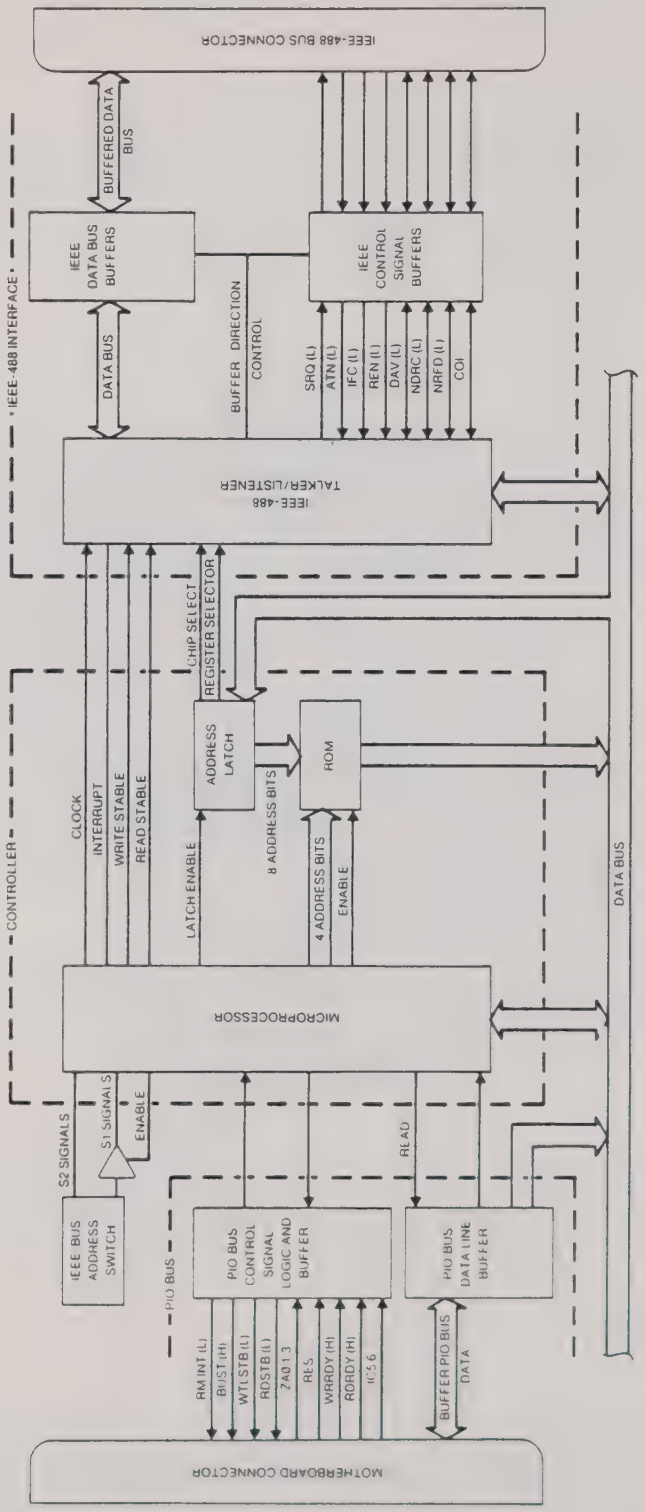


Figure 342-2. IEEE-488 Interface Block Diagram

The two 8-bit processor ports and the processor data bus provide the data paths and control signals necessary to interface to the PIO Bus Communication, IEEE-488 Bus Address Switch, and IEEE-488 Interface circuitry.

PIO BUS COMMUNICATION

The 2280 Series Data Logger contains a parallel bus called the PIO Bus that allows communication between the controller assembly and all logging and user interface devices. To the IEEE-488 Interface Assembly, the PIO Bus is seen as address lines IA0, IA1 and IA3 (Interface Address), and RES (Remote Slot), control signals IC5 and IC6 (Interface Control), BUSY(H), RDRDY(H) (Read Ready), RDSTB(L) (Read Strobe), WRRDY(H) (Write Ready), and WRSTB(L) (Write Strobe), data lines ID0 through ID7 (Interface Data), and interrupt line RMINT(L) (Remote Interrupt).

The state of signal RES informs the IEEE-488 interface assembly in which position, port A or port B, it is installed. RES is connected to logic common (GND1) on the motherboard on the port B position connector and open, left floating, on the port A connector.

Signal RES along with the Interface Address signals IA0, IA1, and IA3 determine the PIO Bus Address for the assembly. Table 342-2 identifies the logic levels necessary for each signal if the assembly is to be addressed by the controller when installed in port A or B. The gating provided by U8 implements the necessary address decoding. Test point TP57 will be at a logic low when the card is addressed. When addressed, the assembly is allowed to drive the BUSY(H) signal back to the mainframe controller assembly.

Table 342-2. Port A and Port B Logic Levels

Signal	Port A Logic State	Port B Logic State
RES	high	low
IA0	low	high
IA1	high	low
IA3	low	low

The microprocessor reads the PIO Bus control signals IC5, IC6, RDRDY(H), and WRRDY(H) buffered though U4 and U13 on port 1 bits 1 through 4. It drives the control signals back to the controller assembly through gating provided by U16 and buffers in U17. The PIO Bus data bits are buffered by U5, U9, and U13.

IEEE-488 ADDRESS SWITCH

Two thumbwheel rotary switches with decimal readout determine the IEEE-488 Bus address for the assembly. Switch S1 represents the most significant digit, and S2 represents the least significant digit of the address. S2 is read directly by the microprocessor on port 2 bits 4 and 5 while S1 is buffered by U4.

IEEE-488 INTERFACE

The IEEE-488 talker/listener chip (U11) is connected to the IEEE-488 connector on the rear panel of the assembly through buffers U1 and U10.

The line T/R1 from the talker/listener chip determines wnether the chip is driving or receiving the signals.

GENERAL MAINTENANCE

The IEEE-488 Interface PCA normally does not require cleaning, but if dirt, dust, or other contamination is visible on the surface, the PCA should be cleaned. Follow PCA cleaning instructions in Section 4 of this manual.

PERFORMANCE TESTS

The following performance test may be used to verify that the IEEE-488 Interface is functional. The performance test may also be used as an initial acceptance test.

WARNING

THE DATA LOGGER CONTAINS HIGH VOLTAGES WHICH CAN BE DANGEROUS OR FATAL. ONLY QUALIFIED PERSONNEL SHOULD ATTEMPT TO SERVICE THE EQUIPMENT. TURN OFF THE DATA LOGGER AND REMOVE ALL POWER SOURCES BEFORE PERFORMING ANY OF THE PROCEDURES IN THIS SECTION.

1. Turn the 2280 front panel keyswitch to the POWER OFF position and disconnect the line and/or battery input power.

2. Install the IEEE-488 Interface in the Port A position. Port A is the vertical slot nearest the center of the instrument as viewed from the rear.

3. Select the IEEE-488 bus address for the 2280 by setting the rear panel switches above the connector to the appropriate positions.

4. Connect a shielded IEEE-488 cable between the IEEE-488 connector on the instrument and your computer.

5. Connect the Data Logger power input and turn the keyswitch to the PROGRAM position.

6. Execute the system diagnostic for port A using the steps given in table 342-2. This verifies that the 2280 controller can communicate with the IEEE-488 interface assembly.

Table 342-3. Device/Controller Interface Test Programming

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1	S	<S> SYSTEM DIAGNOSTICS
2	ENTER	S: DEVICE TO TEST <1-7>? 1
3	3	S3 PORT A
4	ENTER	S3 TEST <1-2>? 1
5	ENTER	

7. The Data Logger should display either TEST PASSED or TEST FAILED. If the display is TEST FAILED, the interface is not working, that is, the 2280 mainframe controller cannot communicate with the IEEE-488 option. If the display is TEST PASSED, execute the second diagnostic test using the steps given in Table 342-4. This tests the internal bus on the interface assembly.

Table 342-4. Internal Bus Test Programming

STEP	KEYSTROKE (S)	DATA LOGGER PROMPT
1	EXIT	S3(or4): TEST <1-2>? 2
2	ENTER	

8. When the test is completed, the Data Logger will display either TEST PASSED or TEST FAILED. (Refer to Section 2 for the system test descriptions).

9. Write a short program on your computer that will put the 2280 into remote. The program required to do this is dependent on the computer you're using. On the Fluke 1720A or 1722A executing the BASIC statement

```
10 REMOTE @2%
```

would put the IEEE-488 instrument with bus address 2 into remote.

10. After executing the program, verify that the 2280 has the message

```
IN REMOTE
```

displayed on the front panel.

13. The performance test is complete.

CALIBRATION

The IEEE-488 Interface Option requires no calibration.

LIST OF REPLACEABLE PARTS AND SCHEMATIC DIAGRAM

An illustrated list of replaceable parts for the IEEE-488 Interface is given in Table 342-5. For parts ordering information, see Section 6 of the 2280 Series Service Manual. A schematic diagram for the IEEE-488 Interface is given in Figure 342-3.

TABLE 342-5. 2280A-342 IEEE-488 INTERFACE PCA
(SEE FIGURE 342-2.)

REFERENCE DESIGNATOR A->NUMERICS---)	S	----------DESCRIPTION----------	FLUKE STOCK --NO--	MFRS SPLY CODE-	MANUFACTURERS PART NUMBER --OR GENERIC TYPE--	TOT QTY	R S -Q	NOT -E
C 1, 2, 5-		CAP,CER,0.22UF,+-20%,50V,Z5U	519157	51406	RPE111Z5U224M50V	17		
C 7, 11- 18,			519157					
C 20- 23			519157					
C 3		CAP,CER,20PF,+-10%,500V,T2H	106369	56289	561CT2HBA102AE200K	1		
C 4		CAP,CER,5.0PF,+-10%,1000V,S2L	368654	89536	368654	1		
C 8		CAP,POLYES,0.1UF,+-10%,50V	696484	89536	696484	1		
C 9		CAP,CER,0.01UF,+80-20%,100V,Z5V	149153	56289	C0238101F103M	1	1	
C 10		CAP,CER,1000PF,+-10%,500V,X5S	357806	56289	C016B102G102K	1		
C 19, 24		CAP,AL,47UF,+-20%,16V	643304	89536	643304	2		
C 25		CAP,CER,100PF,+-10%,1000V,S3N	105593	71590	DD-101	1	1	
DS 1	*	LED,RED,90 LEAD PREP,LUM INT=2MCD	604884	89536	604884	1		
H 1		5/16" ALUM TUBULAR RIVET	245290	89536	245290	2		
H 2		WASHER,LOCK,INTRNL,STEEL,#4	110403	89536	110403	2		
H 3		SCREW,MACH,FHUP,STL,6-32X3/8	271817	89536	271817	2		
H 4		NUT,PRESS,BROACH,STL,6-32	393785	89536	393785	2		
H 5		WASHER,FLAT,BRASS,#4,0.025	110775	89536	110775	2		
J 45		CONN,PWB,RIBBON,90,24 POS,STD ORIENT	658039	89536	658039	1		
L 1, 2		CHOKE,6TURN	320911	89536	320911	2		
MP 1		COVER, IEEE-488-I/F	718395	89536	718395	1		
MP 2		CABLE TIE,4"L,0.100"W,0.75 DIA	172080	89536	172080	1		
MP 3		BAG,SHIELDING,TRANSPARENT,12"X16"	680983	89536	680983	1		
R 1- 3, 5		RES,CF,10K,+-5%,0.25W	348839	80031	CR251-4-5P10K	4		
R 4		RES,CF,330,+-5%,0.25W	368720	80031	CR251-4-5P330E	1		
S 1, 2		SWITCH,ROTARY,1POLE,MULTI POS,SPECIAL	603191	89536	603191	1	1	
TP 1, 10, 55-		CONN,TAB,FASTON,PRESS-IN,0.110 WIDE	512889	02660	62395	10		
TP 60			512889					
TP 70, 74			512889					
U 1, 10	*	IC,LSTTL,OCTL IEEE-488 BUS TRANSCVR	524835	04713	MC3447P	2		
U 2	*	IC, NMOS 8 BIT MICROCOMPUTER	504563	89536	504563	1		
U 3	*	IC,CMOS,HEX INVERTER	404681	02735	CD4069BE	1	1	
U 4, 5, 9,	*	IC,CMOS,HEX BUFFER W/3-STATE OUTPUT	407759	12040	MM80C97N	4	1	
U 13	*		407759					
U 7	*	IC,LSTTL,OCTAL D F/F,+EDG TRG,W/CLEAR	454892	01295	SN74LS273N	1		
U 8	*	IC,CMOS,QUAD 2 INPUT NOR GATE	355172	02735	CD4001AE	1	1	
U 11	*	IC,NMOS,GPIB TALKER/LISTENER	586909	89536	586909	1		
U 12	*	IC,LSTTL,HEX INVERTER	393058	01295	SN74LS04N	1	1	
U 15	*	IC 4 X 8 EPROM (PROGRAMMED)	655605	89536	655605	1		
U 16	*	IC,LSTTL,QUAD 2 INPUT OR GATE	393108	01295	SN74LS32N	1	1	
U 17	*	IC,TTL,QUAD BUFFER W/3-STATE OUTPUT	473728	12040	DM74125N	1	1	
XU 1, 10		SOCKET,DIP,0.100 CTR,24 PIN	643999	89536	643999	2		
XU 2, 11		SOCKET,DIP,0.100 CTR,40 PIN	429282	09922	DILB40P-108	2		
XU 15		SOCKET,DIP,0.100 CTR,24 PIN	376236	91506	324-AG39D	1	1	
Y 1	*	CRYSTAL,6MHZ,+-0.01%,HC-18/U	461665	89536	461665	1		
Z 1, 2		RES,NET,SIP,8 PIN,7 RES,22K,+-2%	500041	89536	500041	2		
Z 3, 4		RES,NET,SIP,8 PIN,7 RES,4.7K,+-2%	412916	80031	95081002CL	2		
Z 5, 6		RES,NET,DIP,14 PIN,7 RES,10K,+-5%	364000	01121	314	2		

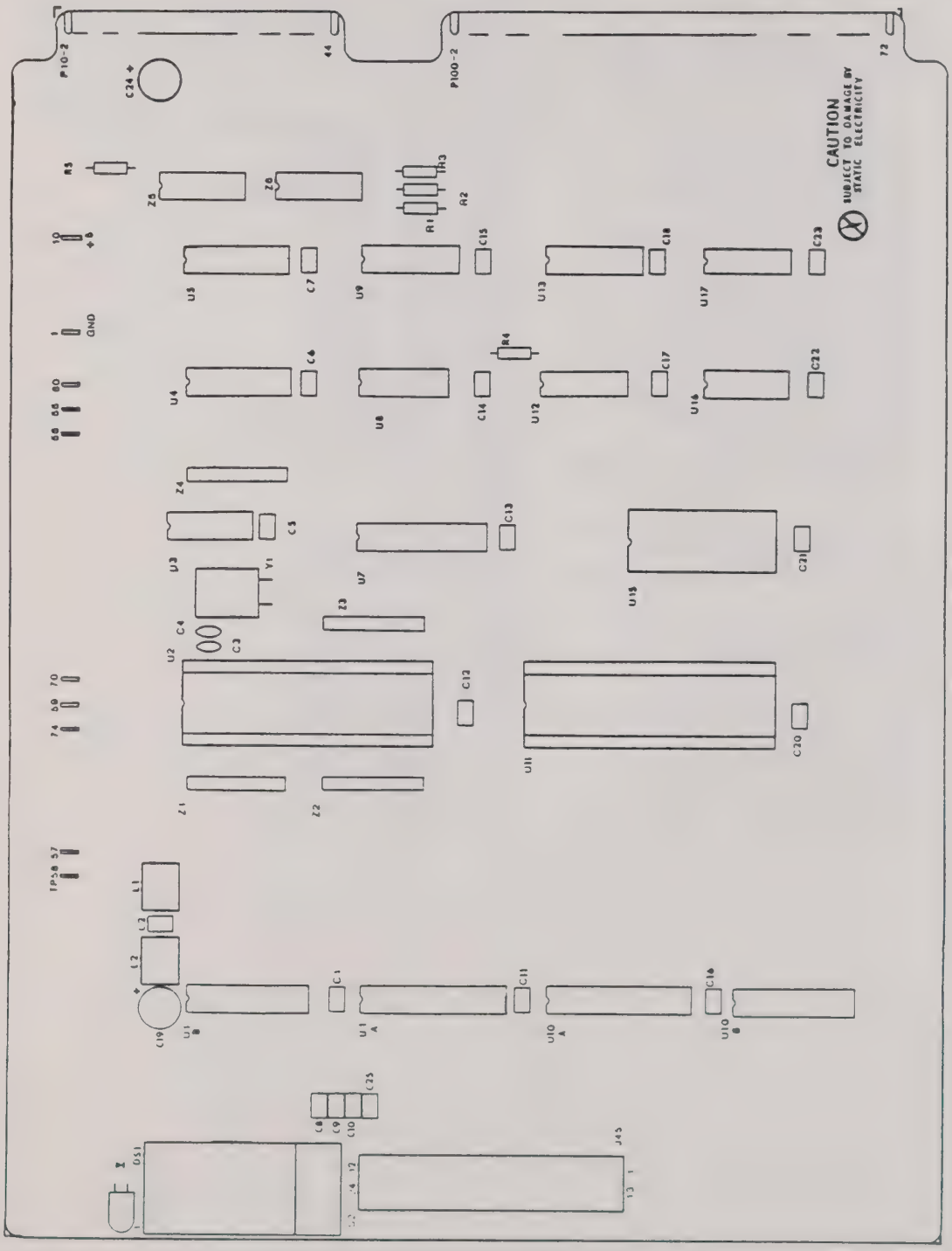
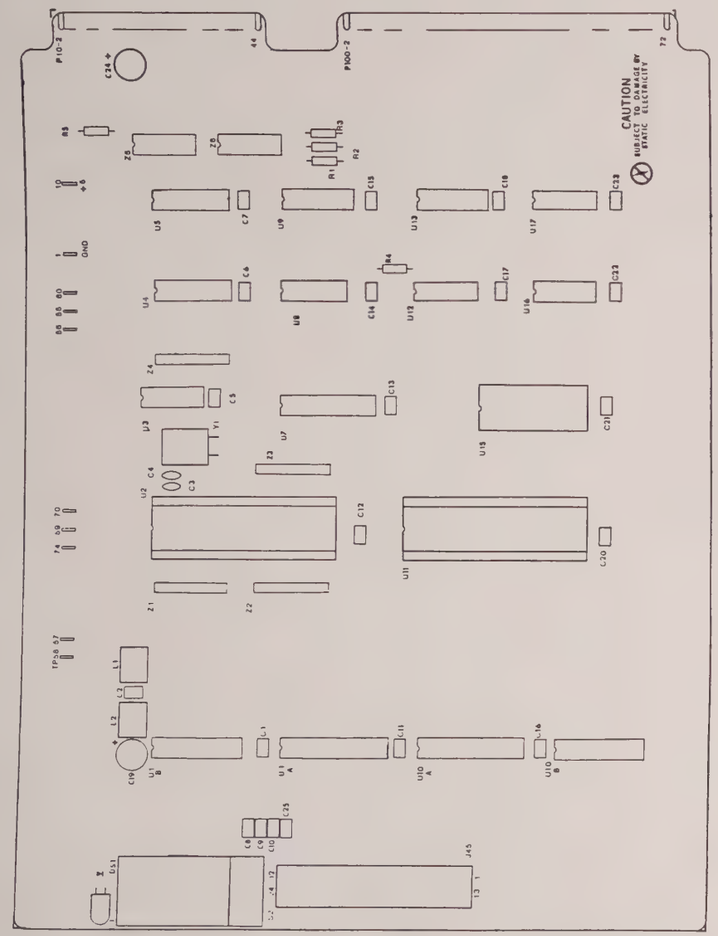


Figure 342-2. 2280A-342 IEEE-488 Interface PCA



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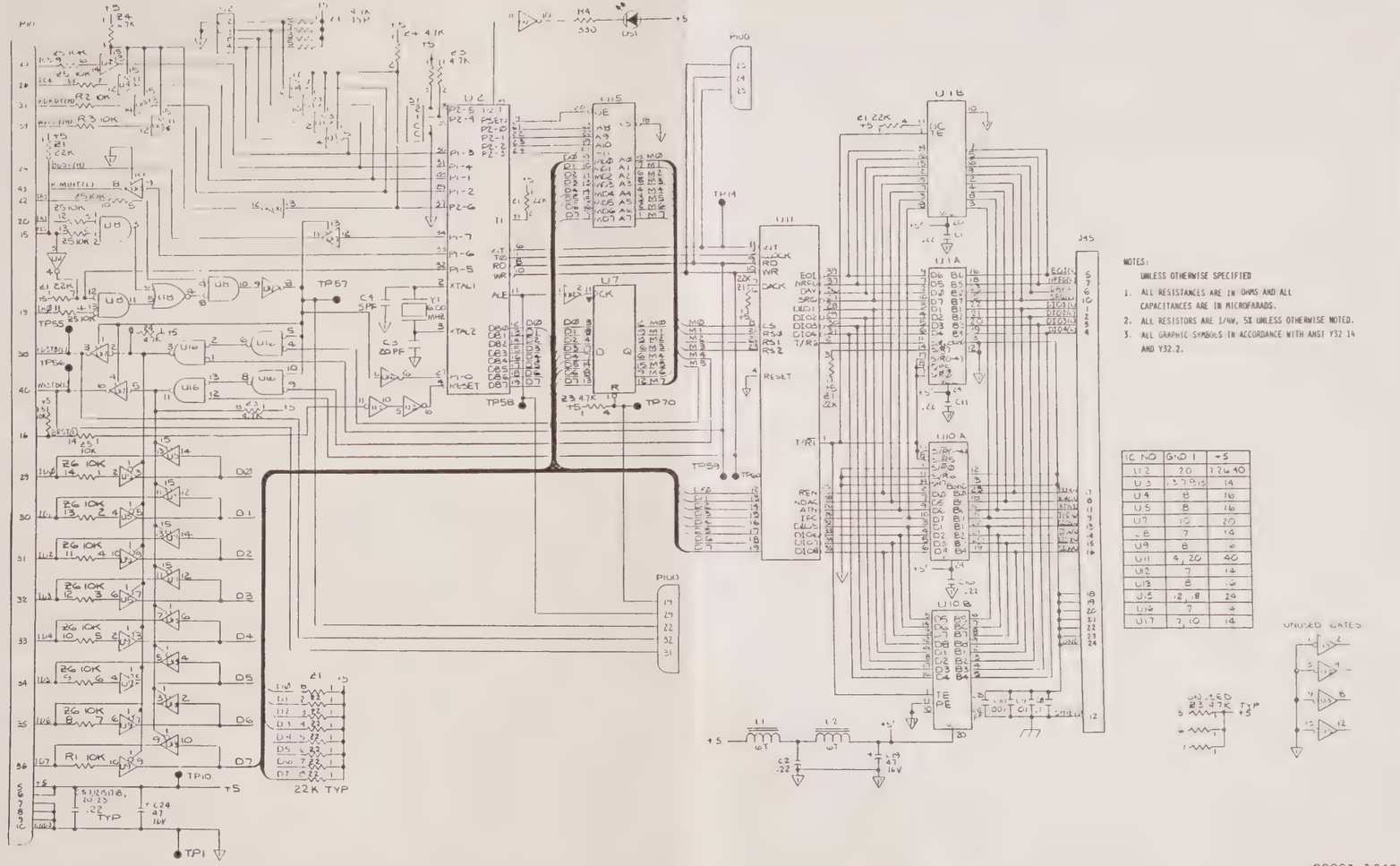
NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCES ARE IN OHMS AND ALL CAPACITANCES ARE IN MICROFARADS.
2. ALL RESISTORS ARE 1/4W, 5% UNLESS OTHERWISE NOTED.
3. ALL GRAPHIC SYMBOLS IN ACCORDANCE WITH ANSI Y32 14 AND Y32.2.
UNUSED GATES

IC NO	GND	+5
U1	20	1,2 & 40
U3	7,9,13	14
U4	8	16
U5	8	16
U7	10	20
U8	7	14
U9	8	16
U11	4, 20	40
U12	7	14
U13	8	16
U15	12, 18	24
U16	7	14
U17	7, 10	14

2280A-1042

Figure 342-2. IEEE-488 Interface Schematic Diagram

SECTION 11

APPENDICES

CONTENTS

Appendix A Specifications 11A-1
Appendix B Fluke Sales Offices and Service Centers 11B-1
Appendix C Manual Change Information 11C-1
Appendix D Differences between 2280B/2280A and 2280B/2285B . 11D-1

GENERAL SPECIFICATIONS

Channel Capacity
- Mainframe ..... 100 Analog or 120 Digital
- 2280B System ..... 1500 maximum
- 2285B System ..... 100 maximum

Program Memory ..... Nonvolatile, with 90 day typical, 30 day minimum battery backup

Display ..... 40 characters, alphanumeric

Printer
- Printing ..... 40 characters/line, 5X7 dot matrix, 6.7 lines/inch
- Plotting ..... Up to 4 channels/line
- Resolution ..... 276 discrete points, 11.2 lines/inch
- Paper ..... Thermosensitive paper roll, NCR T1302 or JUJO 50CM-A, 4000 lines/roll

Master Alarm Relay ..... Normally open, 2.8 VA max

Hardware Trigger Input ..... Accepts an open-collector NPN transistor or contact closure input. Low to high transition triggers any scan group so programmed.

Scanning Speed
Dependent on system configuration and programming

System Scanning Speed in Channels per Second

A/D Converters in System	DC Voltage Readings	Thermocouple and RTD Readings
1	16	15
2	30	26
3	42	35
4	56	40
5	65	44

Power
- AC ..... 100, 120, 220, Vac ±10%, 240V ac +4%, -10%
  50 or 60 Hz
- DC ..... 12V dc (10.5 to 20V dc)
  - Min. Startup Voltage ... 11.2V dc

Less than 120 Watts

Temperature
- Operating ..... 0 to 50°C
  (without Cartridge Tape Option)
- Operating ..... 0 to 40°C
  (with Cartridge Tape Option)
- Storage ..... -25 to 60°C

Humidity (non-condensing)
- 0 to 25°C ..... <95%
- 25 to 40°C ..... <75%
- 40 to 50°C ..... <45%

Weight ..... 20-29 kg (45-66 lbs), depending on configuration

Dimensions ..... 22.23 x 43.94 x 66.17 (cm)
H W D
9.35 x 17.30 x 26.05 (in)

Altitude
- Operating ..... 3050M (10,000 feet)
- Non-operating ..... 12,200M (40,000 feet)

Shock and Vibration ..... Meets MIL-T-28800C Class 5

Table 11A-1. 2280A-160 AC Voltage Input Connector Specifications

Channels	10 Vac, 10 Vdc
Terminals	40 (2 per channel)
AC Voltage	
Range	5V to 250V RMS
Resolution	0.1V ac
Maximum	250V RMS between two terminals
Frequency Range	45 Hz to 450 Hz
Accuracy	See accuracy section: AC Voltage Measurement
Conversion Method	1/2 wave, average responding, calibrated to indicate the RMS value of a sine wave.
DC Voltage	
Ranges and Accuracy	Determined by the Thermocouple/DC Volts Scanner (option 162). See Table 11A-3.
Maximum Input	250V dc or ac RMS between any two terminals
Maximum Common Mode Voltage	250V dc or ac RMS between terminals or between a terminal and ground.
Compatibility	Attaches to the Thermocouple/DC Volts Scanner (option 162).
Temperature	
Operating	-20 to 70°C
Storage	-55 to 75°C
Relative Humidity (without condensation)	
Below 25°C	<= 95%
25 to 40°C	<= 75%
40 to 50°C	<= 45%
50 to 70°C	<= 40%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-2. 2280A-161 High Performance A/D Converter Specifications

Dynamic Range (internal)	±131,071 counts at 50Hz ±109,226 counts at 60Hz
Common Mode Rejection (with 100 ohm imbalance)	170 dB at 50Hz ±0.1% 170 dB at 60Hz ±0.1% 160 dB at dc
Normal Mode Rejection	60 dB at 50Hz ±0.1% or 60Hz ±0.1%
Isolation	250V dc or ac RMS between 2280A-161 and any other module.
Measurement Method	Dual slope, integrating over 1 line cycle
Zero Stability	Automatic zero
Ranges, Resolution, Accuracy	Determined by Scanner (see tables 162-1 and 163-1) and application. See Accuracy sections: Temperature Measurement Using Thermocouples Temperature Measurement Using RTD's DC Voltage Measurement AC Voltage Measurement DC Current Measurement Resistance Measurement Strain Measurement
Temperature	
Operating	-20 to 70°C
Storage	-55 to 75°C
Relative Humidity (without condensation)	
Below 25°C	<= 95%
25 to 40°C	<= 75%
40 to 50°C	<= 45%
50 to 70°C	<= 40%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-3. 2280A-162 Thermocouple/DC Volts Scanner Specifications

Channels	20
Poles per Channel	3 (HI, LO, SHIELD)
Input Impedance	
64 mV and 512 mV Ranges	>200 Mohm in parallel with 6800 pF
8V and 64V Ranges	10 Mohm
Voltage Offset (max)	1 microvolt
Ranges and Displayed Resolution	
64 mV Range	1uV
512 mV Range	10uV
8V Range	100uV
64V Range	1mV
Accuracy	Determined by application. See Accuracy sections: Temperature Measurement Using Thermocouples DC Voltage Measurement AC Voltage Measurement DC Current Measurement Strain Measurement
Zero Stability	Automatic Zero
Input Isolation	250V dc or ac RMS between any two channels or any channel and ground
Overload without Damage	250V dc or 250V ac RMS
Common Mode Voltage (max)	250V dc or ac RMS between any 2 terminals or a terminal and ground
Common Mode Rejection	170 dB at 50Hz ±0.1%
(with 100 ohm imbalance)	170 dB at 60Hz ±0.1%
	160 dB at dc
Normal Mode Rejection	60 dB at 50Hz ±0.1% or 60Hz ±0.1%
Temperature	
Operating	-20 to 70°C
Storage	-55 to 75°C
Relative Humidity (without condensation)	
Below 25°C	<= 95%
25 to 40°C	<= 75%
40 to 50°C	<= 45%
50 to 70°C	<= 40%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-4. 2280B-163 RTD/Resistance Scanner Specifications

Channels	20
Poles per Channel	4 (HI EXCITATION, HI, LO, LO EXCITATION)
Common Return Poles	2 (channels 0-9 LO COM, channels 10-19 LO COM)
Measurement Modes (3)	4-Wire (4W) (no reed resistance errors). 3-Wire Accurate (3WA) (no reed resistance errors. Channels in a decade share a common return). 3-Wire isolated (3WCM) (one reed resistance in measurement path).
Measurement Mode Selection	2 jumpers select scanner measurement mode
Current Sources	2 (1 mA, 32 uA)
Resistance Ranges, Resolution, and Excitation	
Range	256 ohm
Internal Resolution	2.4 mohm
Excitation	1 mA
Range	2048 ohm
Internal Resolution	19 mohm
Excitation	1 mA
Range	64 kohm
Internal Resolution	0.6 ohm
Excitation	32 uA
Accuracy	Determined by application. See Sections: Temperature Measurement Using RTD's Resistance Measurement
Zero Stability	Automatic zero
Input Channel Isolation	
4-Wire (4W)	250V dc or ac RMS between any two channels
3-Wire Accurate (3WA)	250V dc or ac RMS between decades of channels
3-Wire Isolated (3WCM)	250V dc or ac RMS between any two channels
Overload without Damage	30V dc or 24V ac RMS between any two terminals of a channel
Common Mode Isolation	250V dc or ac RMS between scanners, between decades of channels, or between channels within a decade for 4-Wire (4W) and 3-Wire isolated (3WCM) measurement modes, 30V dc or 24V ac RMS between any terminals in the same decade except between LO COM's for the 3-Wire Accurate (3WA) measurement mode
Temperature	
Operating	-20 to 70°C
Storage	-55 to 75°C
Relative Humidity (without condensation)	
Below 25°C	<= 95%
25 to 40°C	<= 75%
40 to 50°C	<= 45%
50 to 70°C	<= 40%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-5. 2280A-164 Transducer Excitation Module Specifications

Outputs	5 constant current sources 1 constant voltage source
Channels of Excitation	20, selectable in groups of 4 for either voltage or current outputs
Common Mode Voltage	No user-applied common mode voltage allowed. All sensors must be isolated.
4-Wire Resistance Measurements	5 constant current sources. Each source excites up to 4 channels.
3-Wire Resistance and Strain Gage Measurements	Any combination of 1/4, 1/2, and/or Full Bridge strain gages or 3-wire RTD's with voltage excitation and user-supplied bridge completion resistors.
Current Excitation	
Excitation Current	1.0mA
Accuracy	
Initial Setting	0.005%
Temperature 15 to 35°C	0.015%
Time since calibration	90 days
Temperature 15 to 35°C	0.030%
Time since calibration	1 year
Temperature -20 to 70°C	0.050%
Time since calibration	1 year
Temperature Coefficient (<15 or >35°C)	10ppm per °C
Maximum Compliance Voltage	0.6V
Voltage Excitation	
Excitation Voltage	switch selectable to 2.0 V or 4.0 V dc
2 Volt Accuracy	
Initial Setting	0.0025%
Temperature 15 to 35°C	0.03%
Time since calibration	90 days
Temperature 15 to 35°C	0.04%
Time since calibration	1 year
Temperature -20 to 70°C	0.05%
Time since calibration	1 year
4 Volt Accuracy	
Initial Setting	0.0035%
Temperature 15 to 35°C	0.015%
Time since calibration	90 days
Temperature 15 to 35°C	0.030%
Time since calibration	1 year
Temperature -20 to 70°C	0.05%
Time since calibration	1 year
Temperature Coefficient (<15 or >35°C)	7ppm per °C
Maximum Current	250 mA
Accuracy	Determined by application. See the Accuracy Specifications section.

Temperature
    Operating ..... -20 to 70°C
    Storage ..... -55 to 75°C
Relative Humidity (without condensation)
    Below 25°C ..... <= 95%
    25 to 40°C ..... <= 75%
    40 to 50°C ..... <= 45%
    50 to 70°C ..... <= 40%
Altitude
    Non-Operating ..... 40,000 feet
    Operating ..... 10,000 feet
Shock and Vibration ..... Meets MIL-T-28800C, Class 5 Standards

Table 11A-6. 2280B-167 Counter/Totalizer Specifications

Channels	6
Functions	Event counting and frequency measurement selectable by channel pairs
Timebase	
Frequency	10MHz
Accuracy	± 0.01%
Input Signals	
Types	TTL, CMOS, contacts, and analog waveforms
Minimum Pulse Width	1.25usec
Minimum Signal Amplitude	175mV RMS 0.5V p-p sine wave 0.35V p-p square wave
Maximum Signal Amplitude	±15V dc or ac peak
Adjustments	Signal threshold, deadband, and contact debounce
Frequency Measurement	
Minimum Frequency	2Hz
Maximum Frequency	400kHz
Accuracy	Timebase accuracy ± 1 display digit
Totalize Measurement	
Maximum Counts	8,388,607
Counting Rate	dc to 400kHz
Operation	Count is reset after each scan
Isolation	30V dc or ac RMS between any terminal and ground. No isolation between channels.
Power Consumption	4.0 watts maximum
Temperature	
Operating	-20 to 70°C
Storage	-55 to 75°C
Relative Humidity (without condensation)	
Below 25°C	<= 95%
25 to 40°C	<= 75%
40 to 50°C	<= 45%
50 to 70°C	<= 40%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-7. 2280A-168 Digital I/O Specifications

Isolation	30V dc or ac RMS between any terminal and ground.
Inputs	
Channels	20 single bit, or one 5 BCD digit word, or one 17-bit binary word
Type	Low Power Schottky TTL
Maximum Input Voltage	6V
Outputs	
Channels	20 single bit
Type	Open-collector, diode clamped, NPN transistors
Output Drive	100mA with 1V drop
Maximum Voltage on Output	30V dc
Temperature	
Operating	-20 to 70°C
Storage	-55 to 75°C
Relative Humidity (without condensation)	
Below 25°C	<= 95%
25 to 40°C	<= 75%
40 to 50°C	<= 45%
50 to 70°C	<= 40%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-8. 2280A-169 Status Output Connector Specifications

Outputs	20
Terminals	2 per channel
Compatibility	Connects to Digital I/O (option 168)
Temperature	
Operating	-20 to 70°C
Storage	-55 to 75°C
Relative Humidity (without condensation)	
Below 25°C	<= 95%
25 to 40°C	<= 75%
40 to 50°C	<= 45%
50 to 70°C	<= 40%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-9. 2280B-170 Analog Output Specifications

Channels	4
Terminals	5 per channel
Accuracy	±0.1% of range
Time since calibration	90 days
Operating Temperature	15 to 35°C
Accuracy	±0.2% of range
Time since calibration	1 year
Operating Temperature	15 to 35°C
Accuracy	±0.4% of range
Time since calibration	1 year
Operating Temperature	-20 to 70°C
Noise	< 0.02% of range in a 10kHz bandwidth
Voltage Outputs	
Ranges	-5 to +5V, 0 to +10V
Resolution	2.5mV/count
Maximum Current	2mA
Capacitive Load	10,000 pF maximum
Output Protection	short-circuit protected
Current Output	
Range	4 to 20mA
Resolution	4uA
Maximum Compliance Voltage	10V
Maximum External Voltage	±24V
Isolation	30V dc or ac RMS between any terminal and ground. No isolation between channels. Current outputs share a common return.
Power Consumption	4.1 watts maximum
Temperature	
Operating	-20 to 70°C
Storage	-55 to 75°C
Relative Humidity (without condensation)	
Below 25°C	<= 95%
25 to 40°C	<= 75%
40 to 50°C	<= 45%
50 to 70°C	<= 40%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-10. 2280A-171 Current Input Connector Specifications

Channels	20
Terminals	2 per channel
Shunt Resistor	8 ohms ±0.02 ohm
Measurement Range	64mA
Overload without Damage	250mA
Common Mode Voltage	250V dc or ac RMS between any two channels or between a channel and ground.
Accuracy	0.25% Input ± 4uA
Time since A/D calibration	90 days
Resolution (displayed)	1uA
Compatibility	Attaches to Thermocouple/DC Volts Scanner (option 162).
Temperature	
Operating	-20 to 70°C
Storage	-55 to 75°C
Relative Humidity (without condensation)	
Below 25°C	<= 95%
25 to 40°C	<= 75%
40 to 50°C	<= 45%
50 to 70°C	<= 40%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-11. 2280A-174 Transducer Excitation Connector Specifications

Channels	20
Terminals	5 per channel
Programming	5 Jumpers select voltage or current excitation on 5 groups of 4 channels.
Compatibility	Attaches to Transducer Excitation Module (option 164)
Temperature	
Operating	-20 to 70°C
Storage	-55 to 75°C
Relative Humidity (without condensation)	
Below 25°C	<= 95%
25 to 40°C	<= 75%
40 to 50°C	<= 45%
50 to 70°C	<= 40%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-12. 2280A-175 Isothermal Input Connector Specifications

Channels	20
Terminals	60 (HI, LO, SHIELD per channel)
Reference Junction	
Accuracy	<0.1 °C
Stability	±0.005°C per °C
Maximum Voltage Rating	250V dc or ac RMS from any terminal to any other terminal or ground.
Temperature	
Operating	-20 to 70°C
Storage	-55 to 75°C
Relative Humidity (without condensation)	
Below 25°C	<= 95%
25 to 40°C	<= 75%
40 to 50°C	<= 45%
50 to 70°C	<= 40%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-13. 2280A-176 Voltage Input Connector Specifications

Channels	20
Terminals	60 (HI, LO, SHIELD per channel)
Maximum Voltage Rating	250V dc or ac RMS from any terminal to any other terminal or ground.
Temperature	
Operating	-20 to 70°C
Storage	-55 to 75°C
Relative Humidity (without condensation)	
Below 25°C	<= 95%
25 to 40°C	<= 75%
40 to 50°C	<= 45%
50 to 70°C	<= 40%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-14. 2280B-177 RTD/Resistance Input Connector Specifications

Channels	20
Terminals	100 (HI EXC, HI, LO, LO EXC, and LO COM per channel)
Maximum Voltage Rating and mating RTD/Resistance Scanner Mode	
163 Measurement Mode	4-Wire (4W)
Ratings	250V dc or ac RMS between any two channels or any channel and ground, 30V dc or 24V ac RMS between any terminals of a channel
163 Measurement Mode	3-Wire Accurate (3WA)
Ratings	250V dc or ac RMS between channels in different decades or between channels in a decade and ground, 30V dc or 24V ac RMS between any terminals within a decade except between LO COM's. (LO COM's of channels within a decade are connected together internally).
163 Measurement Mode	3-Wire isolated = 3-Wire with Common Mode (3WCM)
Ratings	same as for 4-Wire
Compatibility	Attaches to RTD/Resistance Scanner (option 163)
Temperature	
Operating	-20 to 70°C
Storage	-55 to 75°C
Relative Humidity (without condensation)	
Below 25°C	<= 95%
25 to 40°C	<= 75%
40 to 50°C	<= 45%
50 to 70°C	<= 40%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-15. 2280A-179 Digital/Status Input Connector Specifications

Channels	20 single bit, or one 5 BCD digit word, or one 17-bit binary word
Terminals	72
Maximum Input Voltage	6V dc
Isolation	30V dc or ac RMS between any terminal and ground.
Compatibility	Attaches to Digital I/O (option 168)
Temperature	
Operating	-20 to 70°C
Storage	-55 to 75°C
Relative Humidity (without condensation)	
Below 25°C	<= 95%
25 to 40°C	<= 75%
40 to 50°C	<= 45%
50 to 70°C	<= 40%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-16. 2280A-211 Advanced Math Specifications

Functions	Absolute value, square root, exponential, sine, cosine, tangent, inverse sine, inverse cosine, inverse tangent, common logarithm, natural logarithm, table interpolation, integer part, maximum value, minimum value, standard deviation, group average, and elapsed time.
Logical Operators	AND, OR, NOT, EXCLUSIVE-OR
Relational Operators	<, <=, >, >=, =, /=
Interpolation Tables	Up to 10 user-defined.
Temperature	
Operating	0 to 50°C
Storage	-25 to 60°C
Humidity (without condensation)	
0 to 25°C	<95%
25 to 40°C	<75%
40 to 50°C	<45%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-17. 2280A-214 Cartridge Tape Specifications

Drive	2 head, 2 track
Tape	DC100A cartridge
Tape Speeds	
Read and Write	30 inches/second
Search and Rewind	77 inches/second
Encoding Format	Manchester Phase Encoding
Capacity	500 Kbytes nominal (500 blocks) divided into 49 files
Record Size	1024 bytes
Density	200 bytes/inch (1600 bits/inch)
Compatibility	Readable using QANTEX model 1000 tape drive
Temperature	
Operating	0 to 40°C
Storage	-25 to 60°C
Humidity (without condensation)	
no tape installed	
0 to 25°C	<95%
25 to 40°C	<75%
tape installed	
0 to 40°C	20% to 80%
Altitude	
Non-Operating	40,000 feet
Operating	10,000 feet
Shock and Vibration	Meets MIL-T-28800C, Class 5 Standards

Table 11A-18. 2280A-341 RS-232-C Interface Specifications

Interface Type	RS-232-C
Baud Rates	110, 300, 600, 1200, 4800, 9600
Character Format	7 bits plus one parity bit, one start bit, and one stop bit (except at 110 baud where there are 2 stop bits)
Parity	odd, even, or none
Output Signals	Request To Send Data Terminal Ready Transmit Data
Input Signals	Clear To Send Data Set Ready Received Line Signal Detect
Other Signals	Signal Ground Protective Ground
Transmission Flow Control	Sending a control-S character to the interface halts the transmission (output) of data until a control-Q is sent to restart it. De-asserting (setting false) a Clear To Send, Data Set Ready, or Received Line Signal Detect input signal halts the transmission (output) of data until the three signals are asserted (true).

Table 11A-19. 2280A-342 IEEE-488 Interface Specifications

Operating Modes	Addressable talker/listener, or talker only (switch selectable). Responds to serial poll.	
IEEE-488 Functional Subsets	SH1	Source Handshake (complete capability)
	AH1	Acceptor Handshake (complete capability)
	T5	Talker (talk only included)
	TE0	Talker Extended (single address only)
	L4	Listener (listen only excluded)
	LE0	Listener Extended (single address only)
	SR1	Serial Poll
	RL1	Remote Local (local lockout included)
	DC1	Device Clear (complete capability)
	E2	Electrical (tri-state drivers)
	PP0	Parallel Poll (no capability)
	DT0	Device Trigger (no capability)
	C0	Controller (no capability)

ACCURACY SPECIFICATIONS

Temperature Measurement Using Thermocouples

Hardware Used ..... 2280A-161 High Performance A/D
2280A-162 Thermocouple/DC Volts Scanner
2280A-175 Isothermal Input Connector

Accuracy In ±°C

Thermocouple Type (Sensor Temperature Range) Sensor Temperature (°C)	Time Since A/D Calibration (Operating Temperature in °)		
	90 Days (15 to 35)	1 Year (15 to 35)	1 Year (-20 to +70)
J (-200 to 760°C)			
-100 to -25	0.45	0.5	0.8
-25 to 760	0.35	0.4	0.7
K (-275 to 1350°C)			
0 to 900	0.4	0.45	0.7
900 to 1350	0.52	0.65	1.3
T (-230 to 400°C)			
-100 to 75	0.58	0.65	1.1
75 to 150	0.35	0.39	0.7
150 to 400	0.3	0.34	0.6
E (-250 to 900°C)			
-100 TO -25	0.47	0.54	0.9
-25 TO 750	0.3	0.33	0.6
750 TO 900	0.33	0.4	0.8
R (0 to 1767°C)			
250 to 450	0.9	1.0	1.3
450 to 1767	0.8	0.9	1.4
S (0 to 1767°C)			
200 to 1767	0.97	1.1	1.6
B (200 to 1820°C)			
600 to 800	1.4	1.6	1.9
800 to 1820	0.96	1.1	1.3
N (-200 to 400°C) (For 28 gauge thermocouple wire)			
-100 to 150	0.6	0.7	1.1
150 to 400	0.4	0.44	0.7
C (0 to 2315°C)			
200 to 1000	0.57	0.66	0.94
1000 to 2000	0.90	1.2	2.1
2000 to 2315	1.3	1.7	2.9

JDIN (-200 to 900°C)			
-100 to -25	0.5	0.56	0.9
-25 to 900	0.4	0.45	0.7
TDIN (-200 to 600°C)			
0 to 200	0.48	0.53	0.8
200 to 600	0.37	0.41	0.7

Temperature Measurement Using RTD's

Hardware Used ..... 2280A-161 High Performance A/D
2280B-163 RTD/Resistance Scanner
2280B-177 RTD/Resistance Input Connector

Performance

RTD Type, Scanner Range, and Scanner Measurement Mode (sensor temperature range)	90 Days Since A/D Calibration 18 to 28°C Operating Temperature Temperature Shift dT/dt < 1°C / 10min		
Sensor Temperature (°C)	Accuracy	Resolution	Repeatability
Platinum 385 DIN, High Resolution, 4-Wire (4W), and Platinum 390, User-defined High Resolution, 4-Wire (4W) (-200 to 425°C)			
-200 to 150	0.09°C*	0.006°C	0.03°C
150 to 425	0.13°C	0.006°C	0.04°C
Platinum 392, User-defined High Resolution, 4-Wire (4W) (-200 to 425°C)			
-200 to 150	0.08°C*	0.006°C	0.03°C
150 to 425	0.12°C	0.006°C	0.04°C
Platinum 385 DIN, High Temperature, 4-Wire (4W), and Platinum 390, User-defined High Temperature, 4-Wire (4W) (-200°C to probe limit)			
-200 to 600	0.25°C	0.05°C	0.14°C
Platinum 392, User-defined High Temperature, 4-Wire (4W) (-200°C to probe limit)			
-200 to 600	0.24°C	0.05°C	0.14°C
10 Ohm Copper, 4-Wire (4W) (full range)	0.28°C	0.06°C	0.16°C
Platinum 385 DIN, 390, 392, 3-Wire Accurate (3WA) Full range: add °C per ohm lead R to 4W specs.	+0.007°C	+0.001°C	
10 Ohm Copper, 3-Wire Accurate (3WA) Full range: add °C per ohm lead R to 4W specs.	+0.065°C	+0.008°C	
Platinum 385 DIN, 390, 392, 3-Wire Isolated (3WCM) Full range: add °C to 3WA specs	+1.97°C	+1.97°C	

10 Ohm Copper, 3-Wire Isolated (3WCM) Full range: add °C to 3WA specs	+18.2°C	+18.2°C

*NOTE: An ice-point initialization allows Platinum RTD's with user-defined linearization to have accuracies of 0.05°C (392Pt) and 0.06°C (390Pt), and 385 DIN RTD's to have an accuracy of 0.05°C + probe conformity.

Performance

RTD Type, Scanner Range, and Scanner Measurement Mode (sensor temperature range) Sensor Temperature (°C)	90 Days Since A/D Calibration 15 to 35°C Operating Temperature Temperature Shift dT/dt < 1°C / 10min Accuracy	Resolution	Repeatability
Platinum 385 DIN, High Resolution, 4-Wire (4W), and Platinum 390, User-defined High Resolution, 4-Wire (4W) (-200 to 425°C)			
-200 to 150	0.10°C	0.006°C	0.04°C
150 to 425	0.15°C	0.006°C	0.04°C
Platinum 392, User-defined High Resolution, 4-Wire (4W) (-200 to 425°C)			
-200 to 150	0.09°C	0.006°C	0.04°C
150 to 425	0.14°C	0.006°C	0.04°C
Platinum 385 DIN, High Temperature, 4-Wire (4W), and Platinum 390, User-defined High Temperature, 4-Wire (4W) (-200°C to probe limit)			
-200 to 600	0.27°C	0.05°C	0.16°C
Platinum 392, User-defined High Temperature, 4-Wire (4W) (-200°C to probe limit)			
-200 to 600	0.26°C	0.05°C	0.16°C
10 Ohm Copper, 4-Wire (4W) (full range)	0.3°C	0.06°C	0.16°C
Platinum 385 DIN, 390, 392, 3-Wire Accurate (3WA) Full range: add °C per ohm Lead R to 4W specs.	+0.007°C	+0.001°C	
10 Ohm Copper, 3-Wire Accurate (3WA) Full range: add °C per ohm Lead R to 4W specs.	+0.065°C	+0.008°C	

Platinum 385 DIN, 390, 392, 3-Wire Isolated (3WCM)
Full range: add °C
to 3WA specs +1.97°C +1.97°C

10 Ohm Copper, 3-Wire Isolated (3WCM)
Full range: add °C
to 3WA specs +18.2°C +18.2°C
Performance

RTD Type, Scanner Range, and Scanner Measurement Mode (sensor temperature range)	1 Year Since A/D Calibration 15 to 35°C Operating Temperature Temperature Shift dT/dt < 1°C / 10min	
Sensor Temperature (°C	Accuracy	Resolution
Platinum 385 DIN, High Resolution, 4-Wire (4W), and Platinum 390, User-defined High Resolution, 4-Wire (4W) (-200 to 425°C)		
-200 to 150	0.11°C	0.006°C
150 to 425	0.16°C	0.006°C
1 Platinum 392, User-defined High Resolution, 4-Wire (4W) (-200 to 425°C)		
-200 to 150	0.10°C	0.006°C
150 to 425	0.15°C	0.006°C
Platinum 385 DIN, High Temperature, 4-Wire (4W), and Platinum 390, User-defined High Temperature, 4-Wire (4W) (-200°C to probe limit)		
-200 to 600	0.28°C	0.05°C
Platinum 392, User-defined High Temperature, 4-Wire (4W) (-200°C to probe limit)		
-200 to 600	0.27°C	0.05°C
10 Ohm Copper, 4-Wire (4W) (full range)	0.3°C	0.06°C

Platinum 385 DIN, 390, 392, 3-Wire Accurate (3WA)
Full range: add °C
per ohm Lead R
to 4W specs. +0.008°C

10 Ohm Copper, 3-Wire Accurate (3WA)
Full range: add °C
per ohm Lead R
to 4W specs. +0.073°C

Platinum 385 DIN, 390, 392, 3-Wire Isolated (3WCM)
Full range: add °C
to 3WA specs +2.53°C

10 Ohm Copper, 3-Wire Isolated (3WCM) Full range: add °C to 3WA specs	+23.4°C

Performance

RTD Type, Scanner Range, and Scanner Measurement Mode (sensor temperature range) Sensor Temperature (°C)	1 Year Since A/D Calibration -20 to 70°C Operating Temperature Temperature Shift dT/dt < 1°C / 10min Accuracy	Resolution
Platinum 385 DIN, High Resolution, 4-Wire (4W), and Platinum 390, User-defined High Resolution, 4-Wire (4W) (-200 to 425°C)		
-200 to 150	0.19°C	0.006°C
150 to 425	0.29°C	0.006°C
Platinum 392, User-defined High Resolution, 4-Wire (4W) (-200 to 425°C)		
-200 to 150	0.18°C	0.006°C
150 to 425	0.28°C	0.006°C
Platinum 385 DIN, High Temperature, 4-Wire (4W), and Platinum 390, User-defined High Temperature, 4-Wire (4W) (-200°C to probe limit)		
-200 to 600	0.44°C	0.05°C
Platinum 392, User-defined High Temperature, 4-Wire (4W) (-200°C to probe limit)		
-200 to 600	0.43°C	0.05°C
10 Ohm Copper, 4-Wire (4W) (full range)	0.4°C	0.06°C
Platinum 385 DIN, 390, 392, 3-Wire Accurate (3WA) Full range: add °C per ohm Lead R to 4W specs.	+0.010°C	
10 Ohm Copper, 3-Wire Accurate (3WA) Full range: add °C per ohm Lead R to 4W specs.	+0.096°C	

Platinum 385 DIN, 390, 392, 3-Wire Isolated (3WCM)
Full range: add °C
to 3WA specs +2.52°C

10 Ohm Copper, 3-Wire Isolated (3WCM)
Full range: add °C
to 3WA specs +23.4°C

Temperature Measurement Using RTD's

Hardware Used .... 2280A-161 High Performance A/D
2280A-164 Transducer Excitation Module
2280A-174 Transducer Excitation Connector
(with current excitation selected)
2280A-162 Thermocouple/DC Volts Scanner
Choice of Connector:
2280A-175 Isothermal Input
2280A-176 Voltage Input
2280A-160 AC Voltage Input

Performance

RTD Type and Scanner Range (sensor temperature range) Sensor Temperature (°C)	90 Days Since Calibration 15 to 35°C Operating Temperature		
	Accuracy	Resolution	Repeatability
Platinum 390 and 392, User-defined (-200°C to probe limit)			
-200 to 200	0.1°C	0.02°C	0.08°C
200 to 600	0.15°C	0.02°C	0.1°C
Platinum 385 DIN (-200°C to probe limit)			
-200 to 600	0.2°C	0.013°C	0.08°C
10 Ohm Copper (full range)	1.0°C	0.1°C	0.2°C

DC Voltage Measurement Accuracy

Hardware Used ..... 2280A-161 High Performance A/D
2280A-162 Thermocouple/DC Volts Scanner
Choice of Connector:
2280A-175 Isothermal Input
2280A-176 Voltage Input
2280A-160 AC Voltage Input

Accuracy

Range (Internal Resolution)	Time Since A/D Calibration (Operating Temperature in °C) (± % Input ± microvolts)		
	90 Days (15 to 35)	1 Year (15 to 35)	1 Year (-20 to +70)
±64 mV (0.6 uV)	0.005% + 7.0	0.01% + 8.0	0.03% + 9.0
±512 mV (5 uV)	0.005% + 30	0.01% + 40	0.03% + 50
±8V (73 uV)	0.005% + 700	0.01% + 800	0.03% + 900
±64V (0.6 mV)	0.009% + 3mV	0.02% + 4mV	0.05% + 5mV

AC Voltage Measurement Accuracy

Hardware Used ..... 2280A-161 High Performance A/D
2280A-162 Thermocouple/DC Volts Scanner
2280A-160 AC Voltage Input Connector

Performance

Range and Frequencies	90 Days Since A/D Calibration 15 to 35°C Operating Temperature	
	Resolution	Accuracy
5V to 250V ac RMS, 45Hz to 450Hz	0.1V	±1% Input ±.1V

DC Current Measurement Accuracy

Hardware Used ..... 2280A-161 High Performance A/D
2280A-162 Thermocouple/DC Volts Scanner
2280A-171 Current Input Connector

Performance

Range	90 Days Since A/D Calibration 15 to 35°C Operating Temperature	
	Resolution	Accuracy
±64mA	0.6uA	±.25% ±4uA

Resistance Measurement Accuracy

Hardware Used ..... 2280A-161 High Performance A/D
2280B-163 RTD/Resistance Scanner
2280B-177 RTD/Resistance Input Connector

Performance

Scanner Range and Measurement Mode	90 Days Since A/D Calibration, 18 to 28°C Operating Temperature, Temperature Shift dT/dt < 1°C / 10min		
	(mohm)	(±% Input ± mohm)	
	Resolution	Accuracy	Repeatability
256ohm, 4-Wire (4W)	2.4	0.0142% + 5.7	0.0037% + 5.7
2048ohm, 4-Wire (4W)	19	0.0137% + 38	0.0032% + 38
64kohm, 4-Wire (4W)	0.6 ohm	0.055% + 1.2ohm	0.0040% + 1.2ohm**
All, 3-Wire Accurate (3WA)	same as 4W	Add 2.4mohm per ohm lead resistance to 4W specs	Add 0.2mohm per ohm lead resistance to 4W specs
All, 3-Wire Isolated = 3-Wire With Common Mode (3WCM)	same as 4W	Add 0.7 ohm per ohm lead resistance to 3WA specs	Add 0.7 ohm per ohm lead resistance to 3WA specs

**Humidity 15%RH less than listed for the 2280B-163 Scanner

Performance

Scanner Range and Measurement Mode	90 Days Since A/D Calibration, 15 to 35°C Operating Temperature, Temperature Shift dT/dt < 1°C / 10min		
	(mohm)	(±% Input ± mohm)	
	Resolution	Accuracy	Repeatability
256ohm, 4-Wire (4W)	2.4	0.0170% + 5.7	0.0065% + 5.7

2048ohm, 4-Wire (4W)	19	0.0165% + 38	0.0060% + 38
64kohm, 4-Wire (4W)	0.6 ohm	0.06% + 1.2ohm	0.0075% + 1.2ohm**
All, 3-Wire Accurate (3WA)	same as 4W	Add 2.5mohm per ohm lead resistance to 4W specs	Add 0.3mohm per ohm lead resistance to 4W specs
All, 3-Wire Isolated = 3-Wire With Common Mode (3WCM)	same as 4W	Add 0.7 ohm per ohm lead resistance to 3WA specs	Add 0.7 ohm per ohm lead resistance to 3WA specs

**Humidity 15%RH less than listed for the 2280B-163 Scanner

Performance

Scanner Range and Measurement Mode	1 Year Since A/D Calibration 15 to 35°C Operating Temperature Temperature Shift dT/dt < 1°C / 10min	
	Resolution	Accuracy
256ohm, 4-Wire (4W)	2.4mohm	±.0175% Input ±5.7mohm
2048ohm, 4-Wire (4W)	19mohm	±.0170% Input ±38mohm
64kohm, 4-Wire (4W)	1.2ohm	±.06% Input ±1.2ohm
All, 3-Wire Accurate (3WA)	same as 4W	Add 2.8mohm per ohm lead resistance to the 4W specifications
All, 3-Wire Isolated = 3-Wire With Common Mode (3WCM)	same as 4W	Add 0.9ohm to the 3WA specifications

Performance

Scanner Range and Measurement Mode	1 Year Since A/D Calibration -20 to 70°C Operating Temperature Temperature Shift dT/dt < 1°C / 10min	
	Resolution	Accuracy
256ohm, 4-Wire (4W)	2.4mohm	±.0365% Input ±7mohm
2048ohm, 4-Wire (4W)	19mohm	±.0360% Input ±38mohm
64kohm, 4-Wire (4W)	0.6ohm	±.23% Input ±1.2ohm
All, 3-Wire Accurate (3WA)	same as 4W	Add 3.7mohm per ohm lead resistance to the 4W specifications
All, 3-Wire Isolated = 3-Wire With Common Mode (3WCM)	same as 4W	Add 0.9ohm to the 3WA specifications

Resistance Measurement Accuracy

Hardware Used .... 2280A-161 High Performance A/D
2280A-164 Transducer Excitation Module
2280A-174 Transducer Excitation Connector
(with current excitation selected)
2280A-162 Thermocouple/DC Volts Scanner
Choice of Connector:
2280A-175 Isothermal Input
2280A-176 Voltage Input
2280A-160 AC Voltage Input

Performance

Range	90 Days Since Calibration 15 to 35°C Operating Temperature	
	Resolution	Accuracy
64ohm	1mohm	±.02% Input ±7mohm
512ohm	10mohm	±.02% Input ±30mohm

Strain Measurement Accuracy

Hardware Used .... 2280A-161 High Performance A/D
2280A-164 Transducer Excitation Module
2280A-174 Transducer Excitation Connector
(with voltage excitation selected)
2280A-162 Thermocouple/DC Volts Scanner
Choice of Connector:
2280A-175 Isothermal Input
2280A-176 Voltage Input
2280A-160 AC Voltage Input

Performance

Gage Type	90 Days Since Calibration 20 to 30°C Operating Temperature	
	Resolution	Accuracy
Full Bridge	0.25uE	±.05% Input ±2uE
1/2 Bridge	0.5uE	±.05% Input ±13uE
1/4 Bridge	0.5uE	±.05% Input ±25uE

Appendix 11B
Service Centers

List of Abbreviations and Symbols

A or amp	ampere
ac	alternating current
af	audio frequency
a/d	analog-to-digital
assy	assembly
AWG	american wire gauge
B	bel
bcd	binary coded decimal
°C	Celsius
cap	capacitor
ccw	counterclockwise
cer	ceramic
cermet	ceramic to metal(seal)
ckt	circuit
cm	centimeter
cmrr	common mode rejection ratio
comp	composition
cont	continue
crt	cathode-ray tube
cw	clockwise
d/a	digital-to-analog
dac	digital-to-analog converter
dB	decibel
dc	direct current
dmm	digital multimeter
dvm	digital voltmeter
elect	electrolytic
ext	external
F	farad
°F	Fahrenheit
FET	Field-effect transistor
ff	flip-flop
freq	frequency
FSN	federal stock number
g	gram
G	giga (10^9)
gd	guard
Ge	germanium
GHz	gigahenz
gmv	guaranteed minimum value
gnd	ground
H	henry
hd	heavy duty
hf	high frequency
Hz	hertz
IC	integrated circuit
if	intermediate frequency
in	inch(es)
intl	internal
I/O	input/output
k	kilo (10^3)
kHz	kilohertz
kΩ	kilohm(s)
kV	kilovolt(s)
lf	low frequency
LED	light-emitting diode
LSB	least significant bit
LSD	least significant digit
M	mega (10^6)
m	milli (10^{-3})
mA	milliampere(s)
max	maximum
mf	metal film
MHz	megahertz
min	minimum
mm	millimeter
ms	millisecond
MSB	most significant bit
MSD	most significant digit
MTBF	mean time between failures
MTTR	mean time to repair
mV	millivolt(s)
mv	multivibrator
MΩ	megohm(s)
n	nano (10^{-9})
na	not applicable
NC	normally closed
(-) or neg	negative
NO	normally open
ns	nanosecond
opnl ampl	operational amplifier
p	pico (10^{-12})
para	paragraph
pcb	printed circuit board
pF	picofarad
pn	part number
(+) or pos	positive
pot	potentiometer
p-p	peak-to-peak
ppm	parts per million
PROM	programmable read-only memory
psi	pound-force per square inch
RAM	random-access memory
rf	radio frequency
rms	root mean square
ROM	read-only memory
s or sec	second (time)
scope	oscilloscope
SH	shield
Si	silicon
semo	serial number
sr	shift register
Ta	tantalum
tb	terminal board
tc	temperature coefficient or temperature compensating
tcxo	temperature compensated crystal oscillator
tp	test point
u or μ	micro (10^{-6})
uhf	ultra high frequency
us or μs	microsecond(s) (10^{-6})
uut	unit under test
V	volt
v	voltage
var	variable
vco	voltage controlled oscillator
vhf	very high frequency
vlf	very low frequency
W	watt(s)
ww	wire wound
xfmr	transformer
xstr	transistor
xtal	crystal
xtlo	crystal oscillator
Ω	ohm(s)
μ	micro (10^{-6})

Federal Supply Codes for Manufacturers

00213
Nytronics Comp. Group Inc.
Subsidiary of Nytronics Inc.
Formerly Sage Electronics
Rochester, New York

00327
Welwyn International, Inc.
Westlake, Ohio

00656
Aerovox Corp.
New Bedford, Massachusetts

00686
Film Capacitors, Inc.
Passaic, New Jersey

00779
AMP Inc.
Harrisburg, Pennsylvania

01121
Allen-Bradley Co.
Milwaukee, Wisconsin

01281
TRW Electronic Comp.
Semiconductor Operations
Lawndale, California

01295
Texas Instruments, Inc
Semiconductor Group
Dallas, Texas

01537
Motorola Communications &
Electronics Inc.
Franklin Park, Illinois

01686
RCL Electronics Inc.
Manchester, New Hampshire

01730
Replaced by 73586

01884
Use 56289
Sprague Electric Co
Dearborn Electronic Div.
Lockwood, Florida

02114
Ferroxcube Corp
Saugerties, New York

02131
General Instrument Corp.
Harris ASW Div
Westwood, Maine

02395
Rason Mfg. Co
Brooklyn, New York

02533
Snelgrove, C.R. Co., Ltd
Don Mills, Ontario, Canada
M3B 1M2

02606
Fenwal Labs
Div of Travenal Labs
Morton Grove, Illinois

02660
Bunker Ramo Corp., Conn Div.
Formerly Amphenol-Borg
Electric Corp.
Broadview, Illinois

02799
Areo Capacitors, Inc.
Chatsworth, California

03508
General Electric Co.
Semiconductor Products
Syracuse, New York

03614
Replaced by 71400

03651
Replaced by 44655

03797
Eldema Div.
Genisco Technology Corp.
Compton, California

03877
Transistron Electronic Corp.
Wakefield, Massachusetts

03888
KDI Pyrofilm Corp.
Whippany, New Jersey

03911
Clairex Electronics Div.
Clairex Corp.
Mt. Vernon, New York

03980
Muirhead Inc.
Mountainside, New Jersey

04009
Arrow Hart Inc.
Hartford, Connecticut

04062
Replaced by 72136

04202
Replaced by 81312

04217
Essex International Inc.
Wire & Cable Div.
Anaheim, California

04221
Aemco, Div. of
Midtex Inc.
Mankato, Minnesota

04222
AVX Ceramics Div
AVX Corp
Myrtle Beach, Florida

04423
Telonic Industries
Laguna Beach, California

04645
Replaced by 75376

04713
Motorola Inc. Semiconductor
Products
Phoenix, Arizona

04946
Standard Wire & Cable
Los Angeles, California

05082
Replaced by 94988

05236
Jonathan Mfg. Co.
Fullerton, California

05245
Components Corp. now
Corcom, Inc.
Chicago, Illinois

05277
Westinghouse Electric Corp.
Semiconductor Div.
Youngwood, Pennsylvania

05278
Replaced by 43543

05279
Southwest Machine &
Plastic Co.
Glendora, California

05397
Union Carbide Corp.
Materials Systems Div.
New York, New York

05571
Use 56289
Sorague Electric Co.
Pacific Div.
Los Angeles, California

05574
Viking Industries
Chatsworth, California

05704
Replaced by 16258

05820
Wakefield Engineering Inc.
Wakefield, Massachusetts

06001
General Electric Co.
Electronic Capacitor &
Battery Products Dept
Columbia, South Carolina

06136
Replaced by 63743

06383
Panduit Corp.
Tinley Park, Illinois

06473
Bunker Ramo Corp
Amphenol SAMS Div
Chatsworth, California

06555
Beede Electrical Instrument Co
Penacook, New Hampshire

06739
Electron Corp
Littleton, Colorado

06743
Clevite Corp
Cleveland, Ohio

06751
Components, Inc. Semcor Div.
Phoenix, Arizona

06860
Gould Automotive Div.
City of Industry, California

06961
Vernitron Corp., Piezo
Electric Div.
Formerly Clevite Corp., Piezo
Electric Div.
Bedford, Ohio

06980
Eimac Div
Varian Associates
San Carlos, California

07047
The Ross Milton Co.
South Hampton, Pennsylvania

07115
Replaced by 14674

07138
Westinghouse Electric Corp.,
Electronic Tube Div.
Horsehead, New York

07233
TRW Electronic Components
Cinch Graphic
City of Industry, California

07256
Silicon Transistor Corp.
Div. of BBF Group Inc.
Chelmsford, Massachusetts

07261
Aumet Corp.
Culver City, California

07263
Fairchild Semiconductor
Div. of Fairchild Camera
& Instrument Corp
Mountain View, California

07344
Bircher Co., Inc.
Rochester, New York

07597
Burndy Corp.
Tape/Cable Div.
Rochester, New York

07792
Lerma Engineering Corp.
Northampton, Massachusetts

07910
Teledyne Semiconductor
Formerly Continental Device
Hawthorne, California

07933
Use 49956
Raytheon Co
Semiconductor Div. HQ
Mountain View, California

08225
Industro Transistor Corp
Long Island City, New York

Federal Supply Codes for Manufacturers (cont)

08261
Spectra Strip Corp.
Garden Grove, California

08530
Reliance Mica Corp.
Brooklyn, New York

08806
General Electric Co.
Miniature Lamp Products Dept
Cleveland, Ohio

08863
Nylomatic Corp.
Norrisville, Pennsylvania

08988
Use 53085
Skottie Electronics Inc.
Archbald, Pennsylvania

09214
G.E. Co. Semi-Conductor
Products Dept.
Power Semi-Conductor
Products OPN Sec.
Auburn, New York

09353
C and K Components
Watertown, Massachusetts

09423
Scientific Components, Inc.
Santa Barbara, California

09922
Burndy Corp.
Norwalk, Connecticut

09969
Dale Electronics Inc.
Yankton, S. Dakota

10059
Barker Engineering Corp.
Formerly Amerace, Amerace
ESNA Corp
Kenilworth, New Jersey

11236
CTS of Berne
Berne, Indiana

11237
CTS Keene Inc.
Paso Robles, California

11358
CBS Electronic Div.
Columbia Broadcasting System
Newburyport, Minnesota

11403
Best Products Co
Chicago, Illinois

11503
Keystone Columbia Inc.
Warren, Michigan

11532
Teledyne Relays
Hawthorne, California

11711
General Instrument Corp.
Rectifier Division
Hicksville, New York

11726
Qualidyne Corp.
Santa Clara, California

12014
Chicago Rivet & Machine Co.
Bellwood, Illinois

12040
National Semiconductor Corp.
Danburry, Connecticut

12060
Diodes, Inc.
Chatsworth, California

12136
Philadelphia Handle Co.
Camden, New Jersey

12300
Potter-Brumfield Div.
AMF Canada LTD.
Guelph, Ontario, Canada

12323
Presin Co., Inc.
Shelton, Connecticut

12327
Freeway Corp. formerly
Freeway Washer & Stamping Co.
Cleveland, Ohio

12443
The Budd Co. Polychem Products
Plastic Products Div.
Bridgeport, Pennsylvania

12615
U.S. Terminals Inc.
Cincinnati, Ohio

12617
Hamlin Inc.
Lake Mills, Wisconsin

12697
Clarostat Mfg. Co.
Dover, New Hampshire

12749
James Electronics
Chicago, Illinois

12856
Micrometals
Sierra Madre, California

12954
Dickson Electronics Corp.
Scottsdale, Arizona

12969
Unitrode Corp.
Watertown, Massachusetts

13103
Thermalloy Co., Inc.
Dallas, Texas

13327
Solitron Devices Inc.
Tappan, New York

13511
Amphenol Cadre Div
Bunker-Ramo Corp
Los Gatos, California

13606
Use 56289
Sprague Electric Co.
Transistor Div.
Concord, New Hampshire

13839
Replaced by 23732

14099
Semtech Corp.
Newbury Park, California

14140
Edison Electronic Div.
Mc Gray-Edison Co.
Manchester, New Hampshire

14193
Cal-R-Inc. formerly
California Resistor, Corp.
Santa Monica, California

14298
American Components, Inc.
an Insilco Co.
Conshohocken, Pennsylvania

14655
Cornell-Dublier Electronics
Division of Federal Pacific
Electric Co. Govt. Control Dept.
Newark, New Jersey

14752
Electro Cube Inc.
San Gabriel, California

14869
Replaced by 96853

14936
General Instrument Corp.
Semi Conductor Products Group
Hicksville, New York

15636
Elec-Trol Inc.
Saugus, California

15801
Fenwal Electronics Inc.
Div. of Kidde Walter and Co., Inc.
Framingham, Massachusetts

15818
Teledyne Semiconductors,
formerly Ametco Semiconductor
Mountain View, California

15849
Litton Systems Inc. Useco Div.
formerly Useco Inc.
Van Nuys, California

15898
International Business
Machines Corp
Essex Junction, Vermont

15909
Replaced by 14140

16258
Space-Lok Inc.
Burbank, California

16299
Corning Glass
Electronic Components Div.
Raleigh, North Carolina

16332
Replaced by 28478

16473
Cambridge Scientific Ind.
Div. of Chemed Corporation
Cambridge, Maryland

16742
Paramount Plastics
Fabricators, Inc.
Downey, California

16758
Delco Electronics
Div. of General Motors Corp.
Kokomo, Indiana

17001
Replaced by 71468

17069
Circuit Structures Lab.
Burbank, California

17338
High Pressure Eng. Co., Inc.
Oklahoma City, Oklahoma

17545
Atlantic Semiconductors, Inc.
Asbury Park, New Jersey

17856
Siliconix, Inc.
Santa Clara, California

17870
Replaced by 14140

18178
Vactec Inc
Maryland Heights, Missouri

18324
Signetics Corp.
Sunnyvale, California

18612
Vishay Resistor Products Div
Vishay Intertechnology Inc.
Malvern, Pennsylvania

18736
Voltronics Corp
Hanover, New Jersey

18927
GTE Sylvania Inc
Precision Material Group
Parts Division
Titusville, Pennsylvania

19451
Perine Machinery & Supply Co.
Seattle, Washington

19701
Electro-Midland Corp
Mepco-Electra Inc
Mineral Wells, Texas

20584
Enochs Mfg. Inc
Indianapolis, Indiana

Federal Supply Codes for Manufacturers (cont)

20891
Self-Organizing Systems, Inc.
Dallas, Texas

21604
Bucheye Stamping Co.
Columbus, Ohio

21845
Solitron Devices Inc.
Transistor Division
Riveria Beach, Florida

22767
ITT Semiconductors
Palo Alto, California

23050
Product Comp. Corp.
Mount Vernon, New York

23732
Tracor Inc.
Rockville, Maryland

23880
Stanford Applied Engrng.
Santa Clara, California

23936
Pamotor Div., Wm. J. Purdy Co.
Burlingame, California

24248
Replaced by 94222

24355
Analog Devices Inc.
Norwood, Massachusetts

24655
General Radio
Concord, Massachusetts

24759
Lenox-Fugle Electronics Inc.
South Plainfield, New Jersey

25088
Siemen Corp.
Isilen, New Jersey

25403
Amperex Electronic Corp.
Semiconductor &
Micro-Circuits Div.
Slatersville, Rhode Island

27014
National Semiconductor Corp.
Santa Clara, California

27264
Molex Products
Downers Grove, Illinois

28213
Minnesota Mining & Mfg. Co
Consumer Products Div.
St. Paul, Minnesota

28425
Serv-/-Link formerly
Bohannan Industries
Fort Worth, Texas

28478
Deltrol Controls Div.
Deltrol Corporation
Milwaukee, Wisconsin

28480
Hewlett Packard Co.
Corporate HQ
Palo Alto, California

28520
Heyman Mfg. Co.
Kenilworth, New Jersey

29083
Monsanto, Co., Inc.
Santa Clara, California

29604
Stackpole Components Co.
Raleigh, North Carolina

30148
AB Enterprise Inc.
Ahoskie, North Carolina

30323
Illinois Tool Works, Inc.
Chicago, Illinois

31091
Optimax Inc.
Colmar, Pennsylvania

32539
Mura Corp.
Great Neck, New York

32767
Griffith Plastic Corp.
Burlingame, California

32879
Advanced Mechanical
Components
Northridge, California

32897
Erie Technological Products, Inc
Frequency Control Div.
Carlisle, Pennsylvania

32997
Bourns Inc.
Trimpot Products Division
Riverside, California

33173
General Electric Co.
Products Dept.
Owensboro, Kentucky

34333
Silicon General
Westminister, California

34335
Advanced Micro Devices
Sunnyvale, California

34802
Electromotive Inc.
Kenilworth, New Jersey

37942
P.R. Mallory & Co., Inc.
Indianapolis, Indiana

42498
National Radio
Melrose, Massachusetts

43543
Nytronics Inc.
Transformer Co. Div.
Geneva, New York

44655
Ohmite Mfg. Co.
Skokie, Illinois

49671
RCA Corp.
New York, New York

49956
Raytheon Company
Lexington, Massachusetts

50088
Mostek Corp.
Carrollton, Texas

50579
Litronix Inc.
Cupertino, California

51605
Scientific Components Inc.
Linden, New Jersey

53021
Sangamo Electric Co.
Springfield, Illinois

54294
Cutler-Hammer Inc. formerly
Shallcross, A Cutter-Hammer Co.
Selma, North Carolina

55026
Simpson Electric Co.
Div. of Am. Gage and Mach. Co.
Elgin, Illinois

56289
Sprague Electric Co.
North Adams, Massachusetts

58474
Superior Electric Co.
Bristol, Connecticut

60399
Torin Corp. formerly
Torrington Mfg. Co.
Torrington, Connecticut

63743
Ward Leonard Electric Co., Inc.
Mount Vernon, New York

64834
West Mfg. Co.
San Francisco, California

65092
Weston Instruments Inc
Newark, New Jersey

66150
Winslow Tele-Tronics Inc.
Eaton Town, New Jersey

70485
Atlantic India Rubber Works
Chicago, Illinois

70563
Amperite Company
Union City, New Jersey

70903
Belden Corp.
Geneva, Illinois

71002
Birnback Radio Co., Inc.
Freeport, New York

71400
Bussmann Mfg.
Div. of McGraw-Edison Co.
Saint Louis, Missouri

71450
CTS Corp.
Elkhart, Indiana

71468
ITT Cannon Electric Inc.
Santa Ana, California

71482
Clare, C.P. & Co.
Chicago, Illinois

71590
Centrelab Electronics
Div. of Globe Union Inc.
Milwaukee, Wisconsin

71707
Coto Coil Co., Inc.
Providence, Rhode Island

71744
Chicago Miniature Lamp Works
Chicago, Illinois

71785
TRW Electronics Components
Cinch Connector Operations Div.
Elk Grove Village
Chicago, Illinois

72005
Wilber B. Driver Co.
Newark, New Jersey

72092
Replaced by 06980

72136
Electro Motive Mfg. Co.
Williamantic, Connecticut

72259
Nytronics Inc.
Pelham Manor, New Jersey

72619
Dialight Div
Amperex Electronic Corp.
Brooklyn, New York

72653
G.C. Electronics
Div. of Hydrometals, Inc.
Brooklyn, New York

72665
Replaced by 90303

72794
Dzus Fastener Co., Inc.
West Islip, New York

72928
Gulton Ind. Inc.
Gudeman Div.
Chicago, Illinois

Federal Supply Codes for Manufacturers (cont)

72982
Erie Tech. Products Inc.
Erie, Pennsylvania

73138
Bechman Instrument Inc.
Helipot Division
Fullerton, California

73293
Hughes Aircraft Co.
Electron Dynamics Div.
Torrance, California

73445
Amperex Electronic Corp.
Hicksville, New York

73559
Carling Electric Inc.
West Hartford, Connecticut

73586
Circle F Industries
Trenton, New Jersey

73734
Federal Screw Products, Inc.
Chicago, Illinois

73743
Fischer Special Mfg. Co.
Cincinnati, Ohio

73899
JFD Electronics Co.
Components Corp.
Brooklyn, New York

73949
Guardian Electric Mfg. Co.
Chicago, Illinois

74199
Quan Nichols Co.
Chicago, Illinois

74217
Radio Switch Corp
Marlboro, New Jersey

74276
Signalite Div.
General Instrument Corp.
Neptune, New Jersey

74306
Piezo Crystal Co.
Carlisle, Pennsylvania

74542
Hoyt Elect. Instr. Works
Penacook, New Hampshire

74970
Johnson E.F., Co.
Waseca, Minnesota

75042
TRW Electronics Components
IRC Fixed Resistors
Philadelphia, Pennsylvania

75376
Kurz-Kasch Inc
Dayton, Ohio

75378
CTS Knights Inc
Sandwich, Illinois

75382
Kulka Electric Corp.
Mount Vernon, New York

75915
Littlefuse Inc.
Des Plaines, Illinois

76854
Oak Industries Inc.
Switch Div.
Crystal Lake, Illinois

77342
AMF Inc.
Potter & Brumfield Div.
Princeton, Indiana

77638
General Instrument Corp.
Rectifier Division
Brooklyn, New York

77969
Rubbercraft Corp. of CA. LTD.
Torrance, California

78189
Shakeproof
Div. of Illinois Tool Works Inc.
Elgin, Illinois

78277
Sigma Instruments, Inc.
South Braintree, Massachusetts

78488
Stackpole Carbon Co.
Saint Marys, Pennsylvania

78553
Eaton Corp. Engineered
Fastener Div.
Tinnerman Plant
Cleveland, Ohio

79136
Waldes Kohinoor Inc.
Long Island City, New York

79497
Western Rubber Company
Goshen, Indiana

79963
Zierick Mfg. Corp.
Mt. Kisko, New York

80031
Electro-Midland Corp.
Mepco Div.
A North American Phillips Co.
Morristown, New Jersey

80145
LFE Corp., Process Control Div.
formerly API Instrument Co.
Chesterland, Ohio

80183
Use 56289
Sprague Products
North Adams, Massachusetts

80294
Bourns Inc., Instrument Div.
Riverside, California

80583
Hammarlund Mfg. Co., Inc.
Red Bank, New Jersey

80640
Arnold Stevens, Inc.
South Boston, Massachusetts

81073
Grayhill, Inc.
La Grange, Illinois

81312
Winchester Electronics
Div. of Litton Industries Inc.
Oakville, Connecticut

81483
Therm-O-Disc Inc.
Mansfield, Ohio

81483
International Rectifier Corp.
Los Angeles, California

81590
Korry Mfg. Co.
Seattle, Washington

81741
Chicago Lock Co.
Chicago, Illinois

82305
Palmer Electronics Corp.
South Gate, California

82389
Switchcraft Inc.
Chicago, Illinois

82415
North American Phillips
Controls Corp.
Frederick, Maryland

82872
Roanwell Corp.
New York, New York

82877
Rotron Inc.
Woodstock, New York

82879
ITT Royal Electric Div.
Pawtucket, Rhode Island

83003
Varo Inc.
Garland, Texas

83058
The Carr Co., United Can Div.
of TRW
Cambridge, Massachusetts

83298
Bendix Corp.
Electric Power Div
Eatontown, New Jersey

83330
Herman H. Smith, Inc.
Brooklyn, New York

83478
Rubbercraft Corp
of America, Inc.
West Haven, Connecticut

83594
Burroughs Corp.
Electronic Components Div.
Plainfield, New Jersey

83740
Union Carbide Corp.
Battery Products Div.
formerly Consumer Products Div.
New York, New York

84171
Arco Electronics
Great Neck, New York

84411
TRW Electronic Components
TRW Capacitors
Ogallala, Nebraska

84613
Fuse Indicator Corp.
Rockville, Maryland

84682
Essex International Inc.
Industrial Wire Div.
Peabody, Massachusetts

86577
Precision Metal Products
of Malden Inc.
Stoneham, Massachusetts

86684
Radio Corp. of America
Electronic Components Div.
Harrison, New Jersey

86928
Seastrom Mfg. Co., Inc.
Glendale, California

87034
Illuminated Products inc.
Subsidiary of Oak Industries Inc.
Anahiem, California

88219
Gould Inc.
Industrial Div
Trenton, New Jersey

88245
Litton Systems Inc.
Useco Div.
Van Nuys, California

88419
Cornell-Dubilier Electronic Div.
Federal Pacific Co.
Fuquay-Varian, North Carolina

88486
Plastic Wire & Cable
Jewitt City, Connecticut

88690
Replaced by 04217

89536
John Fluke Mfg. Co., Inc.
Seattle, Washington

89730
G.E. Co., Newark Lamp Works
Newark, New Jersey

Federal Supply Codes for Manufacturers (cont)

90201
Mallory Capacitor Co.
Div. of P.R. Mallory Co., Inc.
Indianapolis, Indiana

90211
Use 56365
Square D Co.
Chicago, Illinois

90215
Best Stamp & Mfg. Co.
Kansas City, Missouri

90303
Mallory Battery Co.
Div. of Mallory Co., Inc.
Tarrytown, New York

91094
Essex International Inc.
Suglex/IWP Div.
Newmarket, New Hampshire

91293
Johanson Mfg. Co.
Boonton, New Jersey

91407
Replaced by 58474

91502
Associated Machine
Santa Clara, California

91506
Augat Inc.
Attleboro, Massachusetts

91637
Dale Electronics Inc.
Columbus, Nebraska

91662
Elco Corp.
Willow Grove, Pennsylvania

91737
Use 71468
Gremar Mfg. Co., Inc.
ITT Cannon/Gremar
Santa Ana, California

91802
Industrial Devices, Inc.
Edgewater, New Jersey

91833
Keystone Electronics Corp.
New York, New York

91836
King's Electronics Co., Inc.
Tuckahoe, New York

91929
Honeywell Inc.
Micro Switch Div.
Freeport, Illinois

91934
Miller Electric Co., Inc.
Div. of Aunet
Woonsocket, Rhode Island

92194
Alpha Wire Corp.
Elizabeth, New Jersey

93332
Sylvania Electric Products
Semiconductor Products Div.
Woburn, Massachusetts

94145
Replaced by 49956

94154
Use 94988
Wagner Electric Corp.
Tung-Sol Div.
Newark, New Jersey

94222
Southco Inc. formerly
South Chester Corp.
Lester, Pennsylvania

95146
Alco Electronic Products Inc.
Lawrence, Massachusetts

95263
Leecraft Mfg. Co.
Long Island City, New York

95264
Replaced by 98278

95275
Vitramon Inc.
Bridgeport, Connecticut

95303
RCA Corp.
Receiving Tube Div.
Cincinnati, Ohio

95348
Gordo's Corp.
Bloomfield, New Jersey

95354
Methode Mfg. Corp.
Rolling Meadows, Illinois

95712
Bendix Corp.
Electrical Components Div.
Microwave Devices Plant
Franklin, Indiana

95987
Weckesser Co. Inc.
Chicago, Illinois

96733
San Fernando Electric Mfg. Co.
San Fernando, California

96853
Gulton Industries Inc.
Measurement and Controls Div.
formerly Rustrak Instruments Co.
Manchester, New Hampshire

96881
Thomson Industries, Inc.
Manhasset, New York

97540
Master Mobile Mounts, Div. of
Whitehall Electronics Corp.
Ft. Meyers, Florida

97913
Industrial Electronic
Hardware Corp.
New York, New York

97945
Penwalt Corp.
SS White Industrial Products Div.
Piscataway, New Jersey

97966
Replaced by 11358

98094
Replaced by 49956

98159
Rubber-Teck, Inc.
Gardena, California

98278
Malco A Microdot Co., Inc.
Connector & Cable Div.
Pasadena, California

98291
Sealectro Corp.
Mamaroneck, New York

98388
Royal Industries
Products Div.
San Diego, California

98743
Replaced by 12749

98925
Replaced by 14433

99120
Plastic Capacitors, Inc.
Chicago, Illinois

99217
Bell Industries Elect.
Comp. Div.
formerly Southern Elect. Div
Burbank, California

99392
STM
Oakland, California

99515
ITT Jennings Monrovia Plant
Div. of ITT Jennings formerly
Marshall Industries Capacitor Div.
Monrovia, California

99779
Use 29587
Bunker-Ramo Corp.
Barnes Div.
Landsdowne, Pennsylvania

99800
American Precision Industries Inc.
Delevan Division
East Aurora, New York

99942
Centrelab Semiconductor
Centrelab Electronics Div. of
Globe-Union Inc.
El Monte, California

Toyo Electronics
(R-Ohm Corp.)
Irvine, California

National Connector
Minneapolis, Minnesota

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Motherland Corporation
24 Hatkhola Rd., Tikatuli
Dacca 3, Bangladesh
Tel: 257249 or 255776

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Fluke (Belgium) S.A./N.V.
6, Rue de Geneve
1140 Brussels, Belgium
Tel: (2) 2164090, TLX: 26312

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Coasin Bolivia S.R.L.
Casilla 7295, La Paz, Bolivia
Tel: 40962, TLX: 3233

Brazil •
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Comercio LTDA
Al Amazonas 422,
Alphaville, Baruen,
CEP 06400 Sao Paulo, Brazil
Tel. (011) 421-5477, TLX: 01135589

Fluke Brasil-Industria E
Comercio LTDA
Av Henrique Valadares, 23/401
Rio de Janeiro, Brazil
Tel. 252-1297

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Rank O'Connor's (PTE) Limited
No. 8, Blk. D
Sufri Shop House Complex
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Bandar Seri Begawan, Brunei
Tel 26680

Bulgaria ■
Amtest Associates Ltd.
Clarence House, 31, Clarence St.
Staines, Middlesex TW18 4SY
United Kingdom
Tel (784) 63555, TLX: 928855

Canada •
Allan Crawford Assoc., Ltd.
#14 1935 30th Ave. N.E.
Calgary, Alberta T2E 6Z5
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Appendix 11C
Manual Change Information

REF OR OPTION NO.	ASSEMBLY NAME	FLUKE PART NO.	*To adapt manual to earlier rev configurations perform changes in decending order (by no.), ending with change under desired rev letter																						
			—	A	B	C	D	E	F	G	H	J	K	L	M	N	P									
A1	Display PCA	718502	+	+	+	+	+	+	+	X																
A2	Printer Assembly	646596	+	+	+	+	+	X																		
A3	Printer Interface PCA	639344	+	+	+	+	+	+	+	+	+	+	+	X												
A4	Controller PCA	752956	+	+	+	+	+	+	X																	
A5	Memory PCA	752949	+	+	X																					
A6	Transformer PCA	639245	+	+	+	+	X																			
A7	Motherboard PCA	639237	+	+	+	+	+	+	X																	
A8	Power Supply PCA	716084	X																							

X = The PCB revision levels documented in this manual.
• = These revision letters were never used in the instrument.
— = No revision letter on the PCB.
+ = These revision levels are not documented in this manual.

INTRODUCTION

The 2280 Series manual set (User Guide, System Guide, and Service Manual) documents the 2280B Data Logger. These manuals, although compatible with the 2280A Data Logger, do require some further explanation. Some features can be used with the 2280B, but not on the 2280A. Several option assemblies can be used with the 2280B, but not with the 2280A. This Appendix describes these differences.

FEATURES

Features of the 2280A differ from those of the 2280B in the following areas:

- Alarm Limits: alarm limits cannot be changed while scanning.
- Pseudo Channels: pseudo channels values cannot be changed while scanning.
- Scan Once Trigger Mode: not available on 2280A.
- Remotely Terminated Thermocouples: not supported by 2280A.
- Time of Day: not shown during scanning.
- Internal Tape Transfer Speed: increased speed not available with 2280A.

OPTIONS

The following option assemblies cannot be used with the 2280A:

- RTD/Resistance Scanner and Connector (2280B-163/-177)
- Counter/Totalizer (2280B-167)
- Transducer Excitation Module and Connector (2280A-164/-174)
- AC Voltage Input Connector (2280A-160)
- Analog Output (2280B-170)

INTRODUCTION

The 2280 Series manual set (User Guide, System Guide, and Service Manual) documents the 2280B Data Logger. These manuals, although compatible with the 2285B Data Logger, do require some further explanation. Some features can be used with the 2280B, but not with the 2285B. Also, some option assemblies cannot be used with the 2285B. This Appendix describes these differences.

FEATURES

The 2285B is an economical solution to a data logging system not requiring the expansion capabilities of the 2280B. The following configuration is possible:

- The channel total for the 2285B is limited to 100.
- One High Performance A/D Converter (Option 2280A-161) can be installed.

OPTIONS

The following option assemblies cannot be used with the 2285B:

- Advanced Math Processor (2280A-211)
- DC Cartridge Tape (2280A-214)
- Counter/Totalizer (2280B-167)
- Analog Output (2280B-170)

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